United States Patent [19]

Mundt et al.

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[45] **Date of Patent: Mar. 25, 1986**

[54] **PROCESS FOR FORMING RETROGRADE DOPANT DISTRIBUTIONS UTILIZING SIMULTANEOUS OUTDIFFUSION OF DOPANTS**

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[73] Assignee: **NCR Corporation,** Dayton, Ohio

[21] Appl. No.: 677,636

[22] Filed: **Dec. 3, 1984**

[51] **Int. Cl.**[4] **H01L 21/20;** H01L 21/225

[52] **U.S. Cl.** ..... **148/191;** 29/571; 29/576 B; 29/576 W; 148/187; 148/175; 156/643; 357/42; 357/50

[58] **Field of Search** ..... 29/571, 576 B, 576 W; 148/187, 191, 175; 156/643; 357/42, 50

[56] **References Cited**

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Chen, "Quadruple-Well CMOS for VLSI Technology", IEEE Transactions on Electron Devices, vol. ED-31, No. 7, Jul. 1984, pp. 910-919.

Manoliu et al., "High-Density and Reduced Latchup Susceptibility CMOS Technology for VLIS", IEEE Electron Device Letters, vol. EDL-4, No. 7, Jul. 1983, pp. 233-235.

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[57] **ABSTRACT**

A retrograde dopant distribution is provided in a semiconductor substrate by the combined use of indiffusion and surface outdiffusion and without the use of high energy implants or buried epitaxial layers. The retrograde dopant distribution is provided both in the n-well and the p-well regions to a depth sufficient to accommodate deep trench isolation structures.

8 Claims, 8 Drawing Figures

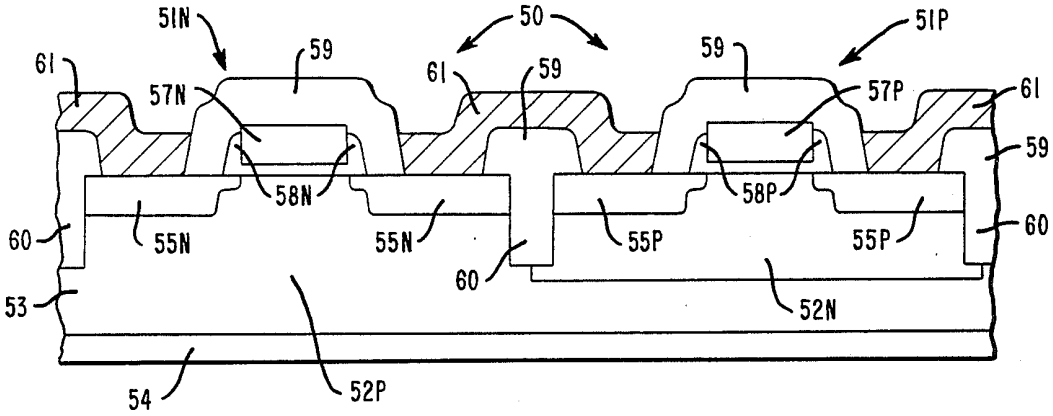


FIG. 1

PRIOR ART

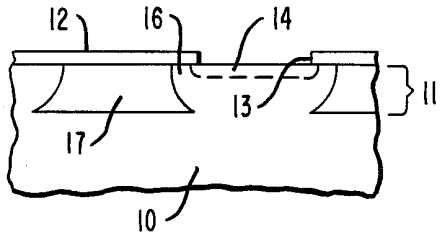


FIG. 2

PRIOR ART

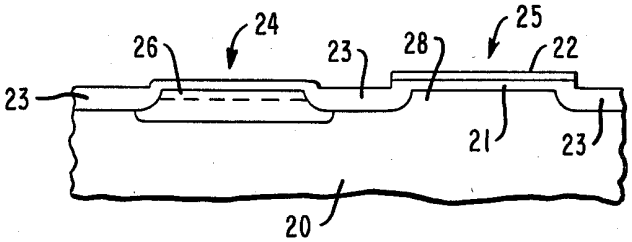


FIG. 3

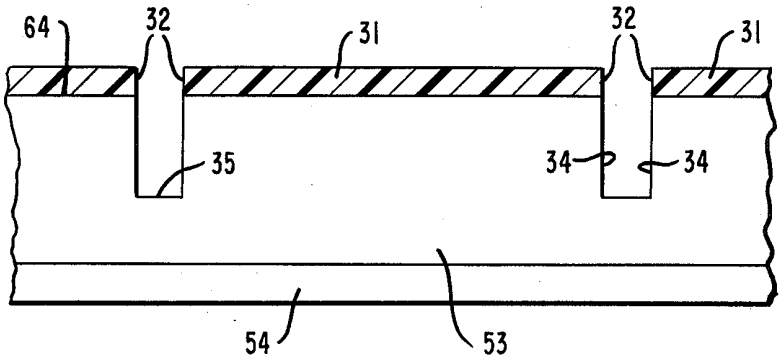


FIG. 4

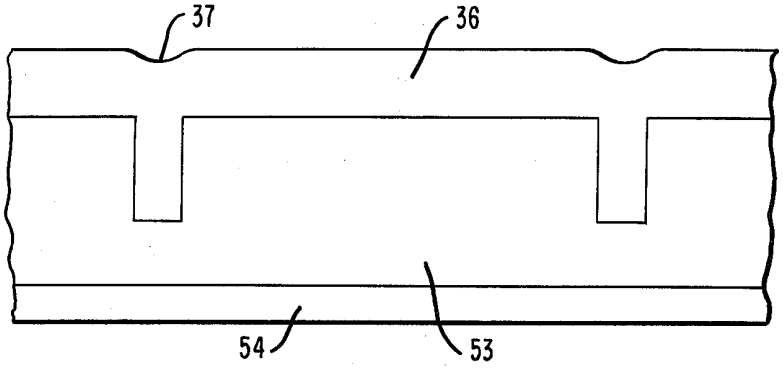


FIG. 5

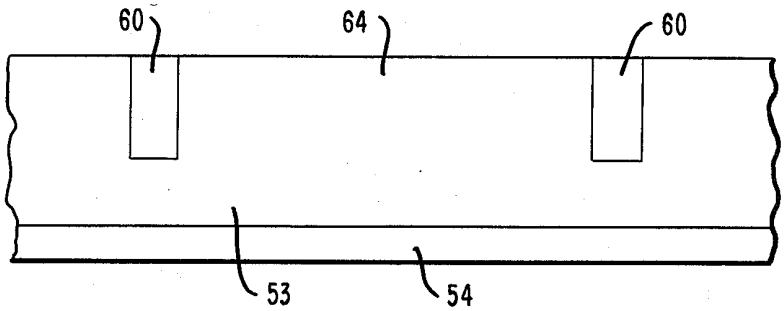
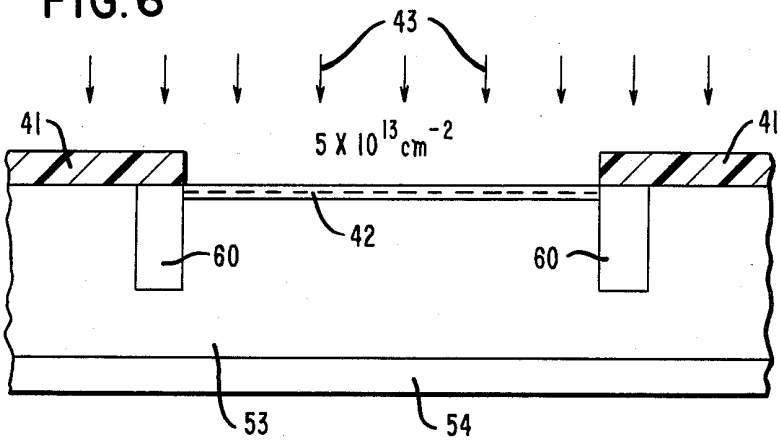


FIG. 6



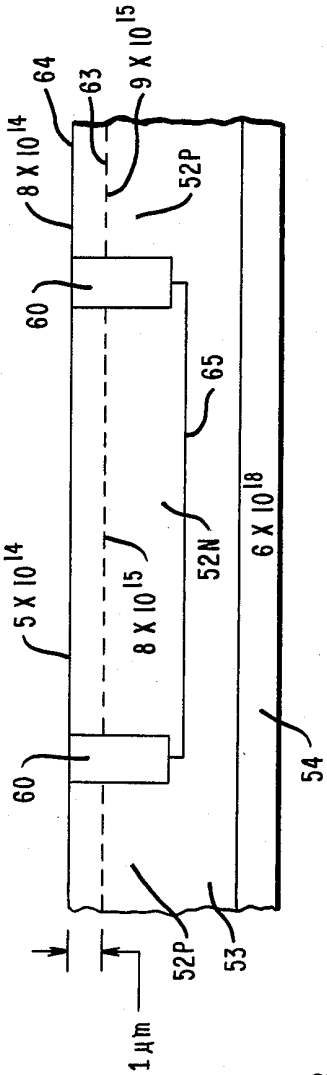


FIG. 7

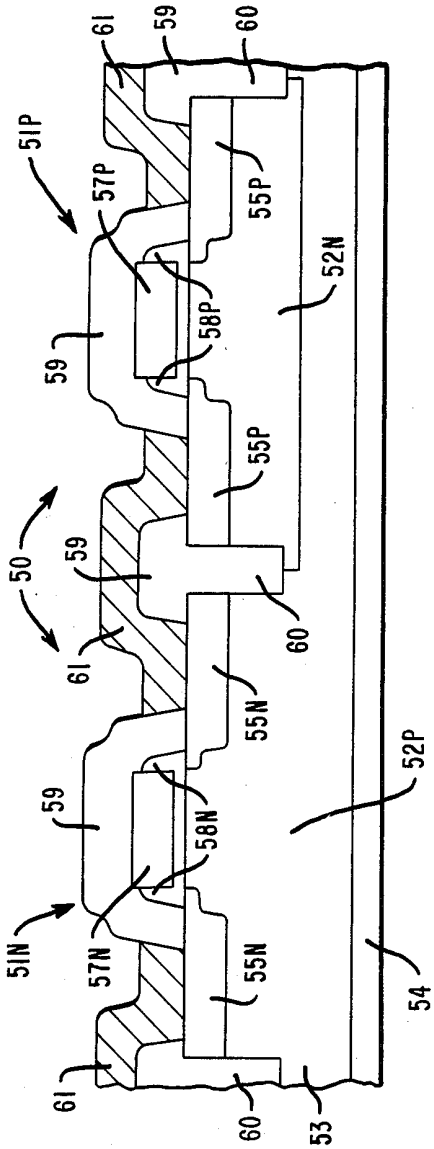


FIG. 8

PROCESS FOR FORMING RETROGRADE DOPANT DISTRIBUTIONS UTILIZING SIMULTANEOUS OUTDIFFUSION OF DOPANTS

BACKGROUND OF THE INVENTION

The present invention relates to a simplified process for forming retrograde dopant distributions in integrated circuit structures, that is, dopant distributions which increase in a vertically inward or downward direction from the surface of a layer or body such as a semiconductor substrate. As used here in reference to the present invention, the word "retrograde" also connotes a controlled dopant profile.

The potential advantages of a retrograde dopant distribution in semiconductor substrates are several, particularly in CMOS integrated circuit structures. The advantages are well-known and include the potential for increased device packing density and decreased susceptibility to latchup. It is believed there are available basically three approaches for forming a retrograde dopant profile. The techniques, namely, high energy implants (greater than about 200 keV), buried epitaxial layers, and outdiffusion, can be used separately or in combination.

An example of retrograde processing techniques is disclosed in Manoliu et al, "High-Density and Reduced Latchup Susceptibility of CMOS Technology for VLSI", *IEEE Electron Device Letters,* Vol. EDL-4, No. 7, July, 1983, pp. 233–235. Manoliu et al. uses the combination of a first implant in a doped substrate and a later implant in an undoped epitaxial layer. The well formation process is concluded with an anneal cycle. The specific CMOS structure and epitaxial buried layer retrograde p-well structure reportedly increases circuit density by reducing the minimum n_+-p^+ spacing while decreasing latchup susceptibility.

Chen, "Quadruple-Well CMOS for VLSI Technology", *IEEE Transactions on Electron Devices,* Vol. ED-31, No. 7, July 1984, pp. 910–919, describes a process for forming a retrograde, quadruple-well CMOS structure. The n-well and p-well retrograde doping profiles each require multiple doping steps. Essentially, the structure is a two-well structure in which deep n-type and p-type wells are separated by respective shallow n-type and p-type wells or channel stops. The shallow wells are implanted through a peripheral field oxide during the deep well implantation. Overall, the Chen process involves, first, forming deep-well windows in a planar field oxide. The p-well region is masked and a high energy phosphorus implant at 290 keV is done in the presence of the mask to define the deep n-well and the adjacent shallow n-type channel stop under the oxide. The n-well is then counter-doped with boron for threshold voltage adjustment.

After the two-implant-step formation of the retrograde n-well, the n-well is masked and a multiple doping sequence is applied to provide the p-well retrograde profile. Initially, a 120 keV boron implant is used to form a relatively deep p-well, and the adjacent shallow p-type channel stop under the oxide. Phosphorus counterdoping adjusts the n-channel threshold voltage. Then, a deep, high energy 340 keV boron implant provides the deep retrograde p-well profile which is used to eliminate latchup. The counter-doping aspects of the process i.e., the combination of high energy implants and opposite conductivity low energy counter-doping,

are also disclosed in Chen, U.S. Pat. No. 4,411,058, issued Oct. 25, 1983.

The outdiffusion of semiconductor dopants from the surfaces of silicon, mentioned above, is another well-known phenomenon, one that in the past has produced undesirable results. For example, outdiffusion from the front and rear major surfaces of semiconductor wafers leads to both macro-outdoping and micro-autodoping. Various process techniques are used to eliminate or decrease the effects of outdiffusion, including two-step processing using process interruption and/or high and low temperatures, and sealing of wafer surfaces with a mask such as silicon, silicon dioxide or silicon nitride.

Recently, outdiffusion has been used advantageously to provide a retrograde dopant distribution, but the process techniques for implementing the outdiffusion-caused retrograde dopant distribution typically are complex. For example, Steinmaier, U.S. Pat. No. 3,767,487 relates to the use of outdiffusion techniques to form selected, isolated retrograde surface-adjacent regions which are used as isolation wells for MOS or bi-polar devices. Referring to FIG. **1**, the MOS integrated circuit process disclosed in the Steinmaier '487 patent involves forming a five-micron thick n-type epitaxial layer **11** on a p-type semiconductor **10**; forming a thermal oxide masking layer **12** over the epitaxial layer having an aperture **13** which defines the p-well or isolation region; depositing a shallow p-well **14** in the surface of the epitaxial layer at the masked apertures using an oxidizing atmosphere to re-cover (not shown) the exposed substrate surface regions; etching the oxide mask to reexpose the epitaxial layer over part of the deposited impurity region beneath the masked windows; and outdiffusing the boron via the mask apertures **13** in a vacuum ampul containing silicon to provide the retrograde concentration in region **14**. In particular, the vertical retrograde dopant concentration in region **14**, that is, the relatively low surface concentration there, provides a high breakdown voltage for the NMOS device which is subsequently formed in the p-well **14**. In addition, in the surface region **16** surrounding the well **14**, the mask prevents outdiffusion, thereby providing a surface region **16** of relatively high doping concentration surrounding the retrograde well **14**. This horizontal dopant concentration gradient is used to prevent short circuits between the epitaxial layer **11** and the subsequently formed NMOS device.

As is evident from the above description, in regard to small geometry, high density structures, the Steinmaier '487 retrograde p-well fabrication process suffers from several disadvantages in addition to complexity. The shallow retrograde p-well **14** does not appear to be capable of providing the desirable retrograde dopant gradient along the deep isolation trenches which are used in some CMOS structures. The adjacent n-well **17** is capped during the outdiffusion step and does not have a retrograde dopant concentration gradient. Furthermore, the lateral dopant concentration gradient at the periphery of the p-well **14** quite obviously limits the minimum dimension of, and spacing between, the wells. In short, the complex processing of the Steinmaier '487 patent is tailored to provide a p-well-only retrograde gradient and a lateral doping gradient that are inconsistent with small geometry, high density integrated circuits.

Shappir, U.S. Pat. No. 3,921,283 uses surface outdiffusion in the fabrication of dielectrically isolated MOSFET semiconductor devices. Referring to FIG. 2, in the

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