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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.
Petitioner

v.

GODO KAISHA IP BRIDGE 1
Patent Owner.

Case IPR2017-01841¹

PETITIONER'S DEMONSTRATIVES FOR ORAL ARGUMENT

¹ Case IPR2017-01842 has been consolidated with this proceeding.

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v.

GODO KAISHA IP BRIDGE 1

Inter Partes Review

Nos. IPR2017-01841 and IPR2017-01842

U.S. Patent No. 7,893,501

PETITIONER'S ORAL ARGUMENT

Proposed Agenda

- Technology Background
- Overview of the '501 Patent
- Overview of the Prior Art
- Undisputed Issues
- Obviousness of Claims
- Issues Raised by Patent Owner and Responses
 - Claim 1: whether applied prior art discloses a transistor that includes an active region

Technology Background

Basic Elements of a MISFET (Transistor)

SFETs include:

an active region made of a substrate, located between the shallow trench isolation regions (STI);

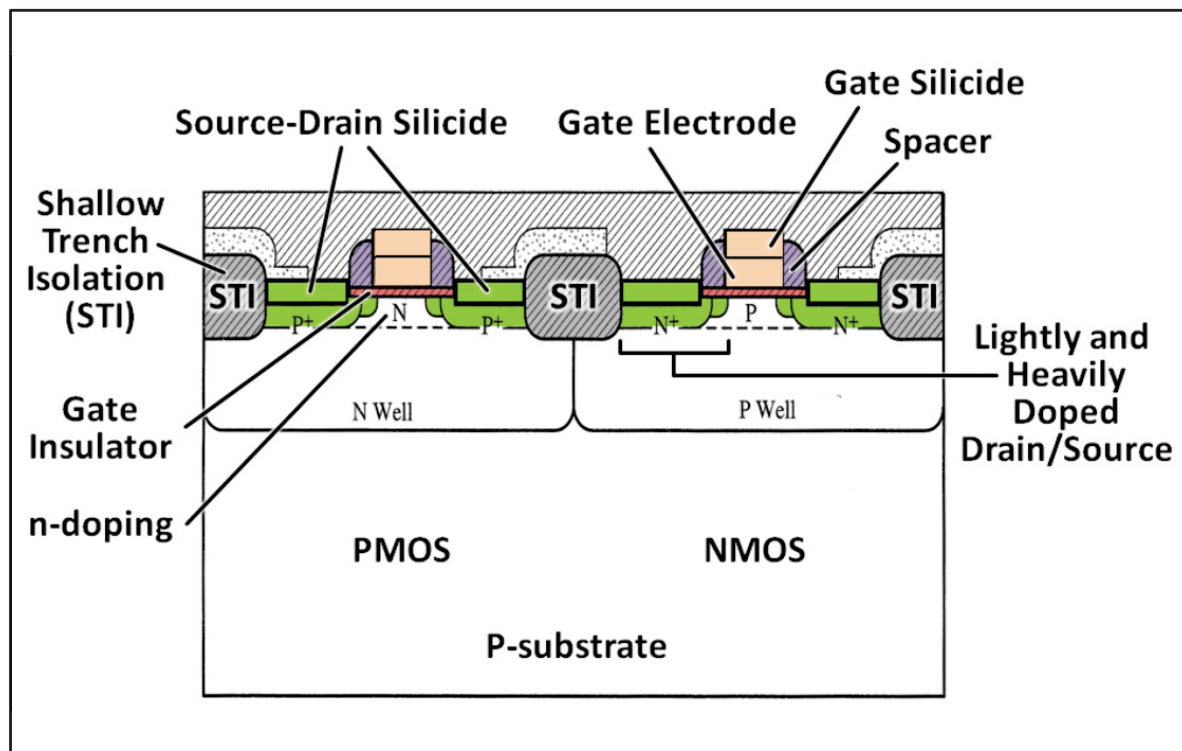
a gate insulating film (red);

a gate electrode (orange);

source and drain regions including a silicide layer (green); and

other elements such as sidewalls (purple)

Example metal-insulator-semiconductor field effect transistors (MISFETs) from Plummer textbook (1st ed. 2000):



Plummer at 86 (Ex. 1008) (annotated); see also Petition at 6-7, Paper 2; Shanfield Decl., ¶¶33-44 (Ex. 1002); Rabaey at 42-43 (Ex-1010)

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