UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

IPR2017-01841[1]
Patent 7,893,501

SUR-REPLY DECLARATION OF ALEXANDER D. GLEW PURSUANT TO JULY 20, 2018 ORDER (PAPER NO. 26)

[1] Case IPR2017-01842 has been consolidated with this proceeding.

I, Alexander D. Glew, declare:

1. My compensation and credentials are provided in Exhibit 2007.

2. Agata and Rashed do not support Dr. Shanfield's assertion that "the claim requirement that 'the MISFET includes: an active region' is met by the prior art relied upon in the grounds" (Ex. 1027, ¶¶ 10, 17-18) for the reasons below.

3. Neither Agata nor Rashed refers to a ***MISFET*** (or other ***transistor***) that "***includes***: an active region" as required by claim 1 of the '501 patent.

4. Agata's "active region 2" that Dr. Shanfield refers to (Ex. 1027, ¶17) is a region where a multi-transistor "semiconductor device" (more specifically a "sense amplifier") is formed. Ex. 1025, 5:9-18. Agata does ***not*** refer to any of the transistors (MOSFETs) in Agata's device as "including" the active region 2. To the contrary, Agata states that it is the "***sense amplifier*** [that] ***includes*** … [the] active region 2." *Id.*, 5:9-18; Abstract ("[t]he ***device includes*** … an active region"). The sense amplifier also "includes" the "isolation regions 3 for isolating the active region 2 from other ***active regions for other devices***." *Id*., 5:9-18.

5. Rashed similarly describes a multi-transistor ***"device*** [that] includes a continuous active region." Ex. 1026 at Abstract, 2:55-56. The active region is "defined … by one or more isolation structures." *Id*. at 1:51-55. Rashed does not refer to any transistor as ***including*** an active region.

6. Dr. Shanfield's assertion that Agata and Rashed illustrate that "more

than one transistor can exist in an active region" (Ex. 1027, ¶¶ 17-18) is misleading and ***irrelevant*** to the issue in this proceeding, which is whether either ***MISFET*** in the multi-transistor device of modified Igarashi Fig. 12 in the Petition "***includes***" the active region the Petition alleges is formed by isolation in that device. That multiple transistors exist in an active region ***of a multi-transistor device*** does not establish that an individual MISFET in that device somehow "includes" the ***device's*** active region. For the reasons stated in Ex. 2007, VIII.C.2. in connection with Igarashi's multi-transistor device, no transistor in the multi-transistor devices of Agata and Rashed "includes" an active region because no such transistor "includes" a region bounded by isolation.

7. Thus, neither Agata nor Rashed refutes my opinion that the claim language "MISFET includes: an active region" requires that an entire region bounded and defined by isolation be part of (i.e., included in) the MISFET, i.e., there is only one MISFET in an active region that the "MISFET includes." *See id.*, VIII.C.2.c-d. Petitioner has not cited a single document that describes a MISFET as "including" an active region where that active region is shared with another transistor, or that refutes my testimony that a POSA would have understood that an active region a MISFET "includes" is dedicated to that MISFET. *Id.*

8. To the extent Agata and Rashed are relevant at all, they ***support*** my opinion that a MISFET only "includes" an active region if the active region is

dedicated to the MISFET. Agata, Rashed, and the '501 patent refer to a structure (respectively, "sense amplifier", "device," and "MISFET") that "includes" an active region where the active region is ***dedicated*** to the structure that "includes" it.

9. Dr. Shanfield's assertion that "all functional MOSFET transistors have an active region" is unsupported and wrong—an area not defined by isolation is ***not*** an active region. *See* Ex. 2007 at VII.A, VIII.C.1.b. All transistors must have a region in the substrate where they are formed, but as the '501 patent makes clear this is a "formation region." Ex. 1001 at 3:20-28, Fig. 1.

10. Dr. Shanfield mischaracterizes my deposition testimony which addressed the term "comprise" and not "includes." Ex. 1027, ¶31; Ex. 1024 at 94:13-95:7. The open ended "comprising" transition in claim 1 does not eliminate the requirement that the "MISFET includes: an active region," which the grounds do not meet. *See* Ex. 2007 at VIII.C.

11. Dr. Shanfield's suggestion that the '501 patent does not show 1-to-1 correspondence between the active regions and MISFETs because the figures are cross sections (Ex. 1027, ¶¶ 14-15) is wrong with respect to Fig. 9A, and refuted by the '501 specification. '501 patent at 3:24-28 (each MISFET "formation region … ***includes*** the active region"). Fig. 9A is a "plane view of an MISFET" (3:8-10, 14:42-45) and illustrates isolation region 2 bounding the active region in which the transistor is formed, i.e., defining the boundary of the active region on all sides.

I understand and have been warned that willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. § 1001). I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of title 18 of the United States Code. I declare under penalty of perjury that the foregoing is true and correct.

Dated: July 27th, 2018

Alexander D. Glew

Dr. Alexander D. Glew