21.3

A Shallow Trench Isolation with SiN Guard-Ring for Sub-Quarter Micron CMOS Technologies

Takashi Ogura, Toyoji Yamamoto, Yukishige Saito,
Yoshihiro Hayashi and Tohru Mogami

Silicon Systems Research Laboratories, NEC Corporation
1120 Shimokuzawa, Sagamihara, Kanagawa 229-11,Japan

Abstract

Shallow trench isolation (STI) technology is important to realize high-speed and high-packing-density CMOS-LSIs. A new SiN guard-ring on the upper edge of filled SiO_2 for steep-sidewall STI is proposed and evaluated to improve the reverse narrow channel effect and device reliability. Good isolation characteristics and sufficient improvement of the reverse narrow channel effect are achieved for STI with SiN guard-ring structure.

Introduction

For sub-quarter micron CMOS, a new isolation technology is necessary for realizing high-performance CMOS devices, because of LOCOS isolation limitation. STI technology has been studied extensively for solving this problem[1]. In STI technology, the surface planarization for trench-filled SiO_2 is the key issue to realize good isolation characteristics. However, SiO_2 upper edge is greatly etched after CMP process, because of pre-treatment for gate oxidation. Furthermore, for scaled CMOS, steep-sidewall trench should be used for advanced STI structure, shown in Fig.1. However, "hump" in sub-threshold characteristics can be generated for steep-sidewall STI because of electric field concentration at the trench edge, as reported in ref. [2]. Therefore, in the steep-sidewall STI for scaled CMOS, the filled SiO_2 surface in trench should be a little higher than the active area surface[3].

In this paper, we present a new STI technology using SiN guard-ring and the electrical properties of STI with this new guard-ring are discussed.

SiN Guard-Ring Fabrication Process

Fig.2 illustrates the process flow for STI with SiN guard-ring. The etching of trench with the steep-sidewall, SiO_2 filling and CMP planarization were carried out after SiN pad fabrication. Next, after removing pad SiO_2 and SiN by wet etching, refilled SiN film was deposited. Filled SiO_2 surface in this stage is 50nm higher than the active area surface; this can eliminate electric field concentration at the trench edge. Finally, after SiN etching on the active area, SiN guard-ring was formed at the active area edge. Fig.3 shows cross-sectional TEM image at the active edge after gate oxidation and deposition of poly-Si film. In Fig.3(a), oxide etching at STI upper edge is suppressed by SiN guard-ring, although SiO_2 sink was caused by wet etching for conventional structure (Fig.3(b)).

Results and Discussion

A. Device characteristics

Isolation characteristics are shown in Fig.4. Punch-through voltage for SiN guard-ring STI is comparable with that for conventional STI. The I_G-V_G characteristics are shown for 2cm perimeter NMOS and PMOS capacitors utilized SiN guard-ring structure with 5.9nm gate oxide in Fig.5. No leakage current increase observed for N/P-MOS capacitors, although gate oxide thinning may be generated at the active edge by SiN guard-ring. The narrow channel characteristics of various structures are shown in Fig.6. V_T lowering for MOSFETs with the SiN guard-ring STI is smaller than those with the conventional STI and is comparable with that for tapered (=75°) sidewall STI MOSFETs; this is due to a little elevation of SiN film near the active area surface and completely filled insulators in STI. The sub-threshold characteristics of N/P-MOSFETs with the SiN guard-ring STI and conventional STI structure are shown in Fig.7. No hump characteristics are observed for the SiN guard-ring STI, although hump characteristics are observed for the conventional STI. This indicates that SiN guard-ring STI is useful for side-wall transistor action suppression.

B. Device reliability

SiN guard-ring fabrication process is worried about MOSFET performance and reliability degradation by SiN film etch-back process. Interface state density (D_{it}) for NMOSFET was evaluated by the measurement of charge-pumping current shown in Table 1. D_{it} value for N/P-MOSFET with the SiN guard-ring STI are comparable with those with the conventional STI. This result indicates MOSFETs do not have any damage by SiN etch-back process. Furthermore, hot-carrier degradation is the next issue for SiN guard-ring STI because of high mechanical stressing by SiN film. Hot-carrier effects were evaluated for various NMOSFETs, shown in Fig.9. Lifetime plot for various devices have the same line; this means SiN guard-ring has no mechanical damage.

Conclusion

A new SiN guard-ring structure for steep-sidewall STI is proposed and evaluated. Good isolation characteristics and sufficient improvement of the reverse narrow channel effect are achieved for the SiN guard-ring STI. Furthermore, it was confirmed that no device degradation, including hot-carrier effects, is achieved for MOSFET with the SiN guard-ring STI. Therefore, this new STI technology is promising for the future scaled CMOS-LSIs.

Acknowledgment

The authors would like to thank T. Kunio and H. Abe for their encouragement through this work, as well as H. Kawaguchi and H. Abiko for their helpful suggestion.

References

[1] H. Kawaguchi et al., Symp. on VLSI Tech. Dig., p125 (1997)
[2] K. Ishimaru et al., Symp. on VLSI Tech. Dig., p97 (1994)
[3] A.H. Perera et al., IEDM Tech. Dig., p679 (1995)

 0-7803-4700-6/98/$10.00 © 1998 IEEE

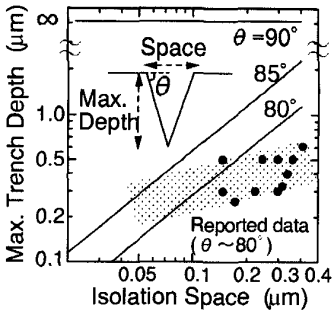
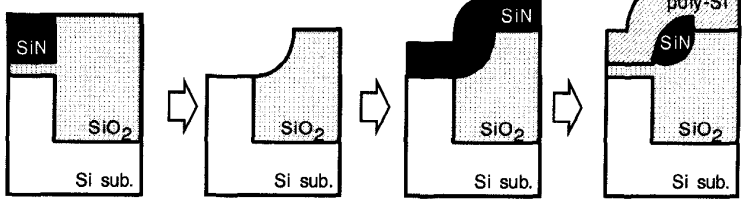


Fig.1 The relationship between isolation space and trench depth for typical trench sidewall angle. More than 80° sidewall angle is required when isolation space is reduced down to 0.1 μ m with 0.3 μ m trench depth.



(a) SiO_2 filling and CMP planarization (b) Pad oxide and SiN removal (c) SiN deposition (d) SiN etch-back, gate oxidation and poly-Si deposition

Fig.2 Process flow of SiN guard-ring STI structure.

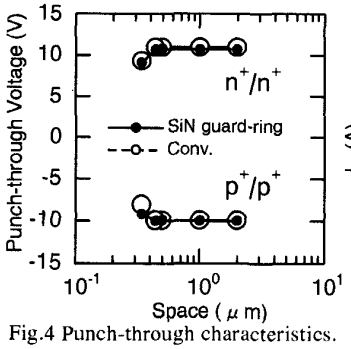


Fig.4 Punch-through characteristics.

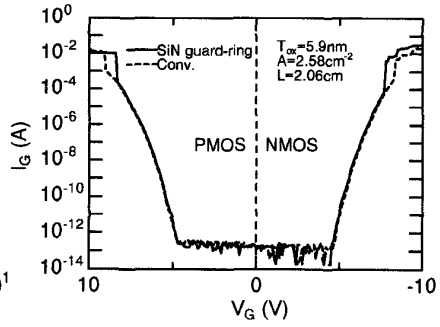
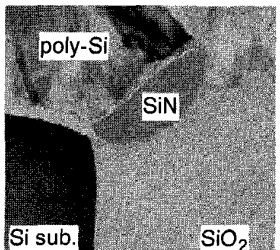
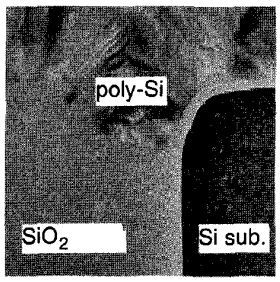


Fig.5 The I_G-V_G characteristics of MOS capacitor.



(a) SiN guard-ring structure



(b) Conventional

Fig.3 Cross sectional TEM image.

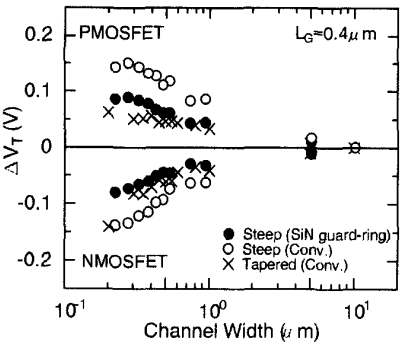


Fig.6 Threshold voltage (V_T) of MOSFETs with various channel width at V_D=±1.5V. V_T is normalized at 10 μ m channel width.

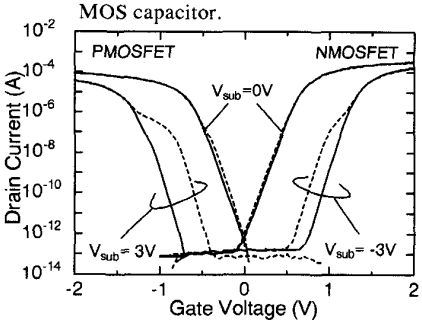
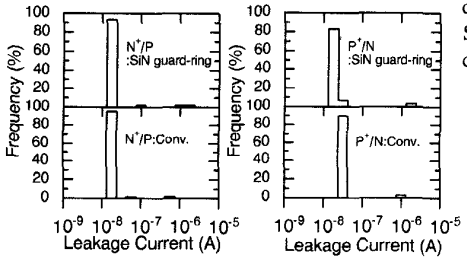


Fig.7 The sub-threshold characteristics of wide channel MOSFETs (W_G/L_G=10 μ m/0.4 μ m) at V_D=±0.1V. Solid and dotted lines indicate SiN guard-ring structure and conventional one, respectively.



(b) p^+/n diodes (a) n^+/p diodes

Fig.8 Histograms of leakage current for diodes. Reverse bias is 5V. Area and perimeter of diodes are 0.01cm^2 and 100cm, respectively

Table 1 Comparison of interface state density (D_{it}) between MOSFETs with SiN guard-ring STI and those with conventional STI.

(A) D_{it} of the active plane

	SiN guard-ring	Conv.
NMOSFET	4.6E+11	3.9E+11
PMOSFET	2.7E+11	2.5E+11

Unit : $cm^{-2} \cdot eV^{-1}$

(B) D_{it} of the active edge

	SiN guard-ring	Conv.
NMOSFET	3.4E+06	8.3E+06
PMOSFET	4.3E+06	5.7E+06

Unit : $cm^{-1} \cdot eV^{-1}$

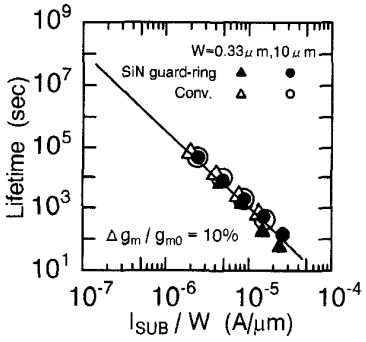


Fig.9 Lifetime plot of narrow and wide channel NMOSFETs.