DIGITAL INTEGRATED CIRCUITS

A DESIGN PERSPECTIVE

SECOND EDITION

JAN M. RABAEY
ANANTHA CHANDRAKASAN
BORIVOJE NIKOLIĆ

PRENTICE HALL ELECTRONICS AND VLSI SERIES
CHARLES G. SODINI, SERIES EDITOR

Pearson Education, Inc.
Upper Saddle River, New Jersey 07458

DOCKET ALARM
Find authenticated court documents without watermarks at docketalarm.com.

Library of Congress Cataloging-in-Publication Data on file.

Vice President and Editorial Director, ECS: *Marcia J. Horton*
Publisher: *Tom Robbins*
Editorial Assistant: *Eric Van Ostenbridge*
Vice President and Director of Production and Manufacturing, ESM: *David W. Riccardi*
Executive Managing Editor: *Vince O'Brien*
Managing Editor: *David A. George*
Production Editor: *Daniel Sandin*
Director of Creative Services: *Paul Belfanti*
Creative Director: *Carole Anson*
Art and Cover Director: *Jayne Conte*
Art Editor: *Greg Dulles*
Manufacturing Manager: *Trudy Pisciotti*
Manufacturing Buyer: *Lisa McDowell*
Marketing Manager: *Holly Stark*

About the Cover: Detail of "Wet Orange," by Joan Mitchell (American, 1925–1992). Oil on canvas, 112 × 245 in. (284.5 × 622.3 cm). Carnegie Museum of Art, Pittsburgh, PA. Gift of Kaufmann's Department Store and the National Endowment for the Arts, 74.11. Photograph by Peter Harholdt, 1995.

© 2003, 1996 by Pearson Education, Inc.
Pearson Education, Inc.
Upper Saddle River, NJ 07458

The author and publisher of this book have used their best efforts in preparing this book. These efforts include the development, research, and testing of the theories and programs to determine their effectiveness. The author and publisher shall not be liable in any event for incidental and consequential damages in connection with, or arising out of, the furnishing, performance, or use of these programs.

All rights reserved. No part of this book may be reproduced, in any form or by any means,
without permission in writing from the publisher.

Printed in the United States of America

10 9 8 7 6 5 4 3 2 1

ISBN 0-13-597444-5

General Library System
University of Wisconsin - Madison
728 State Street
Madison, WI 53706-1494
U.S.A.

Pearson Education Ltd., *London*
Pearson Education Australia Pty, Ltd., *Sydney*
Pearson Education Singapore, Pte. Ltd.
Pearson Education North Asia Ltd., *Hong Kong*
Pearson Education Canada Inc., *Toronto*
Pearson Educación de Mexico, S.A. de C.V.
Pearson Education—Japan, *Tokyo*
Pearson Education Malaysia, Pte. Ltd.
Pearson Education Inc., *Upper Saddle River, New Jersey*

DOCKET ALARM
Find authenticated court documents without watermarks at docketalarm.com.

Contents

	Preface	**vii**
Part 1	**The Fabrics**	**1**
Chapter 1	**Introduction**	**3**
1.1	A Historical Perspective	4
1.2	Issues in Digital Integrated Circuit Design	6
1.3	Quality Metrics of a Digital Design	15
1.3.1	Cost of an Integrated Circuit	16
1.3.2	Functionality and Robustness	18
1.3.3	Performance	27
1.3.4	Power and Energy Consumption	30
1.4	Summary	31
1.5	To Probe Further	31
	Reference Books	32
	References	33
Chapter 2	**The Manufacturing Process**	**35**
2.1	Introduction	36
2.2	Manufacturing CMOS Integrated Circuits	36
2.2.1	The Silicon Wafer	37
2.2.2	Photolithography	37
2.2.3	Some Recurring Process Steps	41
2.2.4	Simplified CMOS Process Flow	42
2.3	Design Rules—The Contract between Designer and Process Engineer	47
2.4	Packaging Integrated Circuits	51
2.4.1	Package Materials	52
2.4.2	Interconnect Levels	53
2.4.3	Thermal Considerations in Packaging	59
2.5	Perspective—Trends in Process Technology	61
2.5.1	Short-Term Developments	61
2.5.2	In the Longer Term	63

DOCKET ALARM
Find authenticated court documents without watermarks at docketalarm.com.

2.7 To Probe Further 64
References 64

Design Methodology Insert A **IC LAYOUT** **67**
A.1 To Probe Further 71
References 71

Chapter 3 **The Devices** **73**
3.1 Introduction 74
3.2 The Diode 74
3.2.1 A First Glance at the Diode—The Depletion Region 75
3.2.2 Static Behavior 77
3.2.3 Dynamic, or Transient, Behavior 80
3.2.4 The Actual Diode—Secondary Effects 84
3.2.5 The SPICE Diode Model 85
3.3 The MOS(FET) Transistor 87
3.3.1 A First Glance at the Device 87
3.3.2 The MOS Transistor under Static Conditions 88
3.3.3 The Actual MOS Transistor—Some Secondary Effects 114
3.3.4 SPICE Models for the MOS Transistor 117
3.4 A Word on Process Variations 120
3.5 Perspective—Technology Scaling 122
3.6 Summary 128
3.7 To Probe Further 129
References 130

Design Methodology Insert B **Circuit Simulation** **131**
References 134

Chapter 4 **The Wire** **135**
4.1 Introduction 136
4.2 A First Glance 136
4.3 Interconnect Parameters—Capacitance, Resistance, and Inductance 138
4.3.1 Capacitance 138
4.3.2 Resistance 144
4.3.3 Inductance 148
4.4 Electrical Wire Models 150
4.4.1 The Ideal Wire 151
4.4.2 The Lumped Model 151
4.4.3 The Lumped *RC* Model 152
4.4.4 The Distributed *rc* Line 156
4.4.5 The Transmission Line 159

DOCKET ALARM Find authenticated court documents without watermarks at docketalarm.com.

4.5 SPICE Wire Models 170
4.5.1 Distributed *rc* Lines in SPICE 170
4.5.2 Transmission Line Models in SPICE 170
4.5.3 Perspective: A Look into the Future 171
4.6 Summary 174
4.7 To Probe Further 174
References 174

Part 2 **A Circuit Perspective 177**

Chapter 5 **The CMOS Inverter 179**
5.1 Introduction 180
5.2 The Static CMOS Inverter—An Intuitive Perspective 180
5.3 Evaluating the Robustness of the CMOS Inverter: The Static Behavior 184
5.3.1 Switching Threshold 185
5.3.2 Noise Margins 188
5.3.3 Robustness Revisited 191
5.4 Performance of CMOS Inverter: The Dynamic Behavior 193
5.4.1 Computing the Capacitances 194
5.4.2 Propagation Delay: First-Order Analysis 199
5.4.3 Propagation Delay from a Design Perspective 203
5.5 Power, Energy, and Energy Delay 213
5.5.1 Dynamic Power Consumption 214
5.5.2 Static Consumption 223
5.5.3 Putting It All Together 225
5.5.4 Analyzing Power Consumption Using SPICE 227
5.6 Perspective: Technology Scaling and its Impact on the Inverter Metrics 229
5.7 Summary 232
5.8 To Probe Further 233
References 233

Chapter 6 **Designing Combinational Logic Gates in CMOS 235**
6.1 Introduction 236
6.2 Static CMOS Design 236
6.2.1 Complementary CMOS 237
6.2.2 Ratioed Logic 263
6.2.3 Pass-Transistor Logic 269
6.3 Dynamic CMOS Design 284
6.3.1 Dynamic Logic: Basic Principles 284

DOCKET ALARM Find authenticated court documents without watermarks at docketalarm.com.

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.