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(12) **United States Patent**
Woerlee et al.

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(54) **METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE**

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(75) Inventors: **Pierre Hermanus Woerlee; Jurriaan Schmitz; Andreas Hubertus Montree**, all of Eindhoven (NL)

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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Primary Examiner—John F. Niebling

(22) Filed: **Dec. 14, 2000**

Assistant Examiner—Walter L. Lindsay, Jr.

(30) **Foreign Application Priority Data**

(74) *Attorney, Agent, or Firm*—Aaron Waxler

Dec. 17, 1999 (EP) 99204374

(57) **ABSTRACT**

(51) **Int. Cl.**⁷ **H01L 21/336**

In a method of manufacturing a semiconductor device comprising a semiconductor body 1 which is provided at a surface 2 with a transistor comprising a gate structure 21, a patterned layer 10 is applied defining the area of the gate structure 21. Subsequently, a dielectric layer 18 is applied in such a way, that the thickness of the dielectric layer 18 next to the patterned layer 10 is substantially equally large or larger than the height of the patterned layer 10, which dielectric layer 18 is removed over part of its thickness until the patterned layer 10 is exposed. Then, the patterned layer 10 is subjected to a material removing treatment, thereby forming a recess 19 in the dielectric layer 18, and a contact window 28,29 is provided in the dielectric layer. A conductive layer 30 is applied filling the recess 19 and the contact window 28,29, which conductive layer 30 is subsequently shaped into the gate structure 21 and a contact structure 26,27 establishing an electrical contact with the surface 2 of the semiconductor body 1.

(52) **U.S. Cl.** **438/291; 438/299; 438/300; 438/301**

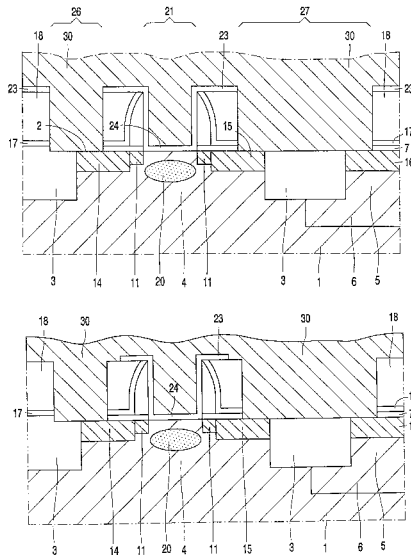
(58) **Field of Search** 438/197, 299, 438/291, 300, 305, 199, 194, 301, 585

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8 Claims, 12 Drawing Sheets



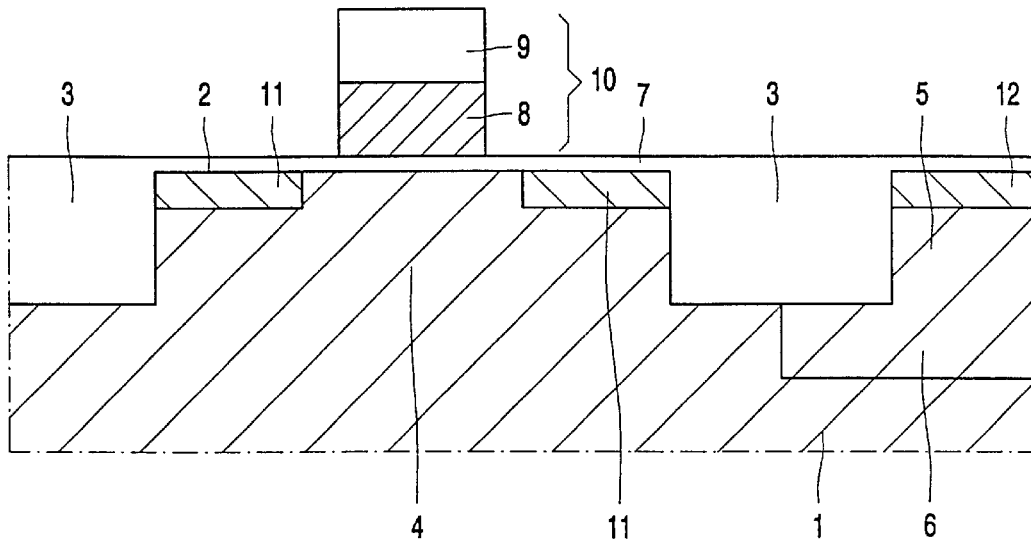


FIG. 1

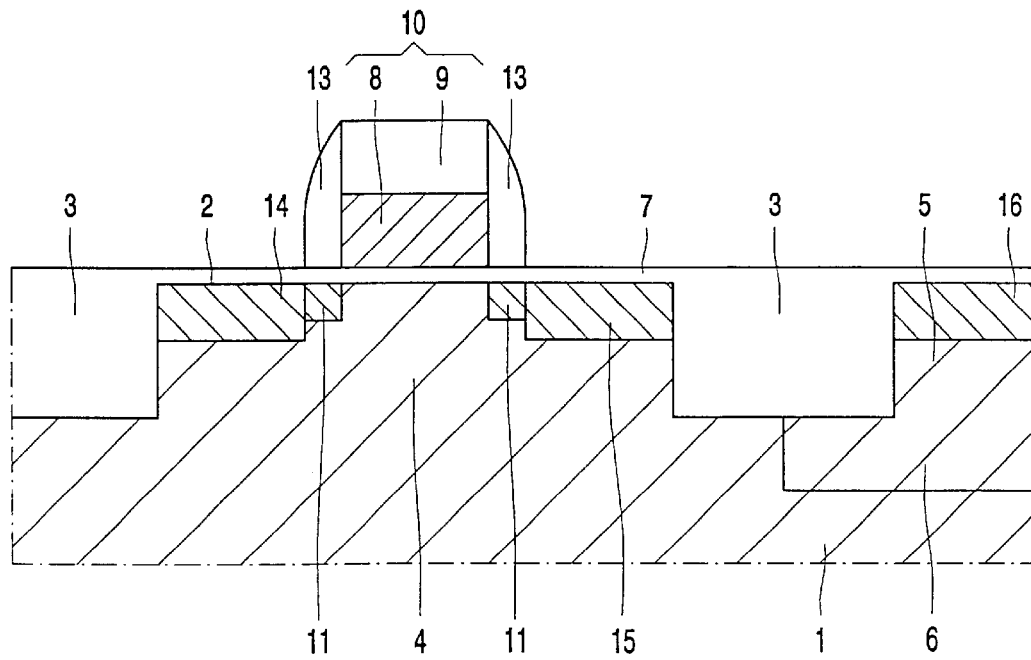


FIG. 2

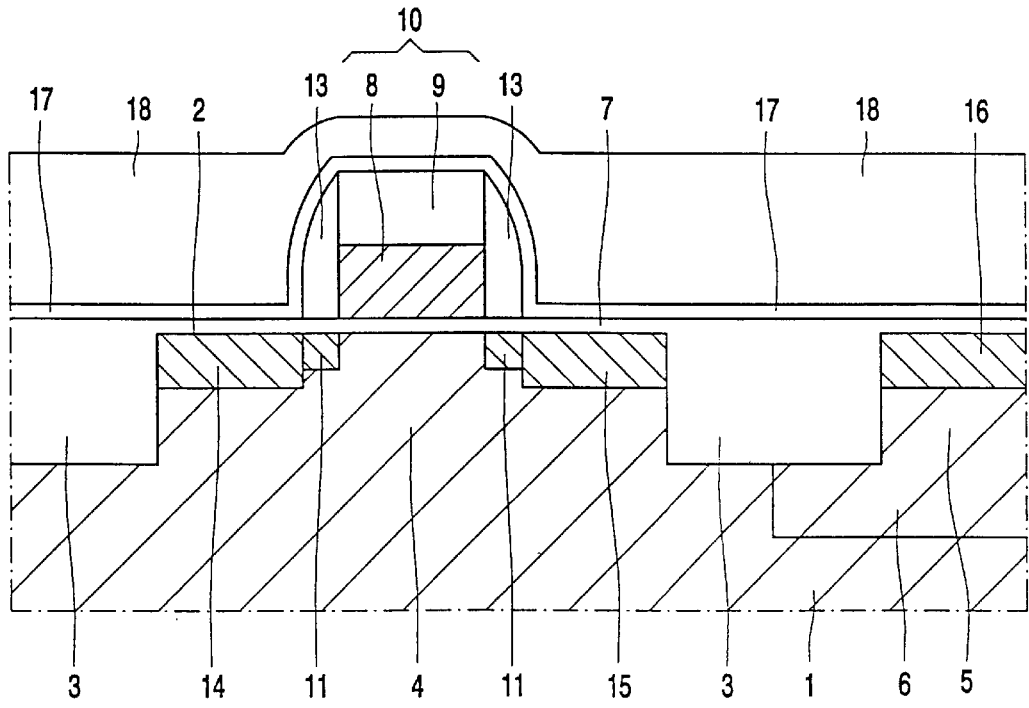


FIG. 3

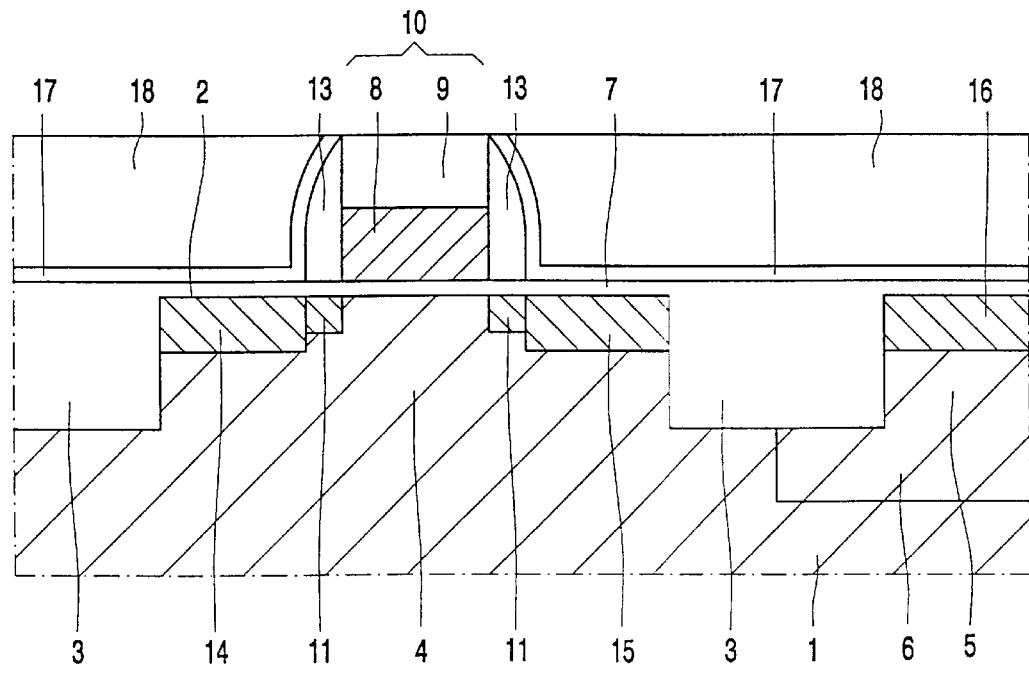


FIG. 4

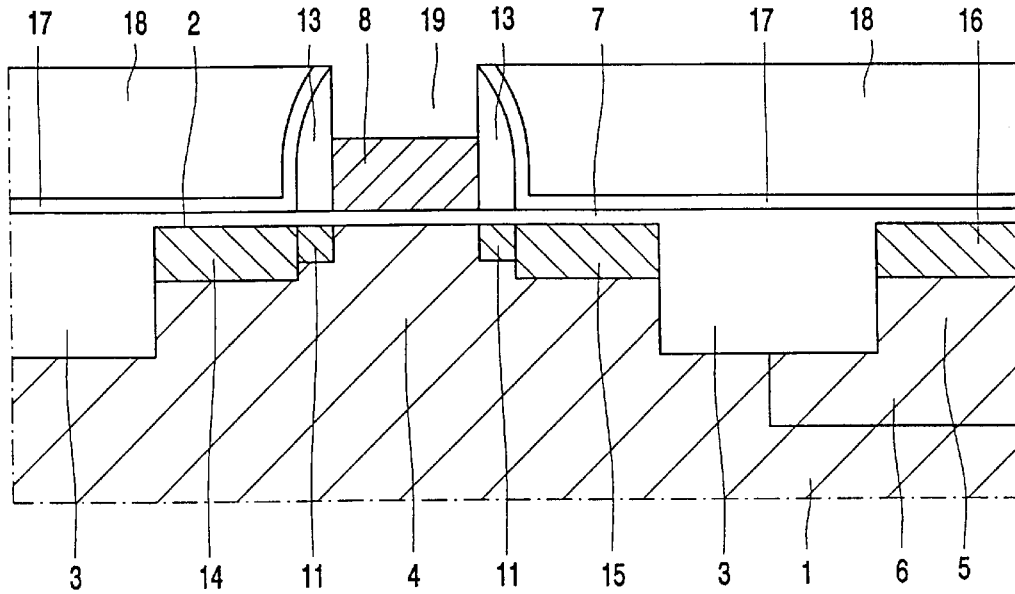


FIG. 5

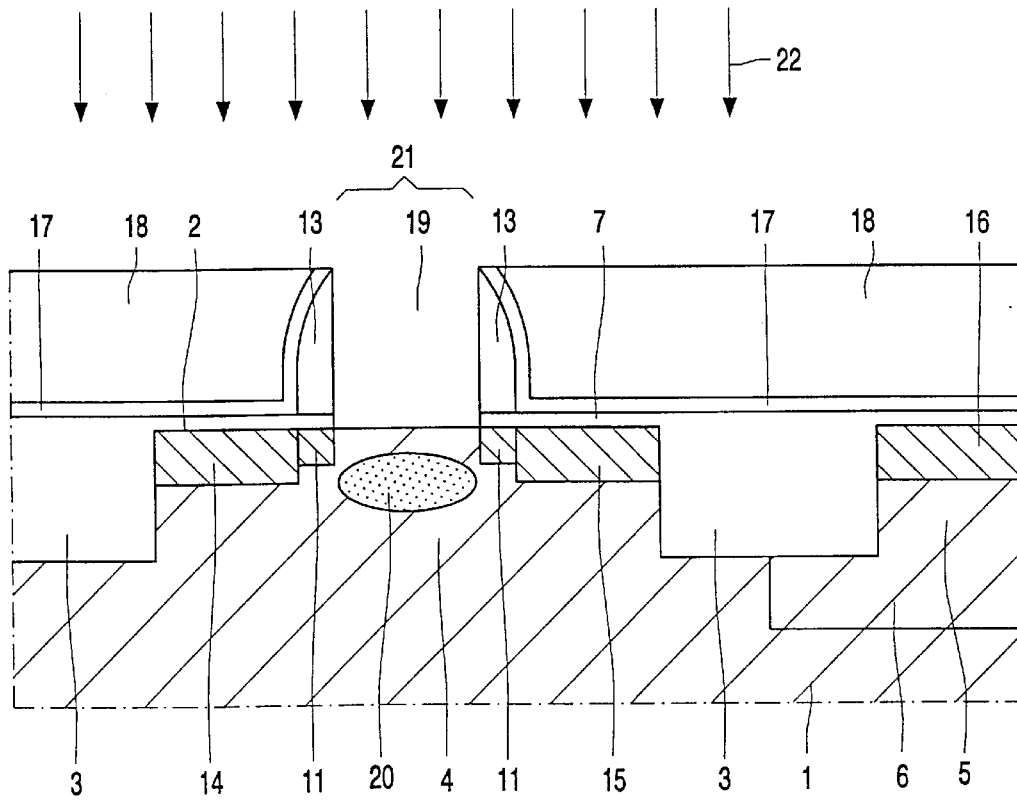


FIG. 6

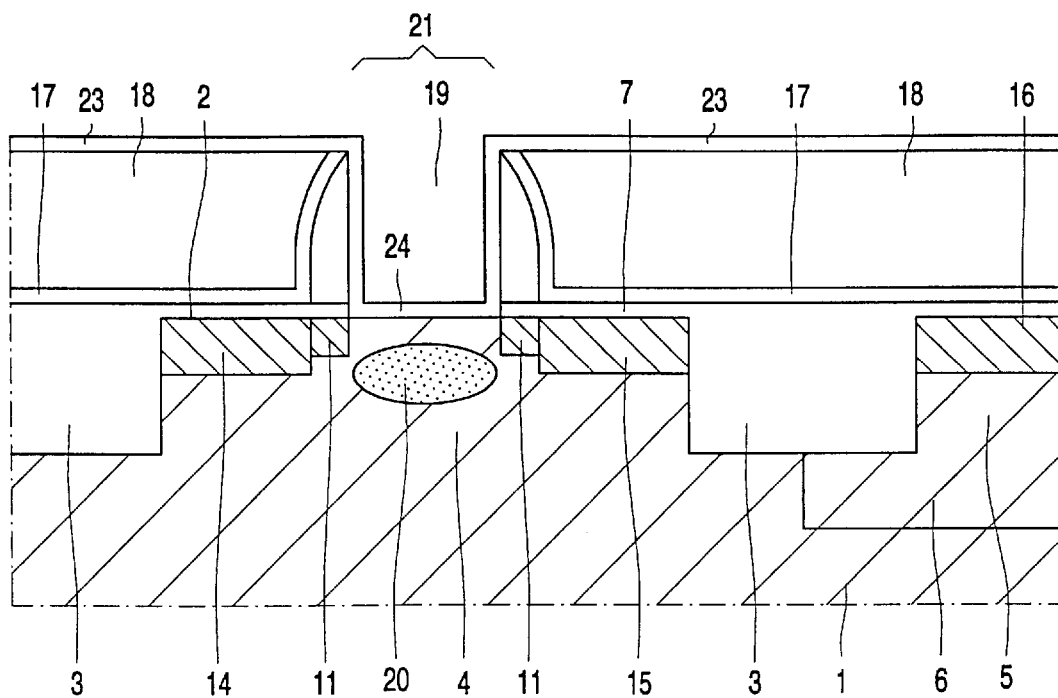


FIG. 7

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