

United States Patent [19]

Misra et al.

[54]

5,960,270 **Patent Number:** [11] **Date of Patent:** Sep. 28, 1999 [45]

METHOD FOR FORMING AN MOS	5,393,681 2/1995 Witek et al 437/40
TRANSISTOR HAVING A METALLIC GATE	5,434,093 7/1995 Chau et al
ELECTRODE THAT IS FORMED AFTER	5,447,874 9/1995 Grivna et al 437/40
THE FORMATION OF SELF-ALIGNED	5,716,861 2/1998 Moslehi
SOURCE AND DRAIN REGIONS	Primary Examiner—John F. Niebling

Assistant Examiner—Lynne A. Gurley [75] Inventors: Veena Misra; Suresh Venkatesan; Christopher C. Hobbs; Brad Smith; Jeffrey S. Cope; Earnest B. Wilson,

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Appl. No.: 08/907,990 [21]

Aug. 11, 1997 [22] Filed:

[51]

U.S. Cl. 438/197; 438/585; 438/586; 438/595; 438/596

438/586, 595, 596

[56] References Cited

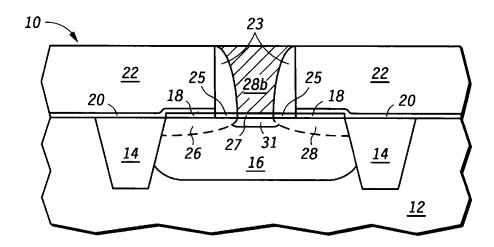
U.S. PATENT DOCUMENTS

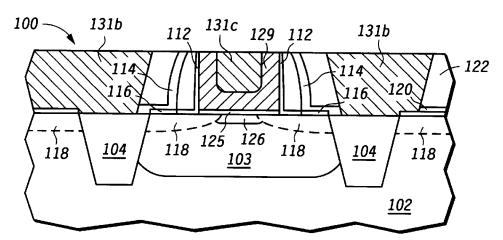
Attorney, Agent, or Firm-Keith E. Witek

ABSTRACT [57]

A method for forming a metal gate MOS transistor begins by forming source and drain electrodes (26, 28, and/or 118) within a substrate (12 or 102). These source and drain regions (26, 28, and 118) are self-aligned to a lithographically-patterned feature (24 or 108). After formation of the source and drain regions, the features (24 and 108 are processed to fill these features with a metallic gate layer (28a or 128a). This metal layer (28a or 128a) is then chemically mechanically polished (CMPed) to form a metallic plug region (28b or 128b) within the features (24 or 108). The plug region (28b or 128b) is formed in either an inlaid or dual inlaid manner wherein this metallic plug region (28b or 128b) is self-aligned to the previously formed source and drain regions and preferably functions as a metal MOS gate

43 Claims, 8 Drawing Sheets







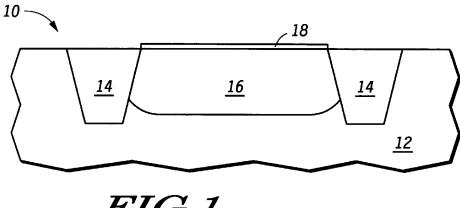
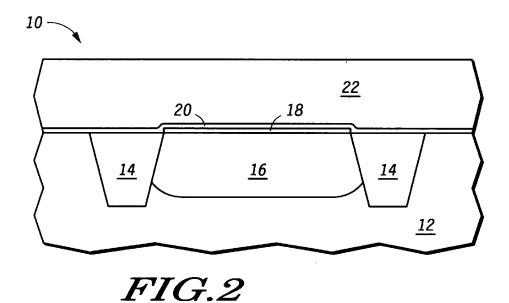


FIG.1

Sep. 28, 1999



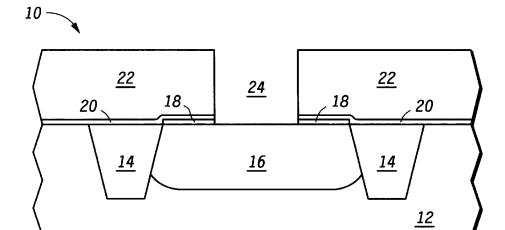


FIG.3



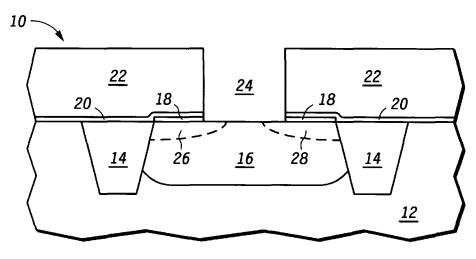


FIG.4

Sep. 28, 1999

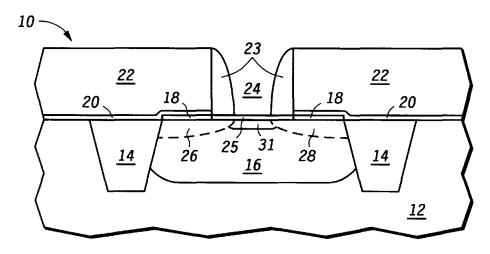


FIG.5

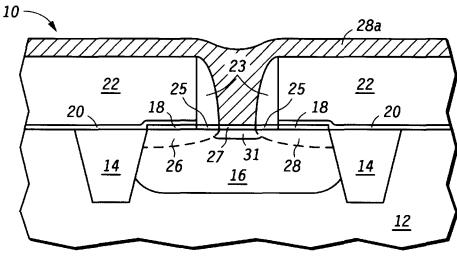
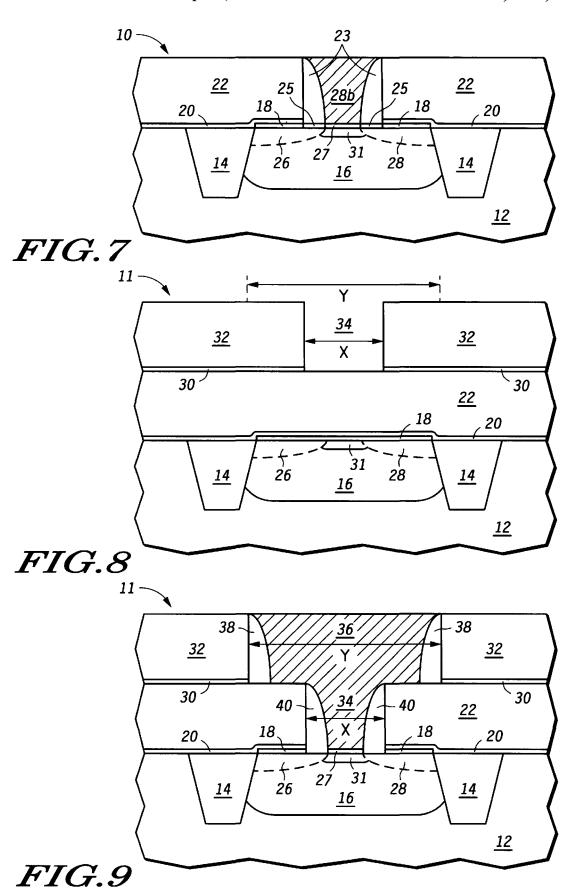
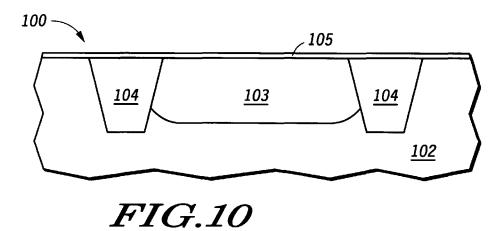
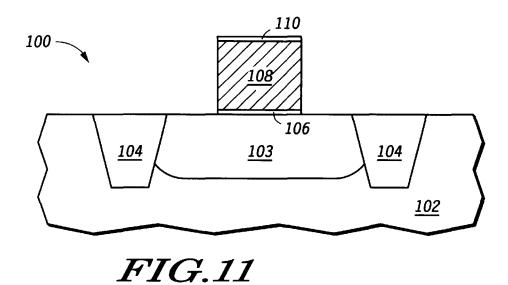


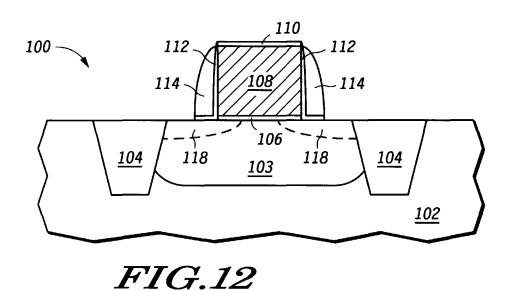
FIG.6





Sep. 28, 1999





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