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UNITED STATES PATENT AND TRADEMARK OFFICE

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.  
Petitioner

v.

GODO KAISHA IP BRIDGE 1  
Patent Owner.

Case IPR2017-01841<sup>1</sup>

**PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE**

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<sup>1</sup> Case IPR2017-01842 has been consolidated with this proceeding.

## Table of Contents

	Page
I. Introduction.....	1
II. Patent Owner’s Interpretation of “an active region made of a semiconductor substrate” is Inappropriately Narrow.....	3
III. Igarashi and Woerlee Disclose the Claimed “Active Region”.....	14
A. Patent Owner’s Imagined Inherency Argument Mischaracterizes Dr. Shanfield’s testimony .....	15
B. Igarashi Discloses a MISFET that Includes an “Active Region” .....	19
C. Patent Owner’s Attacks on Dr. Shanfield’s Testimony are Purely a Distraction .....	22
D. Patent Owner Again Incorrectly Argues that the Petition Relies on Woerlee Only for the Location of the Active Region.....	25
IV. Conclusion .....	28

## I. INTRODUCTION

Patent Owner’s Response (“Response”) confirms that the challenged claims are unpatentable. There is no dispute that Igarashi discloses the allegedly novel “protruding gate” that provided the basis for allowance.<sup>2</sup> Moreover, Patent Owner (“PO”) does not dispute that the instituted grounds expressly disclose every limitation of the challenged claims, except the “active region.” Nor does PO dispute that the references would have been obvious to combine. Instead, PO merely repeats the same arguments that it already raised in its Patent Owner’s Preliminary Response (“POPR”<sup>3</sup>) that Igarashi’s disclosure somehow lacks an “active region,” one of the most basic aspects of a semiconductor device. These arguments were correctly rejected by the Board in the Institution Decision (“DI”) and fail again here.

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<sup>2</sup> In fact, PO actually *cites* Igarashi as evidence that the purported advantages of the “protruding gate” were well-known. Ex. 2007, ¶¶45-50; *see also* IPR2017-01843 POPR, 32 (“[A] POSA would have understood that ... causing the gate electrode to protrude above the silicon nitride ... would advantageously reduce parasitic capacitance. Indeed, Igarashi teaches this explicitly.”), 30-36; IPR2017-01843 POR, 23-25; IPR2017-01843 Ex. 2208, ¶¶45-50.

<sup>3</sup> Unless otherwise specified with the “-01842” prefix, references to exhibits and papers herein are to those filed in Case IPR2017-01841.

*First*, PO again attempts to limit the “active region” to a *single* transistor, which the Board correctly rejected in the DI. DI, 8-9. PO’s interpretation of “active region” is inappropriately narrow. Moreover, PO does not even attempt to reconcile its outcome driven interpretation with its infringement contentions, which identify an alleged “active region” with *multiple* transistors, directly contradicting the arguments the PO advances before the Board. Nothing in the ’501 patent or any other evidence supports such a narrow interpretation, nor can PO’s interpretation of “active region” withstand basic technical scrutiny.

*Second*, PO again incorrectly argues that the Fifth Embodiment described in Igarashi does not teach shallow trench isolation (“STI”) regions forming an active region and that the Petition relies on Woerlee only for the *location* of the STI regions, not formation of STI regions in Igarashi’s fifth embodiment. Response, 37. The Board correctly rejected this argument and should do so again here. DI, 19-20. The Petition is clear that a POSITA would have understood that the disclosure of the features in Igarashi common to its different illustrations—including the STI regions—are applicable to the Fifth Embodiment shown in, for example, Figure 12. *See e.g.*, Petition, 22 (“A POSITA would have understood that the disclosure of the features in Igarashi common to different illustrations are applicable to the embodiment shown in Figure 12 because the same reference

numerals are used to describe common features of Igarashi's disclosure.”)

Moreover, the Petition is clear that it would have been obvious to apply Igarashi's undisputed teaching of an active region to the Fifth Embodiment. DI, 16 (quoting Petition, 32) (“Petitioner also provides several reasons why a person of ordinary skill in the art would have ‘appl[ied] Woerlee's teachings to Igarashi by forming Igarsahi's active region in the substrate and defining it with STI regions that divide the active region.”)

As set forth in the Petition and confirmed below, the challenged claims of the '501 patent would have been obvious under the cited prior art references and, accordingly, Petitioner respectfully requests that the Board cancel all challenged claims.

## **II. PATENT OWNER'S INTERPRETATION OF “AN ACTIVE REGION MADE OF A SEMICONDUCTOR SUBSTRATE” IS INAPPROPRIATELY NARROW**

PO claims that “there is no dispute that under BRI, ‘an active region made of a semiconductor substrate’ is ‘an area of the semiconductor substrate defined by an isolation region where the transistor is formed.’” Response, 26. PO then advances an unduly narrow interpretation of this proposed construction that seeks to limit the active region to having only a *single* transistor, as it sought to do through a different construction in the POPR, which the Board properly rejected. Response 74; POPR, 25, 29; DI, 9. Nothing in the '501 patent or prior art requires such a

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