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Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.
Row 1: 12/170,191, 07/09/2008, Masafumi Tsutsui, 079195-0566, 1644
Row 2: 53080, 7590, 05/10/2010, MCDERMOTT WILL & EMERY LLP, 600 13TH STREET, NW, WASHINGTON, DC 20005-3096
Row 3: EXAMINER WEISS, HOWARD
Row 4: ART UNIT 2814, PAPER NUMBER
Row 5: MAIL DATE 05/10/2010, DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

IP Bridge Exhibit 2018
TSMC v. Godo Kaisha IP Bridge 1

Attorney's Docket Number: 079195-0566

Filing Date: 7/9/2008

Continuing Data: Continuation of 10/859,219 (6/3/2004 now U.S. Patent No. 7,205,615)
which is a continuation of 11/730,988 (4/5/2007 now U.S. Patent No.
7,417,289); RCE established 3/29/2010

Claimed Foreign Priority Date: 6/16/2003 (JPX)

Applicant(s): Tsutsui et al. (Umimoto, Akamatsu)

Examiner: Howard Weiss

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/29/2010 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order

for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 15 to 21 and 23 to 34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xiang et al. (U.S. Patent No. 6,437,404) and Matsuda et al. (U.S. Patent No. 6,870,230).

Xiang et al. show most aspects of the instant invention (e.g. Figures 1 to 11) including:

- MISFET **10** with an active region in a semiconductor substrate **110** and defined between isolation regions **60,62** with said isolation regions' lower surfaces located in and in contact with the semiconductor substrate
- a gate insulating film **58** made of the material claimed (Column 3 Lines 53 to 55)
- a gate electrode **56** made of polysilicon or metal (Column 3 Lines 50 to 53)
- source/drain regions **20,22** formed on both sides of said gate electrode and comprising extended impurity regions **50,52**, main impurity regions **64,66** and silicide layers **26,28**
- a silicon nitride film **80,82** formed over the side surface but not on an upper surface of the gate electrode and over and in contact with the source drain regions
- interlevel insulating film **86** formed on said silicon nitride film and sidewalls **70,72** formed on said gate electrode's side surfaces

Xiang et al. do not show the main impurity regions being heavily doped and the extended impurity regions being lightly doped and in contact with the main impurity regions, the gate insulating film formed only under a lower surface of the gate electrode, a thin film interposed between the silicon nitride film and the source drain regions, a contact plug that passes through the interlevel insulating film and the silicon nitride film in contact with the source/drain regions.

Matsuda et al. teach (e.g. Figures 2, 3 and 9) to form main impurity regions **12** being heavily doped and the extended impurity regions **7** being lightly doped and in contact with the main impurity regions, to form a gate insulating film **3** only under a lower surface of the gate electrode **6a**, to form a thin film **8a** between a silicon nitride film **9a** and the source/drain regions **7,12** and to provide a contact plug **16a** to pass through a interlevel insulating film **13** and the silicon nitride film contacting the source/drain regions to suppress the variation in the width of the sidewalls (Column 11 Lines 49 to 51). It would have been obvious to a person of ordinary skill in the art at the time of invention to form a gate insulating film only under a lower surface of the gate electrode, to form a thin film between a silicon nitride film and the source/drain regions and to provide a contact plug to pass through a interlevel insulating film and the silicon nitride film to contact the source/drain regions as taught by Matsuda et al. in the device of Xiang et al. to suppress the variation in the width of the sidewalls.

In reference to the claim language pertaining to the ability of the silicon nitride film to generate stress in the channel region substantially parallel to the gate length direction, the claiming of a new use, new function, or unknown property which is inherently present in the prior art does not necessarily make the claim patentable. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and *In re Swinehart*, 439 F. 2d 210, 169 USPQ 226 (CCPA 1971); please see MPEP § 2112. Since Xiang et al. show all the features of the claimed invention, the ability of the silicon nitride film to generate stress in the channel region substantially parallel to the gate length direction is an inherent property of Xiang et al. and Matsuda et al.'s invention.

4. Claims 22 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xiang et al. and Matsuda et al., as applied to Claim 15 above, and in further view of Tatsuta (U.S. Patent No. 5,023,676).

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