

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Cases IPR2017-01841 and IPR2017-01842
Patent 7,893,501 B2

Before JUSTIN T. ARBES, MICHAEL J. FITZPATRICK, and
JENNIFER MEYER CHAGNON, *Administrative Patent Judges*.

CHAGNON, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Taiwan Semiconductor Manufacturing Company, Ltd. (“Petitioner”) filed two Petitions for *inter partes* review of, collectively, claims 1, 4–7, 9–19, 21, and 23–25 (“the challenged claims”) of U.S. Patent No. 7,893,501 B2 (Ex. 1001,¹ “the ’501 patent”). Petitioner relies on the Declarations of Stanley R. Shanfield, Ph.D. (Ex. 1002; -1842 Ex. 1102) to support its positions. Godo Kaisha IP Bridge 1 (“Patent Owner”) filed a Preliminary Response in each proceeding, as listed in the following chart.

Case Number	Challenged Claims	Petition	Preliminary Response
IPR2017-01841	1, 4, 7, 9–11, 14, 16–18, 23–25	Paper 2 (“Pet.”)	Paper 6 (“Prelim. Resp.”)
IPR2017-01842	5, 6, 12, 13, 15, 19, 21	Paper 2 (“-1842 Pet.”)	Paper 6 (“-1842 Prelim. Resp.”)

We have authority to determine whether to institute *inter partes* review. *See* 35 U.S.C. § 314(b); 37 C.F.R. § 42.4(a). Upon consideration of the Petitions and the Preliminary Responses, and for the reasons explained below, we determine that the information presented shows a reasonable likelihood that Petitioner would prevail with respect to all of the challenged claims. *See* 35 U.S.C. § 314(a). Accordingly, we institute trial as to the challenged claims, based on the grounds set forth in the Petitions. We also

¹ Unless otherwise specified with the “-1842” prefix, references to exhibits and papers herein are to those filed in Case IPR2017-01841.

IPR2017-01841, IPR2017-01842
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exercise our authority under 35 U.S.C. § 315(d) to consolidate the two proceedings and conduct the proceedings as one trial.²

The following findings of fact and conclusions of law are not final, but are made for the sole purpose of determining whether Petitioner meets the threshold for initiating review. Any final decision shall be based on the full trial record, including any response timely filed by Patent Owner. Any arguments not raised by Patent Owner in a timely-filed response shall be deemed waived, even if they were presented in the Preliminary Response.

A. Related Proceedings

The parties indicate that the '501 patent is the subject of the following ongoing district court proceeding: *Godo Kaisha IP Bridge 1 v. Xilinx, Inc.*, No. 2-17-cv-00100 (E.D. Tex.). Pet. 2; Paper 4, 1. Petitioner has filed two additional petitions challenging claims of the '501 patent—IPR2017-01843 and IPR2017-01844. Pet. 2; Paper 4, 1.

B. The '501 Patent

The '501 patent relates to a semiconductor device including a MISFET (metal-insulator-semiconductor field-effect transistor³) and a method of manufacturing the same. Ex. 1001, 1:16–19. In particular, the '501 patent teaches “a first-type internal stress film formed of a silicon oxide film over source/drain regions of an nMISFET and a second-type

² As indicated in the Order, all further filings in the consolidated proceeding shall be made in Case IPR2017-01841. For clarity in future filings, the parties are instructed to cite to papers and exhibits filed only in Case IPR2017-01842 using the same -1842 prefix style used herein.

³ Ex. 1002 ¶ 34.

internal stress film formed of a TEOS [(tetraethylorthosilicate⁴)] film over source/drain regions of a pMISFET.” *Id.* at [57]. According to the ’501 patent, these internal stress films generate tensile or compressive stresses that, respectively, allow the mobility of electrons or holes to increase.⁵ *Id.*

Figure 1 of the ’501 patent is reproduced below.

FIG. 1

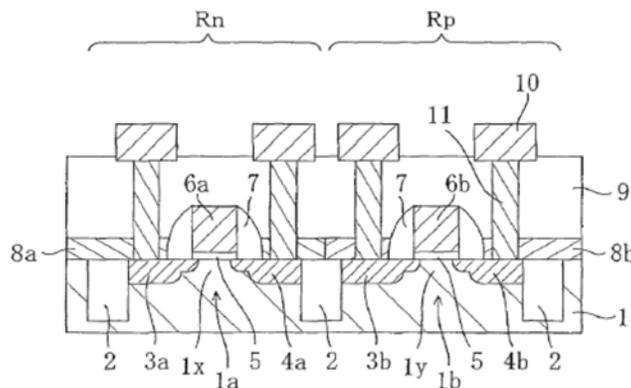


Figure 1, above, is a cross-sectional view of a semiconductor device of an embodiment of the ’501 patent. *Id.* at 2:47–49. The semiconductor device of Figure 1 includes semiconductor substrate 1, which is divided into active regions 1a and 1b by isolation region 2; channel regions 1x, 1y; nMISFET formation region Rn and pMISFET formation region Rp; source regions 3a, 3b and drain regions 4a, 4b; gate insulating film 5; gate electrodes 6a, 6b; sidewalls 7; first-type internal stress film 8a (e.g., silicon nitride film);

⁴ See Ex. 1005 (U.S. Patent No. 5,960,270), 5:40; Ex. 1016 (U.S. Patent No. 6,509,234 B1), 6:67.

⁵ We note that the challenged claims do not recite these stress limitations, which are present only in dependent claims 2, 3, and 20. See Pet. 15 n.2.

second-type internal stress film 8b (e.g., TEOS film); interlevel insulating film 9; lead electrode 10; and contact 11. *Id.* at 3:19–64.

C. Illustrative Claim

Of the challenged claims, claim 1 is independent and claims 4–7, 9–19, 21, and 23–25 depend, directly or indirectly, therefrom. Independent claim 1 of the '501 patent is reproduced below, and is illustrative of the challenged claims.

1. A semiconductor device, comprising a MISFET,
wherein

the MISFIT includes:

an active region made of a semiconductor substrate;

a gate insulating film formed on the active region;

a gate electrode formed on the gate insulating film;

source/drain regions formed in regions of the active region located on both sides of the gate electrode; and

a silicon nitride film formed over from side surfaces of the gate electrode to upper surfaces of the source/drain regions,
wherein:

the silicon nitride film is not formed on an upper surface of the gate electrode, and

the gate electrode protrudes upward from a surface level of parts of the silicon nitride film located at both side surfaces of the gate electrode.

Ex. 1001, 15:42–57.

D. The Applied References

Petitioner relies on the following references in the asserted grounds.

Pet. 4–5; -01842 Pet. 4.

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