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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.
Petitioner

v.

GODO KAISHA IP BRIDGE 1
Patent Owner.

Case IPR2017-01841

PETITIONER'S UPDATED EXHIBIT LIST

Pursuant to the Board's Order dated December 29, 2017, Petitioner hereby submits the December 19, 2017 Conference Call Transcript as Exhibit 1020 and the infringement contentions dated February 1, 2017 for U.S. Patent 7,893,501 from *Godo Kaisha IP Bridge 1 v. Xilinx, Inc.*, Case No. 2:17-cv-00100 (E.D. Tex.) as Exhibit 1021. Petitioner also hereby submits an updated exhibit list.

Respectfully Submitted,

/ Michael Smith/

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CERTIFICATE OF SERVICE

I hereby certify that, on January 9, 2018, I caused a true and correct copy of the foregoing materials:

- Petitioner's Updated Exhibit List
- Petitioner's List of Exhibits
- Exhibits 1020 and 1021

to be served via email on the following counsel of record as listed in Patent Owner's Mandatory Notices:

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PETITIONER'S LIST OF EXHIBITS FOR IPR2017-01841

Exhibit	Description
1001	U.S. Patent No. 7,893,501
1002	Declaration of Stanley R. Shanfield, Ph.D. Regarding U.S. Patent No. 7,893,501, Claims 1, 4, 7, 9-11, 14, 16-18, and 23-25 ("Shanfield Decl.")
1003	Applicant's Amendment and Response dated August 6, 2010
1004	U.S. Patent Publication No. 2002/0145156 to Igarashi et al. ("Igarashi")
1005	U.S. Patent No. 5,960,270 to Misra et al. ("Misra")
1006	U.S. Patent No. 6,406,963 to Woerlee et al. ("Woerlee")
1007	Notice of Allowance dated October 15, 2010
1008	J. Plummer et al., *Silicon VLSI Technology: Fundamentals, Practice and Modeling*, (1st ed. 2000)
1009	W.O. Publication No. 2002/043151 with certified English translation ("Shimizu")
1010	J. Rabaey et al., *Digital Integrated Circuits,* at 40-44 (2d ed. 2003) ("Rabaey")
1011	S. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, (2d. ed. 2003) ("Kang")
1012	K. Maex, *Simply irresistible silicides*, Physics World, at 35-39 (Nov. 1995)
1013	U.S. Patent No. 6,806,584
1014	B. Deal, *Current Concepts in Passivation and Encapsulation of*

Exhibit	Description
	Semiconductor Devices, 10th Electrical Insulation Conf., at 63-68 (Sept. 1971)
1015	T. Ogura et al., *A Shallow Trench Isolation with SiN Guard-Ring for Sub-Quarter Micron CMOS Technologies*, Symposium on VLSI Technology Digest of Technical Papers, at 210-211 (1998)
1016	U.S. Patent No. 6,509,234
1017	U.S. Patent No. 5,726,479
1018	U.S. Patent No. 6,512,266
1019	U.S. Patent No. 6,350,661 ("Lim")
1020	December 19, 2017 Conference Call Transcript
1021	Infringement contentions dated February 1, 2017 for U.S. Patent 7,893,501 from *Godo Kaisha IP Bridge 1 v. Xilinx, Inc.*, Case No. Case No. 2:17-cv-00100 (E.D. Tex.)