

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

UBISOFT, INC. AND SQUARE ENIX, INC.,
Petitioners,

v.

UNILOC USA, INC. AND UNILOC LUXEMBOURG S.A.,
Patent Owners.

Case No. IPR2017-01814
U.S. Patent No. 6,324,578

DECLARATION OF DR. VIJAY K. MADISETTI, PH.D.

I, Vijay K. Madiseti, hereby declare the following:

I. BACKGROUND AND EDUCATION

1. My name is Vijay Madiseti, and I am a Professor of Electrical and Computer Engineering at Georgia Institute of Technology (“Georgia Tech”) in Atlanta, GA.

2. I received a Bachelor of Technology in electronics and Electrical Communications Engineering from the Indian Institute of Technology (IIT) in 1984. I received my Ph.D. in Electrical Engineering and Computer Sciences (EECS) from the University of California, Berkeley in 1989. I am currently a tenured full Professor at Georgia Institute of Technology, and I have been on the faculty of Georgia Institute of Technology since 1989. I have authored or co-authored over 100 reference articles in the area of electrical engineering. I have also authored, co-authored, or edited several books in the areas of electrical engineering, signal processing, image and video processing, computer engineering, and embedded systems, including *Modeling, Analysis, Simulation of Computer and Telecommunications Systems* (1994), *VLSI Digital Signal Processors* (1995) and *The Digital Signal Processing Handbook* (First & Second Editions) (1998, 2012), and *VHDL: Electronics Systems Design Methodologies* (2000). Although I discuss my expert qualifications in more detail below, I also attach as [**Appendix A**] a recent and complete curriculum vitae, which details my educational and professional background and includes a listing of most of my publications.

3. I have been active in the area of computer and information security and protection in the networked environment since late 1980s, starting with my work on “GAFFES: A Design of A Globally Distributed File System” (EECS Technical Report, UCB/CSD-87-361, June 1987) which described early work on security, authentication and replication in the network context. I have also published papers in the area of coding theory for secure storage, communications and noise immunity in the context of storage networks (See, e.g., “Constrained Multitrack RLL Codes for the Storage Channel”, IEEE Transactions on Magnetics, Vol. 31, Issue 3, 1995). I have also developed algorithms for detection of erroneous (or false) information that can be introduced and propagated into computer networks, and developed a preemptive algorithm called WOLF that has been efficient in limiting the propagation by rolling back the effects of incorrect messages within a network. (See WOLF: A Rollback Algorithm for Optimistic Distributed Simulation Systems, 1988).

4. I have been involved in research and technology in the area of signal processing, event-driven programming, embedded systems, and distributed computer and information systems since the late 1980s, and my work in this area has focused on secure and efficient distribution of information over networks, synchronization of updates across a distributed network, and multiprocessing systems and tools.

5. In 1987, at UC Berkeley, I worked on implementing a globally distributed file system, called GAFFES, to facilitate information sharing in a global network of workstations. GAFFES provided four services to handle naming, replication and caching, security and authentication, and file access primitives. GAFFES outlined features of access in terms of users and their roles, and in terms of beliefs and policies. Every file in GAFFES has at least one role, and the owner of a role determines the roles that may use that role to operations on software files.

6. In the past twenty years, I have also authored several peer-reviewed papers in the areas of computer software and design, and these include:

- V. Madiseti, et al, "Synchronization mechanisms for distributed event-driven computation", ACM Transactions on Modeling and Computer Simulation, Vol 2, No. 1, January 1992
- V. Madiseti, et al, "The Georgia tech Digital Signal Multiprocessor", IEEE Transactions on Signal Processing, Vol 41, No. 7, July 1993
- V. Madiseti et al, "Rapid Prototyping on the Georgia Tech Digital Signal Multiprocessor", IEEE Transactions on Signal Processing, Vol 42, March 1994.
- V. Madiseti et al, "Computer Simulation of Application-Specific Signal Processing Systems", International Journal in Computer Simulation, Vol. 4, No. 4, Nov 1994
- V. Madiseti, "Reengineering legacy embedded systems", IEEE Design & Test of Computers, Vol 16, Vol 2, 1999
- V. Madiseti et al, "Virtual Prototyping of Embedded Microcontroller-based DSP Systems", IEEE Micro, Vol 15, Issue 5, 1995
- V. Madiseti, et al, "Incorporating Cost Modeling in Embedded-System Design", IEEE Design & Test of Computers, Vol 14, Issue 3, 1997
- V. Madiseti, et al, "Conceptual Prototyping of Scalable Embedded DSP Systems", IEEE Design & Test of Computers, Vol 13, Issue 3, 1996.

- V. Madiseti, “Electronic System, Platform & Package Codesign,” IEEE Design & Test of Computers, Vol 23, Issue 3, June 2006.
- V. Madiseti, et al, “A Dynamic Resource Management and Scheduling Environment for Embedded Multimedia and Communications Platforms”, IEEE Embedded Systems Letters, Vol 3, Issue 1, 2011.

7. I have over 100 peer-reviewed publications issued from the early 1980s to the present on topics related to computer engineering, signal processing, event-driven programming, and digital system design.

8. I am a Fellow of the Institute of Electrical and Electronics Engineering (“IEEE”), which signifies the highest professional standing in my research and educational community.

9. In sum, I have over 25 years of experience in research and development in the areas of signal processing, event-driven programming, computer engineering and electrical engineering as a professor, researcher and consultant.

10. I have been retained by Petitioners and am submitting this declaration to offer my independent expert opinion concerning certain issues raised in the Petition for *Inter Partes* Review (“Petition”). I am being compensated at the rate of \$450 per hour, as well as being reimbursed for fees and expenses reasonably incurred with this engagement. My compensation is not based on the substance of the opinions rendered here. As part of my work in connection with this matter, I have studied U.S. Patent No. 6,324,578 (“the ‘578 patent”), including the respective written descriptions, figures and claims, in addition to the ‘578 patent prosecution

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