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Lam

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[54] **MEMORY SHARING ARCHITECTURE FOR A DECODING IN A COMPUTER SYSTEM**

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[51] **Int. Cl.**[6] **G06F 12/10**

[52] **U.S. Cl.** **711/206**

[58] **Field of Search** 711/202, 203, 711/206, 207; 395/846; 710/22

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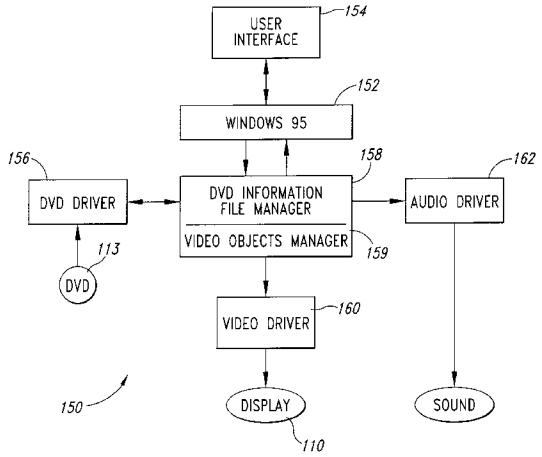
[57] **ABSTRACT**

A method and apparatus employing a memory management system that can be used with applications requiring a large contiguous block of memory, such as video decompression techniques (e.g., MPEG 2 decoding). The system operates with a computer and the computer's operating system to request and employ approximately 500 4-kilobyte pages in two or more noncontiguous blocks of the main memory to construct a contiguous 2-megabyte block of memory. The system can employ, on a single chip, a direct memory access engine, a microcontroller, a small block of optional memory, and a video decoder circuit. The microcontroller retains the blocks of multiple pages of the main memory, and the page descriptors of these blocks, so as to lock down these blocks of memory and prohibit the operating system or other applications from using them. The microcontroller requests the page descriptors for each of the blocks, and programs a lookup table or memory mapping system in the on-chip memory to form a contiguous block of memory. As a result, the video decoder circuit can perform operations on a 2-megabyte contiguous block of memory, where the microcontroller employs the lookup table to translate each 2-megabyte contiguous address requested by the video decoder circuit to its appropriate page in the main memory. As soon as the video decoding operations are complete, the microcontroller releases the blocks of multiple pages of memory back for use by the computer.

40 Claims, 3 Drawing Sheets



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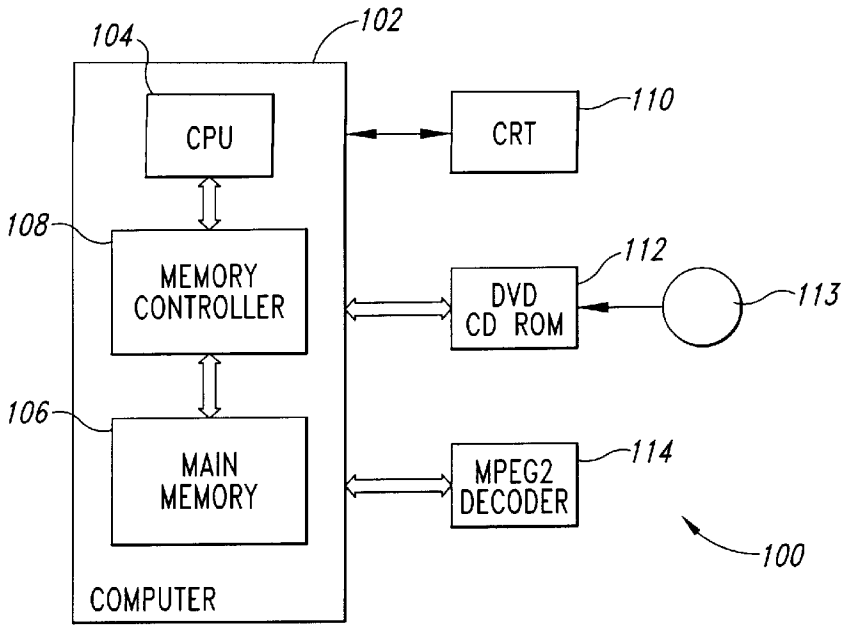

Fig. 1

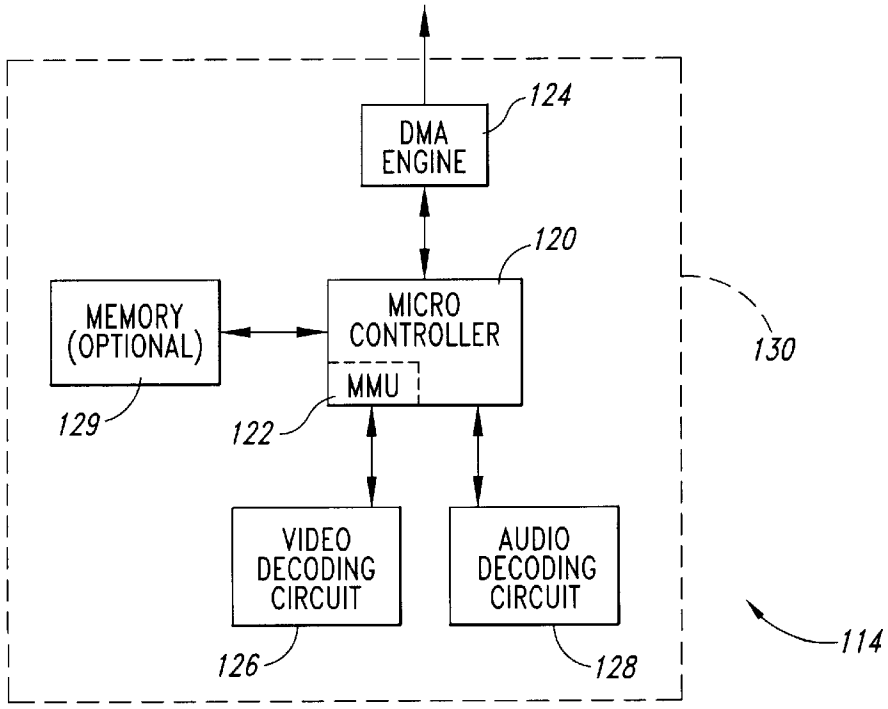

Fig. 2

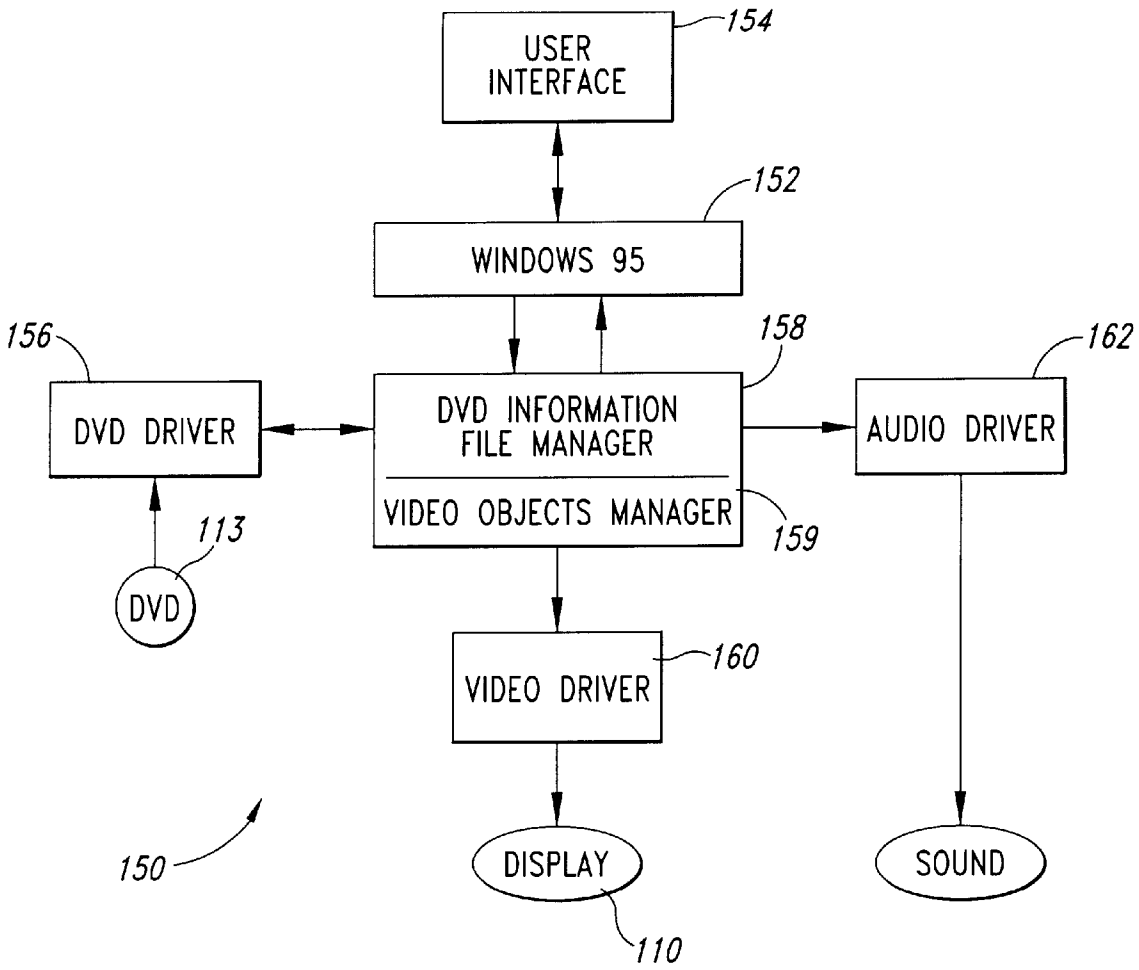

Fig. 3

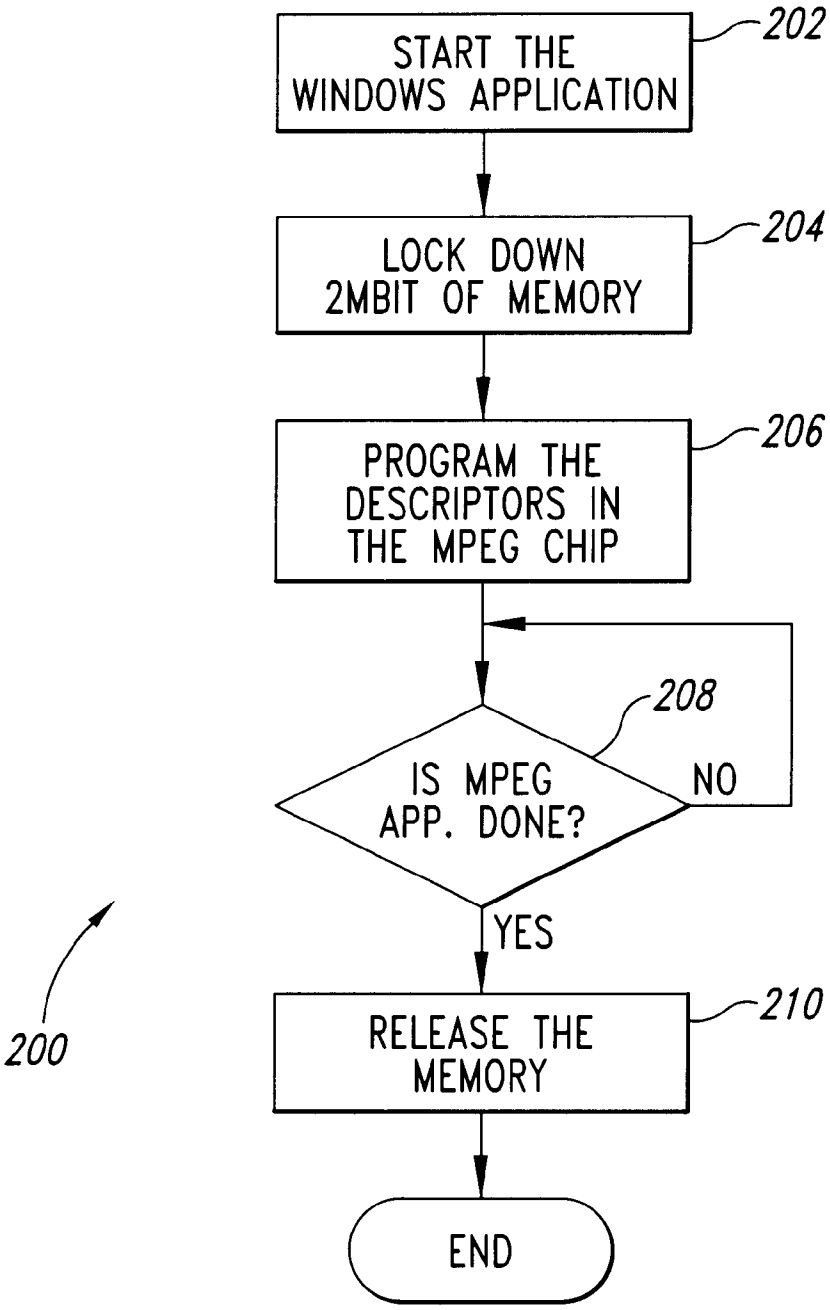

Fig. 4

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