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Title: MPEG Decoder System And Method Having A Unified Memory For Transport Decode And System Controller Functions

Mail Stop *Inter Partes* Review Commission for Patents P.O. Box 1450 Alexandria, VA 22313-1450

DECLARATION OF DR. CLAUDIO T. SILVA UNDER 37 C.F.R. § 1.68 IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 5,870,087

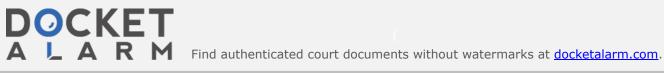


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2	2. Claim Elements 1.1 and 16.1: "a channel receiver for receiving and [MPEG encoded/encoded video] stream"	.30



3. Claim Elements 1.2 and 16.2: "transport logic coupled to the channel receiver which demultiplexes one or more multimedia data streams from the encoded stream"	
4. Claim Elements 1.3 and 16.3: "a system controller coupled to the transpologic which controls operations within the [MPEG/video] decoder system"	
5. Claim Elements 1.4 and 16.4: "[an MPEG/a video] decoder coupled to receive one or more multimedia data streams output from the transport logic, wherein the [MPEG/video] decoder operates to perform [MPEG/video] decoding on the multimedia data streams"	
6. Claim Elements 1.5 and 16.5: "a memory coupled to the [MPEG/video] decoder, wherein the memory is used by the [MPEG/video] decoder during [MPEG/video] decoding operations"	39
7. Claim Elements 1.6 and 16.6: "wherein the memory stores code and data useable by the system controller which enables the system controller to perform control functions within the [MPEG/video] decoder system".	)
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11. Claim Elements 1.10 and 16.10: "wherein the system controller is operable to access the memory to retrieve code and data during system control functions"	
B. Fujii Anticipates Dependent Claim 7.	57
1. Claim Element 7.1: "wherein said memory includes a plurality of memor portions, wherein said memory includes a video frame portion for storing video frames"	у 57



2. Claim Element 7.2: "a system controller portion for storing code and data executable by the system controller"
3. Claim Element 7.3: "and a transport buffer portion for storing data used by the transport logic"
C. The Combination of Fujii and Bheda Renders Obvious Claims 2-3 and 17
1. Claim Elements 2.1 and 17.1: "wherein the [MPEG/video] decoder includes a memory controller coupled to the memory"
2. Claim Elements 2.2 and 17.2: "wherein the transport logic is coupled to the memory controller and is operable to access the memory through the memory controller"
3. Claim Elements 2.3 and 17.3: "wherein the system controller is coupled to the memory controller and is operable to access the memory through the memory controller"
4. Claim 3: "The MPEG decoder system of claim 2, wherein the memory controller is operable to store compressed data in the memory to reduce memory storage requirements."
D. The Combination and Fujii and Lam Renders Obvious Dependent Claim 5
E. The Combination of Maturi and Yao Renders Obvious Independent Claims 1 and 16
1. Claims 1 and 16 Preambles: "[An MPEG/ A video] decoder system which includes a single memory for use by transport, decode and system controller functions"
2. Claim Elements 1.1 and 16.1: "a channel receiver for receiving and [MPEG encoded/encoded video] stream"
3. Claim Elements 1.2 and 16.2: "transport logic coupled to the channel receiver which demultiplexes one or more multimedia data streams from the encoded stream"



4.	Claim Elements 1.3 and 16.3: "a system controller coupled to the transport logic which controls operations within the [MPEG/video] decoder system"
5.	Claim Elements 1.4 and 16.4: "[an MPEG/a video] decoder coupled to receive one or more multimedia data streams output from the transport logic, wherein the [MPEG/video] decoder operates to perform [MPEG/video] decoding on the multimedia data streams"
6.	Claim Elements 1.5 and 16.5: "a memory coupled to the [MPEG/video] decoder, wherein the memory is used by the [MPEG/video] decoder during [MPEG/video] decoding operations"
7.	Claim Elements 1.6 and 16.6: "wherein the memory stores code and data useable by the system controller which enables the system controller to perform control functions within the [MPEG/video] decoder system"
8.	Claim Elements 1.7 and 16.7: "wherein the memory is used by the transport logic for demultiplexing operations"
9.	Claim Elements 1.8 and 16.8: "wherein the [MPEG/video] decoder is operable to access the memory during [MPEG/video] decoding operations"
10.	Claim Elements 1.9 and 16.9: "wherein the transport logic is operable to access the memory to store and retrieve data during demultiplexing operations"
11.	Claim Elements 1.10 and 16.10: "wherein the system controller is operable to access the memory to retrieve code and data during system control functions"
	he Combination of Maturi and Yao Renders Obvious Dependent laim 795
1.	Claim Element 7.1: "wherein said memory includes a plurality of memory portions, wherein said memory includes a video frame portion for storing video frames"
2.	Claim Element 7.2: "a system controller portion for storing code and data executable by the system controller"



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