United States Patent [19]

Schoenborn

[56]

[54] ANISOTROPIC POLYSILICON ETCHING PROCESS

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- [73] Assignee: LSI Logic Corporation, Milpitas, Calif.
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- [22] Filed: Dec. 20, 1990
- [51] Int. Cl.⁵ H01L 21/00
- [58] Field of Search 656/657, 662, 643, 646

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- [45] Date of Patent: Sep. 7, 1993

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Primary Examiner-Thi Dang

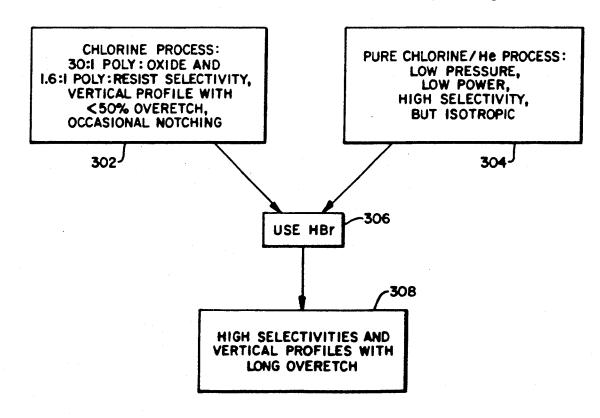
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Attorney, Agent, or Firm—Gerald E. Linden; Michael D. Rostoker

ABSTRACT

An anisotropic polysilicon etching process in $Cl_2/HBr/He$ is disclosed. The use of HBr allows etching to occur under high poly:oxide selectivity conditions (e.g., above 40:1) that would otherwise produce lateral etching of the poly under the photoresist mask (isotropy). The selectivity of poly:resist is also increased (e.g., above 4:1). Poly sidewall passivation is enhanced without relying on resist redeposition. Gate oxide loss is also minimized, and anisotropy is realized with increased overetch (e.g., 60%). Exemplary process settings are: 1) 250 mTorr, 190 Watts, 0.5 cm gap, 100 sccm Cl_2 , 50 sccm HBr and 40 sccm He; and 2) 270 mTorr, 200 Watts, 0.5 cm gap, 80 sccm Cl_2 , 55 sccm HBr and 45 sccm He.

19 Claims, 16 Drawing Sheets



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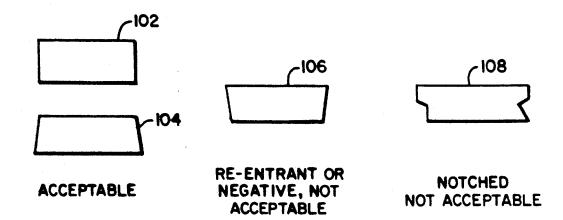


FIG. IA

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FIG. 10

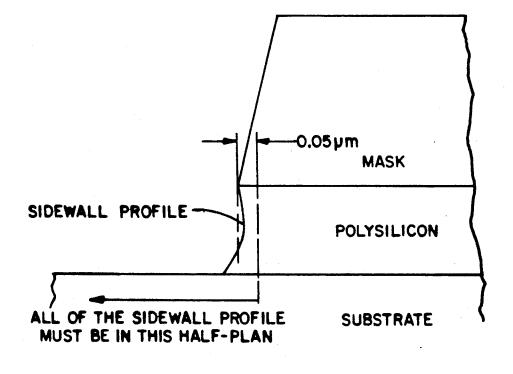


FIG. ID

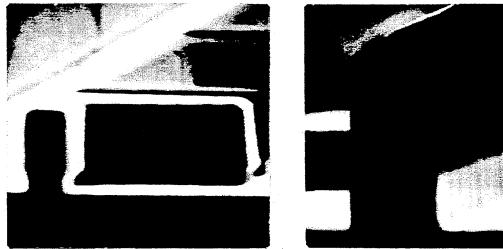
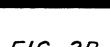
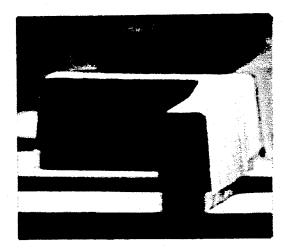


FIG. 2A



<u>FIG. 2B</u>



<u>FIG. 4</u>

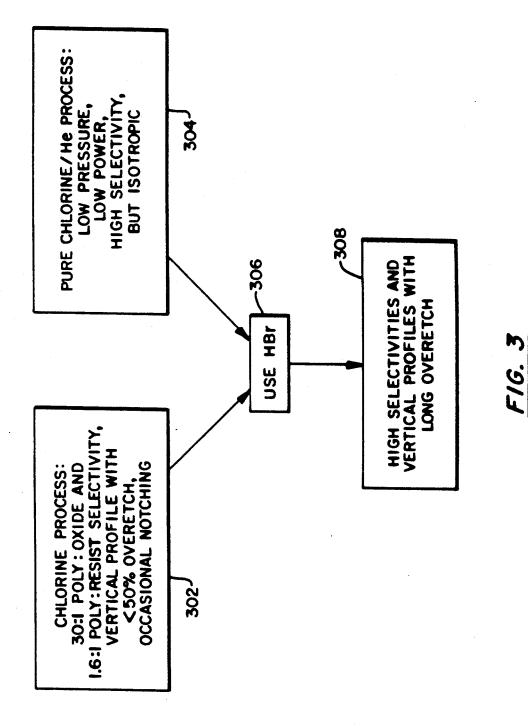
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<u>FIG. 5</u>

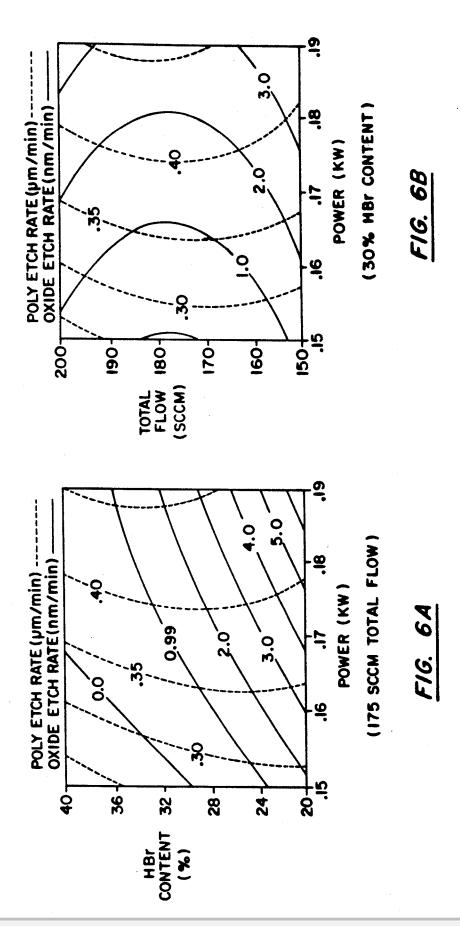
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