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MICRO-REACTION ENGINEERING
APPLICATIONS OF REACTION ENGINEERING TO PROCESSING OF ELECTRONIC AND PHOTONIC MATERIALS

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ABSTRACT

Processing of electronic materials for electronic and opto-electronic devices combines a facinating variety of physical transport processes and chemical reactions that raise new challenges to chemical reaction engineering. These are reviewed along with recent examples of applications of chemical reaction engineering to microelectronic processing. Chemical vapor deposition and plasma processing of thin films are emphasized as areas where chemical reaction engineering could have a significant impact. Other thin film processes, e.g. physical vapor deposition and oxidation, are surveyed briefly. Bulk crystal growth analysis is included to demonstrate recent advances in detailed modelling of physical transport processes of interest to reactor modelling. Finally, common challenges, including micro/macroscopic modelling, large scale computing and fundamental physicochemical phenomena are discussed.

KEY WORDS

Electronic materials; crystal growth; chemical vapor deposition; plasma processing; thin film processing; reactor modelling.

INTRODUCTION

[001] Starting with the announcement of the transistor in 1948 and the introduction of the planar transistor in 1959 the microelectronics industry has undergone an impressive evolution to the current state where microelectronic circuits are essential in almost all aspects of modern society. For the last 25 years the number of components in the most advanced integrated circuits has doubled every year to the present level of 10^6 transistors on a chip (cf. Warner and Grung, 1983 and references within for a short historical overview). Si continues to be the major semiconductor material for the microelectronic industry while compound semiconductors such as GaAs, AlGaAs, and GaInAsP find increasing use in high speed electronic devices and optoelectronic components. The latter technology is critical for fiberoptic communication and future optical computing and storage systems.

[002] The rapid and extensive growth in microelectronics owes much to the scientists and engineers concerned with solving materials and processing problems associated with achieving new device structures and ever higher levels of integration. These problems are compounded and new ones arise as the minimum feature size of a device shrinks below one micron, as the level of integration grows, and as new materials such as polymers are incorporated into device structures. In addition, compound semiconductor technology raises processing challenges beyond those commonly found in Si based fabrication. This review aims to demonstrate that chemical reaction engineering could play a significant role in understanding these problems and advancing fabrication techniques. Existing semiconductor unit operations, where chemical reaction engineering approaches readily apply, are described along with new challenges to the discipline. First, general characteristics of microelectronics processing are discussed.

MICROELECTRONIC PROCESSING

[003] Fabrication of microelectronic components involves a variety of complex chemical processes which can be divided into the unit operations summarized in Table 1. Chemical reaction engineering concepts are particularly relevant to chemical vapor deposition and plasma processing. The unit operations are combined in the manufacturing process to produce three dimensional microstructures, which determine the performance of the final electronic component.

[004] Figure 1 illustrates two typical device structures: (A) a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) representing Si based technology and (B) an InGaAsP semiconductor laser exemplifying III-V compound semiconductor processes. The "building" of a particular microelectronic

TABLE 1 Microelectronic Unit Operations

Unit Operation	Examples
Bulk crystal growth	Czochralski, floating zone, Bridgman
Liquid phase epitaxy (LPE)	
Physical vapor deposition (PVD)	evaporation, molecular beam epitaxy (MBE), sputtering
Chemical vapor deposition (CVD)	low pressure CVD, organometallic CVD, laser CVD
Doping	diffusion, ion implantation
Oxidation	
Resist processing	coating, baking, development
Plasma processing	plasma enhanced chemical vapor deposition (PECVD), plasma etching
Packaging	encapsulation, bonding
Substrate cleaning	

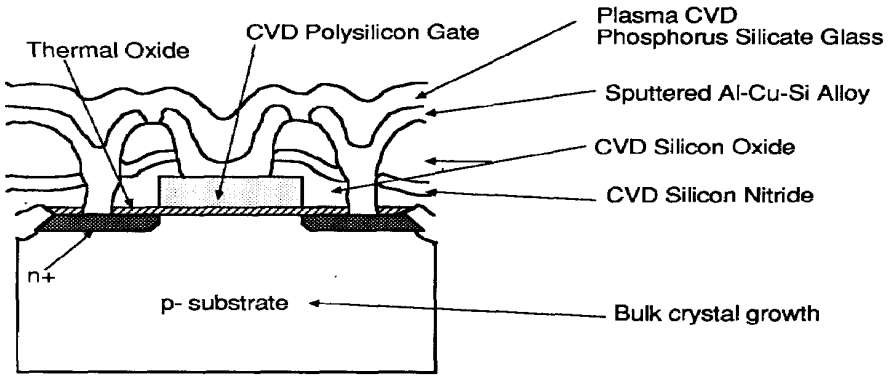

Fig. 1a. Metal oxide semiconductor field effect transistor (MOSFET) (after Douglas, 1980).

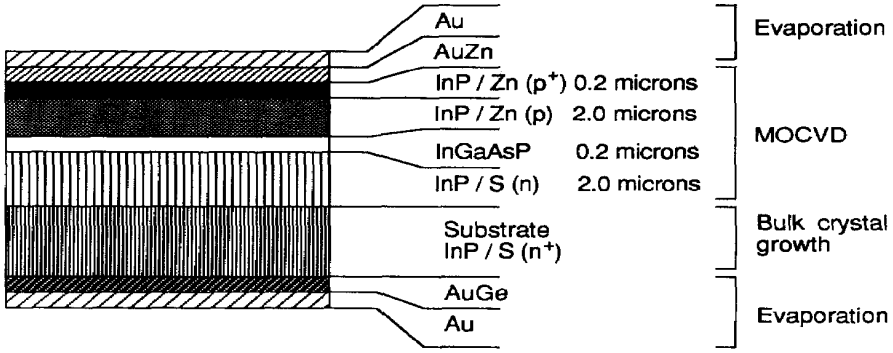

Fig. 1b. InGaAsP semiconductor laser (after Li, 1985).

circuit involves a long sequence of the unit operations conducted in batch mode. The process commonly entails more than 30 individual steps (cf. Parrillo, 1983) and complex, advanced microprocessors can involve as many as 200 steps. The ultimate measure of whether or not these have been done successfully is the performance of the final circuit.

[005] Figure 2 illustrates a typical process sequence for a simple Si MOS structure. Metallurgical Si is refined by reacting it with HCl in a fluidized bed to chlorosilanes and then purifying one of them, typically $SiHCl_3$ by distillation. High purity polycrystalline Si is subsequently grown from the $SiHCl_3$ by chemical vapor deposition and then melted. Up to 0.25 m diameter boules of single crystalline Si are pulled from the melt, mostly by Czochralski crystal growth. The boules are cut into thin wafers, which are chemomechanically polished. Impurities are removed from the near surface region by "gettering processes".

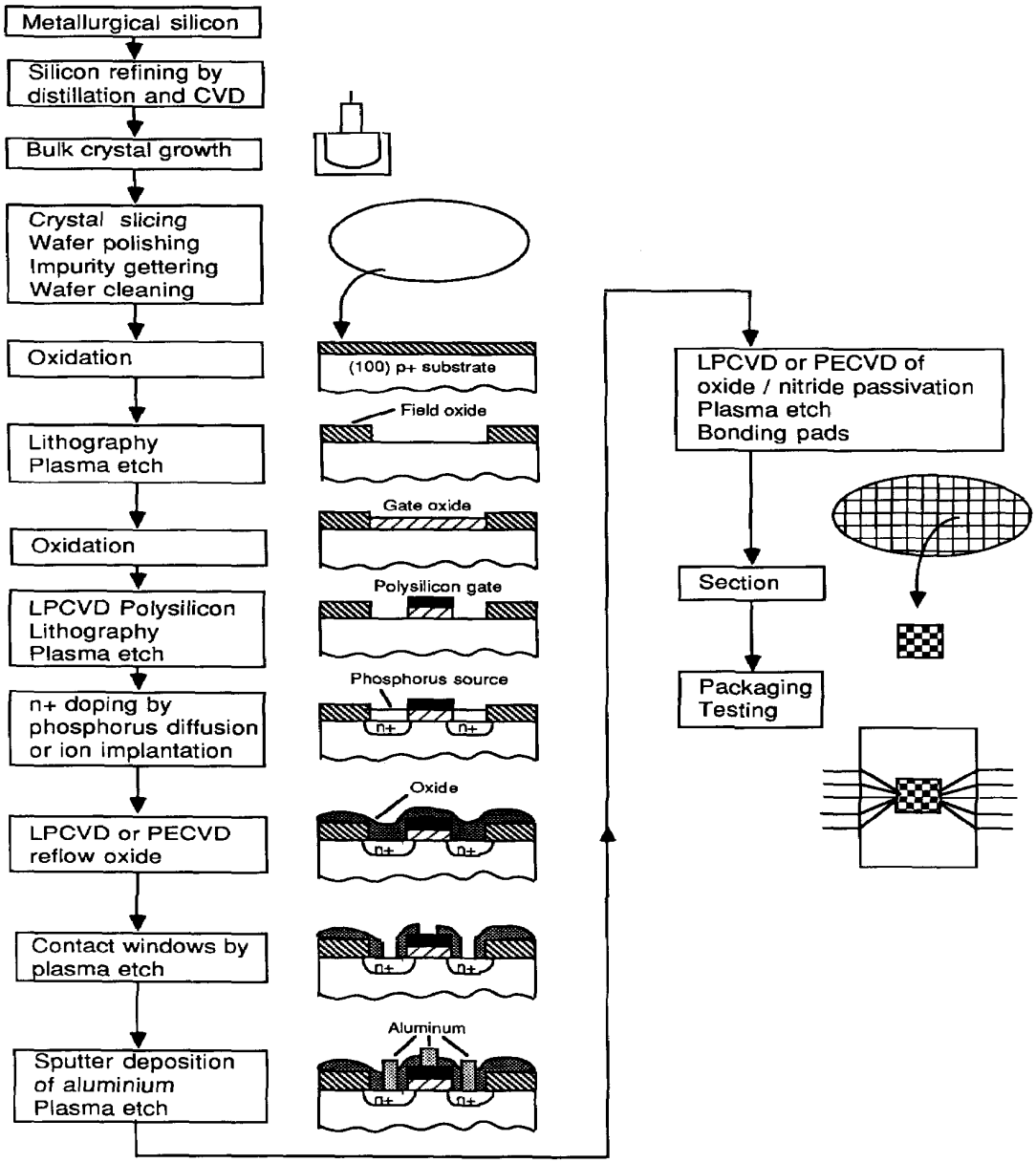

Fig. 2. Typical fabrication sequence for MOS technology.

[006] The MOS structure is constructed on the wafer utilizing 1–2 μm of the gettered subsurface region. First, a SiO_2 layer is formed by a gas solid reaction of Si with O_2 (dry oxidation) or H_2O (wet oxidation). An opening is defined in this layer by lithography, which involves coating the surface with a radiation sensitive polymer resist. By exposing the resist to UV light through a mask, the exposed region is either made less soluble than the original resist by crosslinkages (negative resist) or it is made more soluble by chain scission (positive resist). After development of the resist in a suitable solvent the remaining resist serves as a mask for transferring the pattern to the underlying oxide layer. This step is usually done by plasma etching.

[007] Next a gate oxide is grown by oxidation of the Si exposed by the SiO_2 etch. The original field

oxide also thickens during this step. Next polycrystalline Si is grown as a gate material by low pressure chemical vapor deposition (LPCVD). Areas for source and drain are opened by lithography and plasma etching. Subsequently, the reexposed Si is doped with an n-type dopant (P or As) to form the source and drain regions. This can be done by either depositing a phosphorus oxide and diffusing P into the Si at high temperatures or by embedding P into the Si by ion implantation. The latter is the preferred technique today.

[008] LPCVD or plasma enhanced CVD is used to cover the whole device by a silicon oxide containing phosphorus and perhaps also boron oxides to obtain the required stress and reflow characteristics. The reflow smooths corners in the surface topography so that metal contact lines may be put down with reduced shadowing and thinning problems. Connections to the source, the gate and the drain are made by opening holes to the underlying Si through the use of lithography and plasma etching followed by sputter deposition of Al or Al-alloy films. The metal film is then patterned, as the other thin film have been, by lithography and plasma etching. The final metallization pattern also acts as interconnections between devices on the die (chip).

[009] The final microcircuit is protected by a silicon oxide or nitride layer deposited by plasma enhanced CVD. Bonding pads are opened in this layer and the circuit is tested. The wafer is then diced and working circuits are encapsulated in ceramic or polymer packages.

[010] In order to realize current device structures with 1 μm minimum feature size and narrow junctions, the actual fabrication process is more complex than the one outlined in Fig. 2. For example, interdiffusion effects make it necessary to deposit a barrier between the Al metallization and Si. Additional and more difficult steps may be involved in compound semiconductor processing since these materials tend to decompose at elevated temperatures and do not form a stable oxide with properties similar to SiO_2. Unit operations, process sequences and device examples are described in a number of texts and tutorial papers (Chemla, 1985; Doane and coworkers, 1982; Ferry, 1985; Howes and Morgan, 1985; Ghandhi, 1983; Larrabee, 1985; Li, 1985; Meindl, 1978; Oldham, 1978; Suematsu, 1985; Sze, 1983).

[011] The unit operations have a number of common features of interest for reaction engineering analysis. They involve complicated gas phase and heterogeneous reactions in reactor geometries that are difficult to model. Since the manufacturing process is designed to produce identical microstructures with submicron accuracy in line widths, feature alignments, junction depths and etch trench profiles over a 150 mm diameter wafer, characteristic length scales differ by 5-6 orders of magnitude. The same situation arises in heterogeneous catalysis where the active catalyst material often is dispersed as 10 nm crystallites within a 10 mm particle. However, in many catalytic systems details of the microscopic behavior are not essential for prediction of reactor performance so a continuum description on the particle size scale may be used. The length scale issue is further complicated in microelectronic systems by low operating pressures that imply that the mean free path is greater than the minimum feature size but less than the characteristic size of the equipment. Thus a Monte-Carlo simulation may be appropriate at the microscopic level while a conventional continuum description is necessary for the macroscopic analysis. Orders of magnitude variations in characteristic time scales are also encountered either as a result of fast chemical reactions or large differences between transport and reaction rates. These length and time scale magnitude variations create numerical problems for the solution of reactor models by requiring finely meshed spatial discretizations and stiff ordinary differential equation solvers.

[012] Microelectronic processing involves high purity starting materials and well characterized single crystalline substrates, at least in the initial process step. Impurities on the ppm and even ppb in some compound semiconductor cases can drastically affect device performance. This poses practical difficulties but is advantageous for analysis. Surface reaction rates determined by single crystal surface studies are relevant to process studies and the reactor inlet fluid compositions are well defined. This is not the case in classical reaction engineering problems such as hydrodesulfurization where the feedstock contains numerous poorly characterized substances and the reaction mechanisms and rates are unknown except for a few model reactant species. In the following sections additional general issues as well as specific reaction engineering problems are addressed for the unit operations in Table 1. Particular emphasis will be given to chemical vapor deposition and plasma processing.

CRYSTAL GROWTH

Starting Materials

[013] Silicon refining starts with metallurgical Si (98% Si) which is reacted with HCl in a fluid bed reactor in the presence of a catalyst to form a mixture of chlorosilanes. The $SiHCl_3$ fraction is purified by distillation and reduced with H_2 to polycrystalline Si by chemical vapor deposition (CVD) on resistively heated Si rods in a so-called Siemens decomposer. The result is electronic grade polycrystalline Si with impurity levels in the sub ppb range. The refining process clearly involves classical chemical engineering unit operations except for the CVD of polycrystalline Si. Detailed analysis of the Siemens decomposer is difficult because of complex flow and temperature distributions, but Lai and coworkers (1985) have gained some insights into the overall reactor performance by using a CSTR model. The fundamental issues in this and other CVD systems will be discussed in a later section.

[014] Since the Siemens process is an electric power, equipment and labor intensive semi-batch process,

there has been considerable interest in replacing it with a continuous production scheme that would convert SiH_4 into Si powder by gas-phase nucleation and particle growth. This powder could then be fed directly to the single crystal growth stage without exposure to the atmosphere and grinding equipment, reducing the chance of contamination. Early work on this so-called free-space reactor was done by Levin (1980) and Lay and Iay (1981). However, since SiH_4 readily nucleated in the gas phase and the residence time was too short for significant growth by Brownian coagulations, the reported Si particle sizes were submicron.

[015] The practical and fundamental issues involved in designing an aerosol process for growing sufficiently large particles (~ 10 μm) for efficient collection have been investigated extensively by Flagan and coworkers (Alam and Flagan, 1984, 1986; Flagan, 1984; Wu and Flagan, 1985). They propose to generate seed particles by homogeneous nucleation of the reaction products of SiH_4 and then increase the size of the particles by chemical vapor deposition. The latter step has to be done at a slow enough rate that transport of reactants to the particle surface prevents significant supersaturation from occurring. Thus, reaction engineering analysis is necessary to understand the role of the various rate processes and identify conditions under which large particles can be grown. Alam and Flagan (1984, 1986) have addressed some of the nucleation issues, but questions still remain in the kinetics of nucleation and particle growth by CVD as well as in the coupling of these with physical transport processes within the reactor.

[016] Growth of Si particles from SiH_4 or $SiHCl_3$ in a fluidized bed reactor is also a potential configuration for continuous production of Si powder. In this reactor the particles grow by scavenging small particles produced by homogeneous nucleation and by CVD. Material purity is an issue because of the contamination from reactor walls and internals as well as from possible low purity seed particles fed to the reactor (Alam and Flagan, 1986). The system has been studied experimentally by Hsu and coworkers (1984) and Lai and coworkers (1986) have recently formulated two models for the fluidized bed reactor with simultaneous CVD and agglomeration of Si fines from homogeneous nucleation.

[017] In comparison to Si production there has been little work on continuous refining of starting materials for compound semiconductor crystal growth. The main driving force for Si has been the reduction of materials cost for solar cell applications. This has not been an issue for GaAs and related compound semiconductors, which are produced in much smaller quantities than Si. Furthermore, the crystal quality is difficult to control (cf. Howes and Morgan, 1985; Gatos and Lagowski, 1983). Therefore, compounds such as GaAs are produced by direct reaction of batch refined constituents, e.g. pure Ga and As. The reaction is exothermic and complicated by widely differing vapor pressures of the individual constituents (cf. Ghandhi, 1983, p.82; Howes and Morgan, 1985).

Bulk Crystal Growth from the Melt

[018] Although bulk crystal growth from the melt does not involve chemical reactions per se, it is worthwhile to include a short discussion of this process for completeness. Moreover, crystal growth analysis involves the same type of physical transport models that are needed for reactor studies. In fact, the use of detailed flow and energy computations in crystal growth modelling, notably by Brown and Crochet and their respective coworkers, could serve as an example for more consideration of flow phenomena in chemical reaction engineering. This is the topic of a companion paper by Crochet (1986) in this issue. Since there is voluminous literature on crystal growth and the field is very active, only key references pertinent to the present review will be included.

[019] There are three major bulk crystal growth processes: Czochralski, floating zone, and Bridgman (Foster, 1977; Grabmaier, 1981; Pamplin, 1975). These are illustrated schematically in Fig. 3.

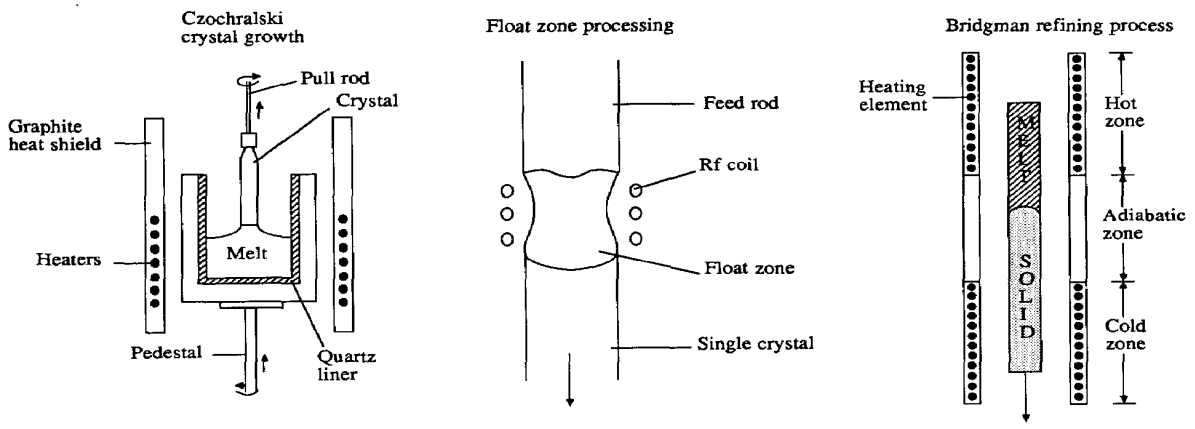

Fig. 3. Crystal growth techniques.

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