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# United States Patent [19]

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Jeng

[45] Date of Patent: **Sep. 26, 1995**

[54] **LOW TEMPERATURE ANISOTROPIC ASHING OF RESIST FOR SEMICONDUCTOR FABRICATION**

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"Electron Cyclotron Resonance Plasma Etching of Photoresist at Cryogenic Temperatures", J. Appl. Phys., vol. 72, No. 7, pp. 3050-3057; Oct.-1992-Varhue et al.

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[21] Appl. No.: **242,922**

### [57] ABSTRACT

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This invention encompasses using anisotropic plasma at a low temperature to strip resist from a semiconductor wafer. A semiconductor wafer **10** is placed in a reactor **26** which contains an oxygen plasma source **28**. The oxygen plasma source **28** emits oxygen plasma **32** which is drawn towards the biased wafer **10**, exposing the resist layer **22** of the wafer to anisotropic oxygen plasma. A sensor **30** detects when the ashing of the resist is complete, and then the plasma source is turned off.

[51] Int. Cl.<sup>6</sup> ..... **H01L 21/00**

[52] U.S. Cl. .... **156/659.11**

[58] Field of Search ..... 156/626, 627, 156/643, 659.1, 661.1, 345

Advantages of the invention include the ability to remove resist from wafers without damaging polymeric dielectric layers, which are sensitive to the harsh effects of traditional resist removal methods. With the present invention, very little damage occurs to the material on the sidewalls of vias.

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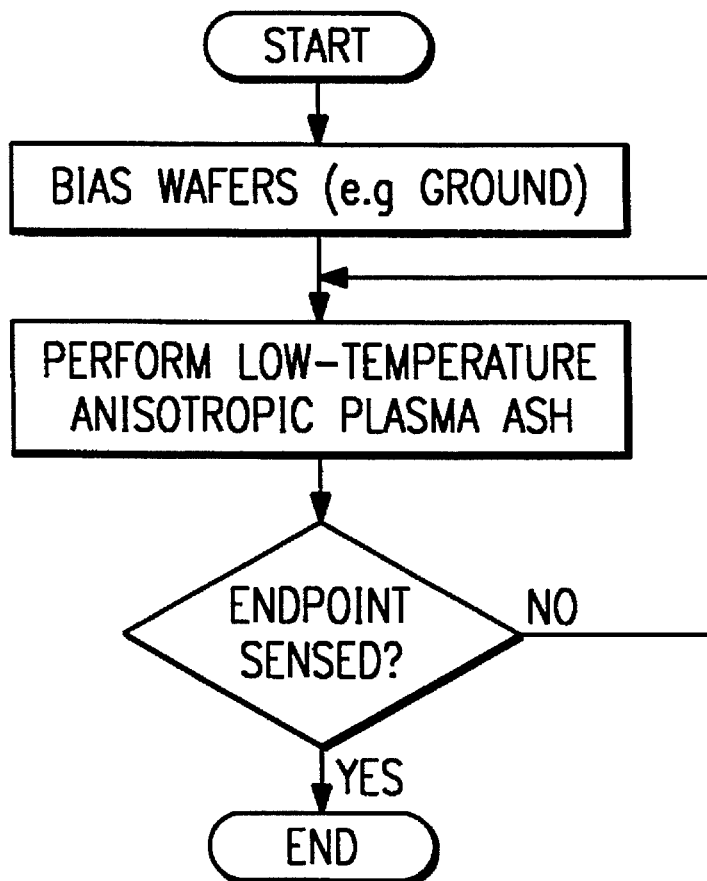
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4 Claims, 3 Drawing Sheets



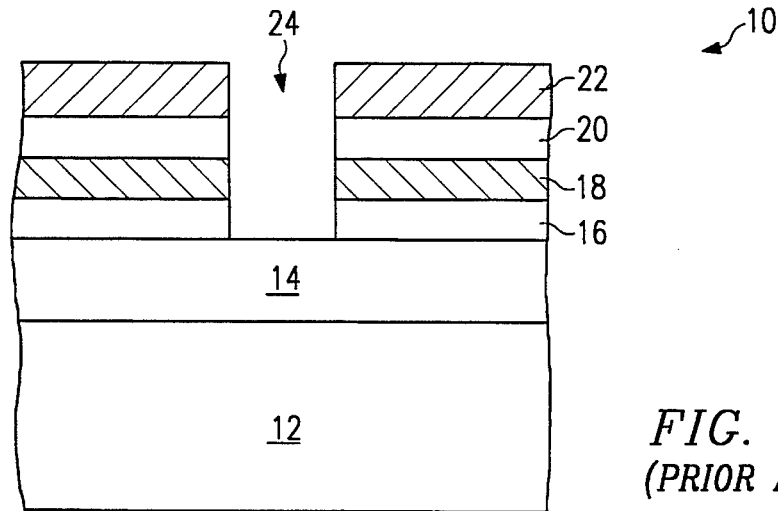


FIG. 1A  
(PRIOR ART)

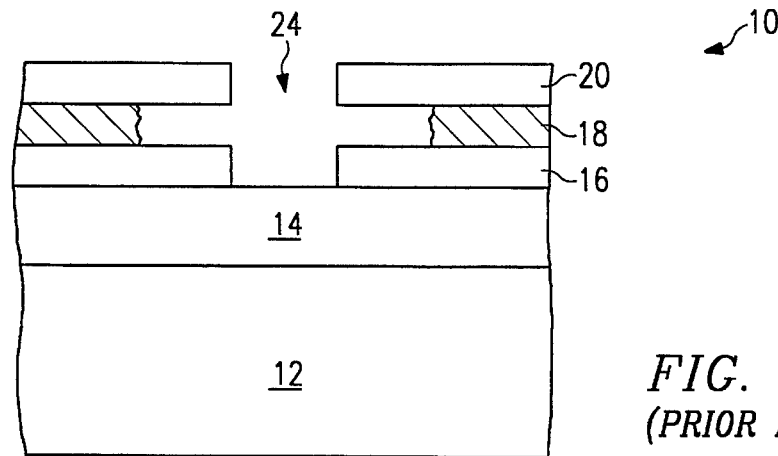


FIG. 1B  
(PRIOR ART)

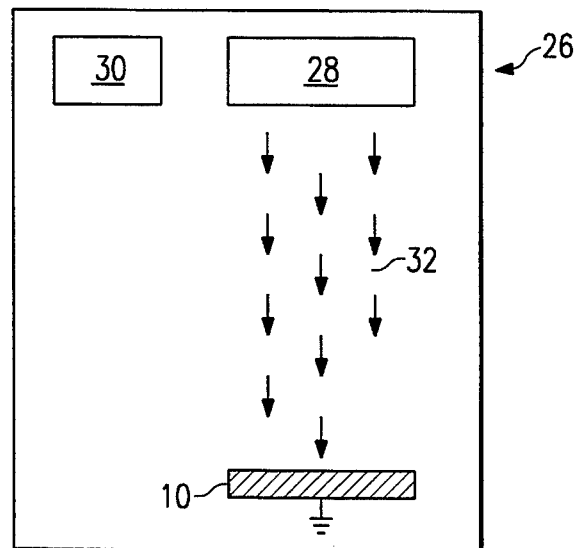


FIG. 2

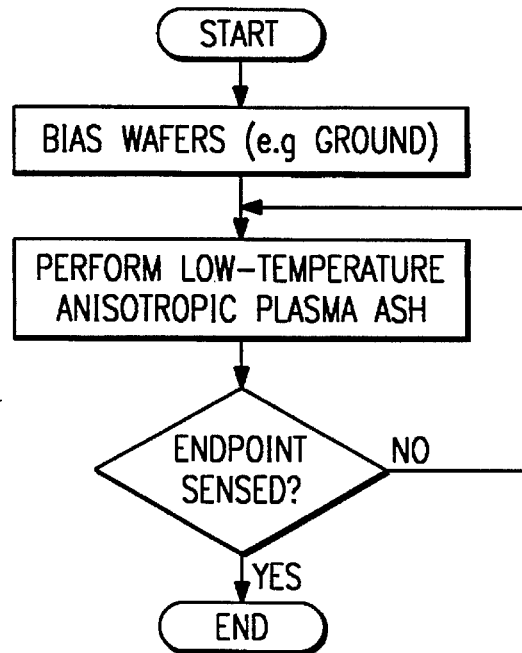


FIG. 3

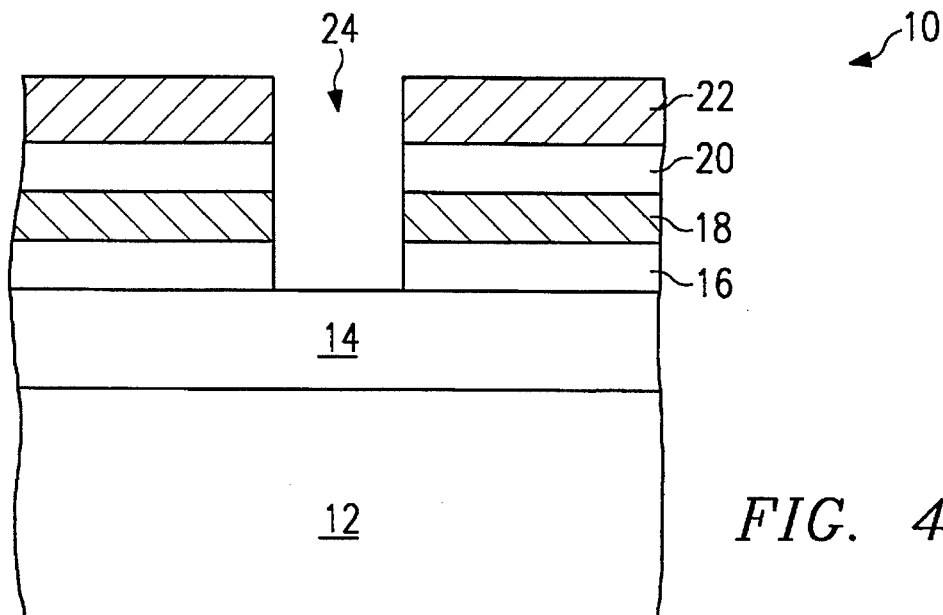


FIG. 4A

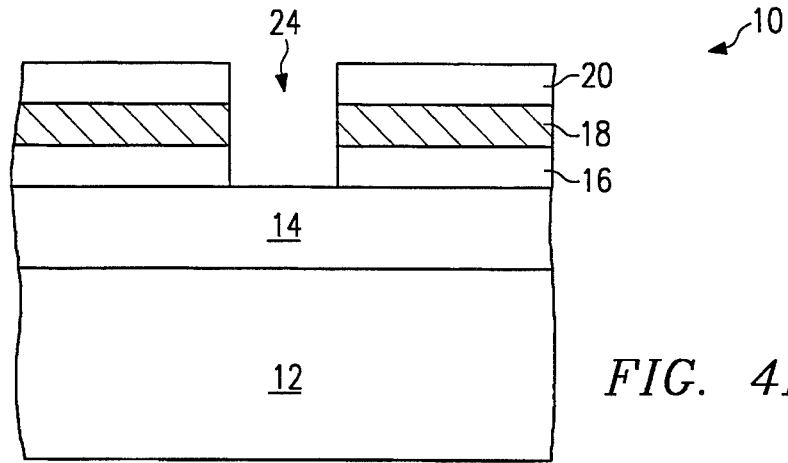


FIG. 4B

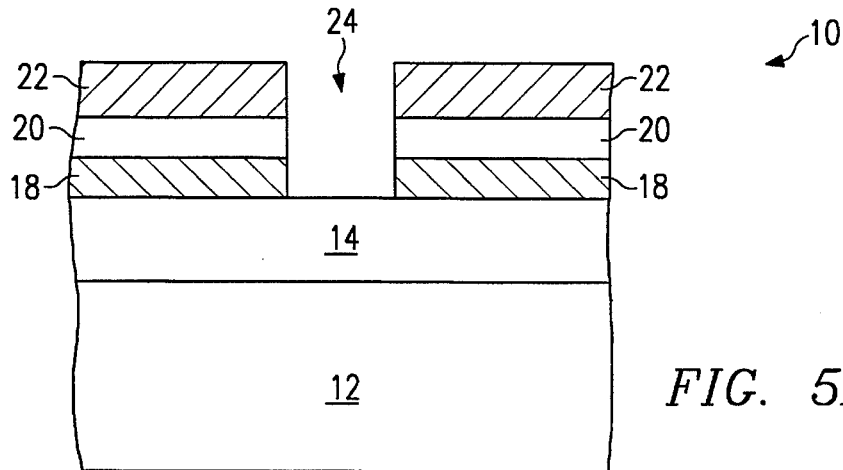


FIG. 5A

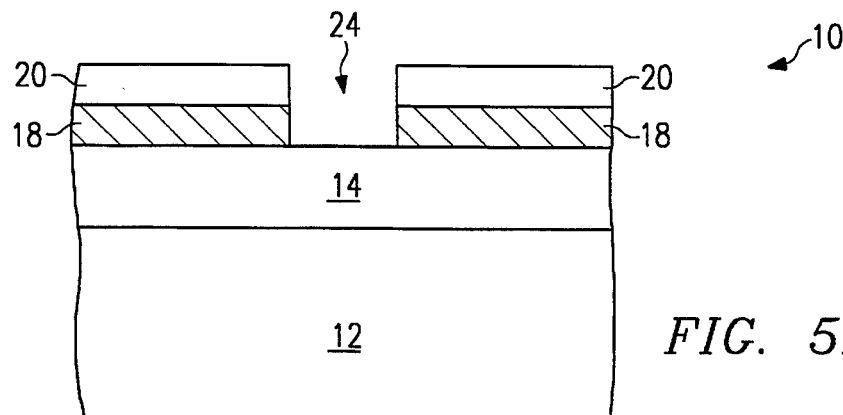


FIG. 5B

**LOW TEMPERATURE ANISOTROPIC  
ASHING OF RESIST FOR  
SEMICONDUCTOR FABRICATION**

**FIELD OF THE INVENTION**

This invention relates generally to the fabrication of semiconductor devices, and more specifically to resist strip processes.

**BACKGROUND OF THE INVENTION**

Semiconductors are widely used in integrated circuits for electronic applications, including radios and televisions. Such integrated circuits typically use multiple transistors fabricated in single crystal silicon. Many integrated circuits now contain multiple levels of metallization for interconnections. As geometries shrink and functional density increases, it becomes imperative to reduce the RC time constant within multi-level metallization systems.

Although the dielectric typically used in the past to isolate metal lines from each other was silicon dioxide, recent trends have been towards using materials with low-dielectric constants in order to reduce the RC time constant. Many low-dielectric insulators are either pure polymers (e.g. parylene, BCB, teflon, polyimide) or organic spin-on glass (OSOG, e.g. silsequioxane and siloxane glass). The oxidation resistance of these low-dielectric materials is generally poorer than the oxidation resistance of silicon dioxide.

Conventional ash processes are available for high-aspect-ratio contacts and vias; however, such processes are damaging to dielectric materials, especially low-dielectric materials. Oxygen plasma (ash) is commonly used to remove photoresist from wafer surfaces. The conventional ash process is performed in barrel and down-stream reactors, and is carried out at a high temperature (approximately 250° C.) for a long period of time to assure that all photoresist is completely cleared. Unfortunately, high temperature ash processes not only clear photoresist from the surface of the wafer, but also remove polymer contents from low-dielectric materials, resulting in problems such as shrinking, cracking, moisture absorption, via poisoning, undercutting, and general degradation of the dielectric property of low-dielectric materials. Via integration has presented a problem in the use of low-dielectric materials.

Thus, the use of low-dielectric constant materials in the semiconductor industry has resulted in the need for an ash process that does not damage polymeric dielectric materials while removing the photoresist.

**SUMMARY OF THE INVENTION**

This invention encompasses using anisotropic plasma at a low temperature to strip resist from a semiconductor wafer. A semiconductor wafer is placed in reactor which contains an oxygen plasma source and an optional sensor. The oxygen plasma source emits oxygen plasma which is drawn towards the wafer by an electric field, exposing the surface of the wafer to anisotropic oxygen plasma. A sensor detects when the ashing of the photoresist of the wafer is complete,

and then the plasma source is turned off.

One embodiment is a method for removing resist from a semiconductor wafer, including the steps of coating a substrate with a polymeric dielectric layer, applying an inorganic layer over the polymeric dielectric layer, applying a resist layer over the inorganic layer, patterning the resist layer, etching the inorganic layer, and ashing the resist with an anisotropic oxygen plasma.

Another embodiment is a system for removing resist from a semiconductor wafer, comprising a reactor, a wafer having a polymeric dielectric layer positioned within the reactor, and an oxygen plasma generator located inside the reactor.

An advantage of the invention is the ability to remove resist from wafers with low-dielectric materials, which are sensitive to the harsh effects of traditional resist removal methods. The decomposition of low-dielectric constant materials, which may activate the oxidation reaction, is minimized by lowering the wafer (substrate) temperature. With the present invention, very little damage occurs to the material on the sidewall of the vias.

**BRIEF DESCRIPTION OF THE DRAWINGS**

In the drawings, which form an integral part of the specification and are to be read in conjunction therewith, and in which like numerals and symbols are employed to designate similar components in various views unless otherwise indicated:

FIG. 1 is a prior art drawing showing the effects of a conventional ash process on a cross-sectional view of a semiconductor via;

FIG. 2 shows a typical environment in which the present invention may be performed;

FIG. 3 is a flow chart of the process steps of the invention;

FIG. 4 is a cross-sectional view showing the effects of the present invention on a semiconductor via; and

FIG. 5 is a cross-sectional view of an example of an alternate semiconductor circuit.

**DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS**

The making and use of the presently preferred embodiments are discussed below in detail. However, it should be appreciated that the present invention provides many applicable inventive concepts which can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not delimit the scope of the invention.

The following is a description of several preferred embodiments and alternative embodiments, including manufacturing methods. Corresponding numerals and symbols in the different figures refer to corresponding parts unless otherwise indicated. Table 1 below provides an overview of the elements of the embodiments and the drawings.

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