

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

ALACRITECH, INC.,

Plaintiff,

v.

CENTURY LINK COMMUNICATIONS
LLC, ET AL.,

Defendants,

INTEL CORPORATION, ET AL.,

Intervenors.

Case No. 2:16-cv-00693-RWS-RSP
(Lead Case)

MEMORANDUM OPINION AND ORDER ON CLAIM CONSTRUCTION

Before the Court is the opening claim construction brief of Alacritech, Inc. (Plaintiff) (Dkt. No. 181, filed on April 4, 2017),¹ the response of Tier 3, Inc., Savvis Communications Corp., CenturyLink Communications LLC, Dell Inc., Wistron Corp., Wiwynn Corp., SMS Infocomm Corp., Cavium, Inc., and Intel Corporation (collectively, “Defendants”) (Dkt. No. 303, filed under seal on July 10, 2017), and the reply of Plaintiff (Dkt. No. 307, filed under seal on July 14, 2017). The Court held a hearing on the issues of claim construction and claim definiteness on August 7, 2017. Having considered the arguments and evidence presented by the parties at the hearing and in their briefing, the Court issues this Order.

¹ Citations to the parties’ filings are to the filing’s number in the docket (Dkt. No.) and pin cites are to the page numbers assigned through ECF.

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I. BACKGROUND

Plaintiff alleges infringement of eight U.S. Patents: No. 7,124,205 (the '205 Patent), No. 7,237,036 (the '036 Patent), No. 7,337,241 (the '241 Patent), No. 7,673,072 (the '072 Patent), No. 7,945,699 (the '699 Patent), No. 8,131,880 (the '880 Patent), No. 8,805,948² (the '948 Patent), and No. 9,055,104 (the '104 patent) (collectively, the "Asserted Patents"). The '205, '036, '241, '072, '699, '880, and '948 Patents are related through separate chains of continuation and continuation-in-part applications that ultimately converge on a provisional application filed on Oct. 14, 1997, U.S. Provisional Patent Application 60/061,809 (the '809 Provisional). The '104 Patent claims priority back to a provisional application filed on April 22, 2002.

The Asserted Patents each pertain generally to technology for accelerating computer networking. The '205, '036, '241, '072, '699, and '880 Patents are generally directed to network-accelerating technology that offloads some of the network-layer processing from the computer processor to an interface device. The '104 Patent is generally directed to network-accelerating technology that reduces delays that result from waiting on data-receipt acknowledgments.

The abstracts and exemplary claims of the Asserted Patents provide as follows:

The abstract of the '205 Patent provides:

A network interface device connected to a host provides hardware and processing mechanisms for accelerating data transfers between the host and a network. Some data transfers are processed using a dedicated fast-path whereby the protocol stack of the host performs no network layer or transport layer processing. Other data transfers are, however, handled in a slow-path by the host protocol stack. In one embodiment, the host protocol stack has an ISCSI layer, but a response to a solicited ISCSI read request command is nevertheless processed by the network interface device in fast-path. In another embodiment, an initial portion of a response to a solicited command is handled using the dedicated fast-path and then after an error

² The parties do not present the Court with any claim-construction disputes from the '948 Patent.

condition [sic] occurs a subsequent portion of the response is handled using the . . . slow-path. The interface device uses a command status message to communicate status to the host.

The abstract of the '036 Patent provides:

A system for protocol processing in a computer network has an intelligent network interface card (INIC) or communication processing device (CPD) associated with a host computer. The INIC provides a fast-path that avoids protocol processing for most large multi-packet messages, greatly accelerating data communication. The INIC also assists the host for those message packets that are chosen for processing by host software layers. A communication control block for a message is defined that allows DMA controllers of the INIC to move data, free of headers, directly to or from a destination or source in the host. The context is stored in the INIC as a communication control block (CCB) that can be passed back to the host for message processing by the host. The INIC contains specialized hardware circuits that are much faster at their specific tasks than a general purpose CPU. A preferred embodiment includes a trio of pipelined processors with separate processors devoted to transmit, receive and management processing, with full duplex communication for four fast Ethernet nodes.

The abstract of the '241 Patent provides:

A system for protocol processing in a computer network has an intelligent network interface card (INIC) or communication processing device (CPD) associated with a host computer. The INIC provides a fast-path that avoids protocol processing for most large multi-packet messages, greatly accelerating data communication. The INIC also assists the host for those message packets that are chosen for processing by host software layers. A communication control block for a message is defined that allows DMA controllers of the INIC to move data, free of headers, directly to or from a destination or source in the host. The context is stored in the INIC as a communication control block (CCB) that can be passed back to the host for message processing by the host. The INIC contains specialized hardware circuits that are much faster at their specific tasks than a general purpose CPU. A preferred embodiment includes a trio of pipelined processors with separate processors devoted to transmit, receive and management processing, with full duplex communication for four fast Ethernet nodes.

The abstract of the '072 Patent provides:

A system for protocol processing in a computer network has an intelligent network interface card (INIC) or communication processing device (CPD) associated with a host computer. The INIC provides a fast-path that avoids protocol processing for most large multi-packet messages, greatly accelerating data communication. The INIC also assists the host for those message packets that are chosen for processing by host software layers. A communication control block for a message is defined that allows DMA controllers of the INIC to move data, free of headers, directly to or from a destination or source in the host. The context is stored in the INIC as a communication control block (CCB) that can be passed back to the host for message processing by the host. The INIC contains specialized hardware circuits that are much faster at their specific tasks than a general purpose CPU. A preferred embodiment includes a trio of pipelined processors with separate processors devoted to transmit, receive and management processing, with full duplex communication for four fast Ethernet nodes.

The abstract of the '699 Patent provides:

A Network Interface device (NI device) coupled to a host computer receives a multi-packet message from a network (for example, the Internet) and DMA's the data portions of the various packets directly into a destination in application memory on the host computer. The address of the destination is determined by supplying a first part of the first packet to an application program such that the application program returns the address of the destination. The address is supplied by the host computer to the NI device so that the NI device can DMA the data portions of the various packets directly into the destination. In some embodiments the NI device is an expansion card added to the host computer, whereas in other embodiments the NI device is a part of the host computer.

The abstract of the '880 Patent provides:

An intelligent network interface card (INIC) or communication processing device (CPD) works with a host computer for data communication. The device provides a fast-path that avoids protocol processing for most messages, greatly accelerating data transfer and offloading time-intensive processing tasks from the host CPU. The host retains a fallback processing capability for messages that do not fit fast-path criteria, with the device providing assistance such as validation even for slow-path messages, and messages being selected for either fast-path or slow-path processing. A context for a connection is defined that allows the device to move data, free of headers, directly to or from a destination or source in the host. The context can be passed back to the host for message processing by the host. The device contains

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