

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CAVIUM, INC.
Petitioner

v.

ALACRITECH, INC.
Patent Owner

Case IPR. No. **Unassigned**
U.S. Patent No. 8,850,948
Title: INTELLIGENT NETWORK INTERFACE SYSTEM AND METHOD FOR
PROTOCOL PROCESSING

**Declaration of Robert Horst, Ph.D. in Support of
Petition for *Inter Partes* Review
of U.S. Patent No. 8,850,948**

TABLE OF CONTENTS

	Page
I. INTRODUCTION AND QUALIFICATIONS	1
II. MATERIALS RELIED ON IN FORMING MY OPINION.....	3
III. UNDERSTANDING OF THE GOVERNING LAW	4
A. Invalidity by Anticipation	4
B. Invalidity by Obviousness	5
IV. LEVEL OF ORDINARY SKILL IN THE ART	6
V. STATE OF THE ART AND OVERVIEW OF TECHNOLOGY AT ISSUE.....	8
A. Layered Network Protocols.....	8
1. OSI Layers	8
2. TCP/IP Layers.....	8
B. TCP/IP	10
1. Encapsulation	12
2. Ethernet Header.....	14
3. IP Header.....	16
4. TCP header.....	17
5. Application Data	22
6. RFC 793 – TCP Specification.....	22
B. Protocol Offload and Fast-Path Processing.....	22
1. RFC 647 – Front-Ending.....	23
2. RFC 929 – Outboard Processing.....	24
3. Mediation Levels.....	25
C. Offloaded Protocols.....	28
1. OSI Protocol Offload	28
2. TCP/IP Protocol Offload.....	28
3. VMTP and XTP Protocol Offload	28
4. Multi-Protocol Offload	29

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D.	Portions of the Protocol Offloaded.....	29
1.	Checksum Offload	30
2.	Full Offload.....	30
3.	Multi-Level Offload	31
4.	Header Prediction.....	31
E.	Offload Implementation	34
1.	Multiprocessor Offload	34
2.	Offload Adapters based on Microprocessors	36
3.	Offload Adapters based on Custom Processors or Custom Logic	37
F.	Protocol Offload Summary	40
G.	Additional Background Technology	41
1.	DMA	41
2.	Virtual and Physical Memory Addresses.....	43
VI.	OVERVIEW OF 948 PATENT	45
VII.	948 PATENT PROSECUTION HISTORY	48
VIII.	CLAIM CONSTRUCTIONS	49
A.	Legal Standard.....	49
IX.	THE PRIOR ART.....	50
A.	Thia: Thia, A Reduced Operation Protocol Engine (ROPE) for a multiple-layer bypass architecture (1995).....	50
B.	Tanenbaum96: A. Tanenbaum, Computer Networks, 3rd ed. (1996)	57
C.	Stevens2: Stevens, TCP-IP Illustrated, Vol. 2	68
X.	Obviousness Combinations – Motivations To Combine.....	71
A.	Thia in Combination with Tanenbaum96.....	71
B.	Thia in Combination with Tanenbaum96 and further in Combination with Stevens2	75
XI.	FOUNDATIONS OF INVALIDITY	77

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I, Robert Horst, hereby declare as follows:

I. INTRODUCTION AND QUALIFICATIONS

1. My name is Robert Horst. I have been retained on behalf of Petitioner Cavium, Inc. (“Cavium”) to provide this Declaration concerning technical subject matter relevant to the petition for *inter partes* review (“Petition”) concerning U.S. Patent No. 8,850,948 (Ex.1001, the “948 Patent”). I reserve the right to supplement this Declaration in response to additional evidence that may come to light.

2. I am over 18 years of age. I have personal knowledge of the facts stated in this Declaration and could testify competently to them if asked to do so.

3. My compensation is not based on the resolution of this matter. My findings are based on my education, experience, and background in the fields discussed below.

4. I am an independent consultant with more than 30 years of expertise in the design and architecture of computer systems. My current curriculum vitae is submitted as Exhibit 1004 and some highlights follow.

5. Currently, I am an independent consultant at HT Consulting where my work includes consulting on technology and intellectual property. I have testified as an expert witness and consultant in patent and intellectual property litigation as well as *inter partes* reviews and re-examination proceedings.

6. I earned my M.S. (1978) in electrical engineering and Ph.D. (1991) in computer science from the University of Illinois at Urbana-Champaign after earning my B.S. (1975) in electrical engineering from Bradley University. During my master’s program, I designed, constructed and debugged a shared memory parallel microprocessor system. During my doctoral program, I designed and simulated a massively parallel, multi-threaded task flow computer.

7. After receiving my bachelor’s degree and while pursuing my master’s degree, I worked for Hewlett-Packard Co. While at Hewlett-Packard, I designed the micro-sequencer and cache of the HP3000 Series 64 processor. From 1980 to 1999, I worked at Tandem Computers, which was acquired by Compaq Computers in 1997. While at Tandem, I was a designer and architect of several generations of fault-tolerant computer systems and was the principal architect of the NonStop Cyclone superscalar processor. The system development work at Tandem also included development of the ServerNet System Area Network and applications of this network to fault tolerant systems and clusters of database servers.

8. Since leaving Compaq in 1999, I have worked with several technology companies, including 3Ware, Network Appliance, Tibion, and AlterG in the areas of network-attached storage and biomedical devices. From 2012 to 2015, I was Chief Technology Officer of Robotics at AlterG, Inc., where I worked

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