

I, Lisa Rowlison de Ortiz, declare:

1. I am the Head of Catalog & Metadata Services at University of California, Berkeley (“UC Berkeley”) library. I am familiar with the UC Berkeley library system, including the library catalog and policies and procedures regarding the receipt, indexing, and availability of books and periodicals.
2. According to UC Berkeley Library policies and procedures, Library items are indexed in the library catalog and are made freely available to the faculty and student body of UC Berkeley as well as to the general public.
3. The UC Berkeley library holds a copy of a chapter by Y.H. Thia and C.M. Woodside, “A Reduced Operation Protocol Engine (ROPE) for a multiple-layer bypass architecture,” published in the book Protocol for High Speed Networks IV, 1st Edition (TJ Press Ltd. 1995), pages 224-239. (“Thia”).
4. When a monograph is received and cataloged by the UC Berkeley Library, the date of cataloging is set and retained in the catalog record. The catalog date (“Cat Date”) for Thia is February 26, 1996 (*see* Exhibit A). Furthermore, after the volume is labeled and sent to its shelving location the date of receipt by this shelving location is stored in an internal note. This information shows that the volume was received by the Engineering Library on March 20, 1996. *Id.* The volume would have been available to the public within a few days of that date.

thereon. I declare that all statements made of my knowledge are true, and that all statements made on information and belief are believed to be true.

Executed on January 27, 2017, in Berkeley, California.

A handwritten signature in blue ink, reading "Lisa Rowlison de Ortiz", written over a horizontal line.

Lisa Rowlison de Ortiz

Protocols High Speed Networks

Edited by

Gerald Neufeld and M
*Department of Computer Science
University of British Columbia
Vancouver
Canada*

CAVIUM-1064
Cavium, Inc. v. Alacritech, Inc.
Page 003

Sponsored by IFIP WG6.1/WG6.4 in co-
operation with the
IEEE Com. Soc.
Published by Chapman & Hall on behalf
of the
International Federation for Information



CHAPMAN & HALL
London · Glasgow · Weinheim
Melbourne · Madras

PART FIVE Protocols	
11 The design of BTOP – an ATM bulk transfer protocol <i>L. Casey</i>	171
12 High performance presentation and transport mechanisms for integrated communication subsystems <i>W.S. Dabbous</i>	189
13 PATROCLUS: a flexible and high-performance transport subsystem <i>T. Braun</i>	205
14 A reduced operation protocol engine (ROPE) for a multiple-layer bypass architecture <i>Y.H. Thia and C.M. Woodside</i>	224
PART SIX Implementation and Performance	
15 Deadlock situations in TCP over ATM <i>K. Moldakiev and P. Gunningberg</i>	243
16 A guaranteed-rate channel allocation scheme and its application to delivery-on-demand of continuous media data <i>T. Kamada, J. Ting and D. Fracchia</i>	260
17 A hybrid deposit model for low overhead communication in high speed LANs <i>R.B. Osborne</i>	276
PART SEVEN Posters	
18 A multimedia document distribution system over DQDB MANs <i>L. Ororzo-Barbosa and M. Soto</i>	295
19 From SDL specifications to optimized parallel protocol implementations <i>S. Leue and P. Oechslin</i>	308
20 Partial-frame retransmission scheme for data communication error recovery in B-ISDN <i>I. Inoue and N. Morita</i>	328
21 Protocol parallelization <i>Joseph D. Touch</i>	349
Index of contributors	361
Keyword index	362

PREFACE

Welcome to the fourth IFIP workshop on protocols for high speed networks held in Stockholm (1993) respectively. We received a large number of contributions. This year, forty papers were received of which twenty were presented as poster papers. Although the program committee decided to keep the number of papers to accommodate more discussion in keeping with the format of the workshop follows three very successful workshops held in 1990, 1991 and 1992 respectively.

Many people have contributed to the success of this workshop. We are thankful to all the authors of the papers that were presented and to the organizations which have contributed financially to this workshop. We are also thankful to the following organizations: CICS, UBC, MPR Teltech and Newbridge Networks.

Mabou Ito
Gerald Neufeld

Departments of Electrical Engineering and Computer Science
University of British Columbia

A Reduced Operation Protocol Engine (ROPE) for a multiple-layer bypass architecture

Y.H. Thia (*)¹ and C.M. Woodside (**)

Newbridge Networks, Inc., Ottawa, Canada (*) and
Dept. of Systems and Computer Engineering, Carleton University, Ottawa, Canada (**)

Abstract — The Reduced Operation Protocol Engine (ROPE) presented here offloads critical functions of a multiple-layer protocol stack, based on the "bypass concept" of a fast path for data transfer. The motivation for identifying this separate processing path is that it involves only a small subset of the complete protocol, which can then be implemented in hardware. Multiple-layer bypass also eliminates some inner-layer operations such as queue and buffer management, context switching and movement of data across layers, all of which are a significant overhead. ROPE is intended to support high-speed bulk data transfer. The paper describes the design of a ROPE chip for the OSI Session and Transport layer protocols, using VHDL. The design is practical in terms of chip complexity and area, using current gate array technology, and simulation shows that it can support a data rate approaching 1 gigabit per second, in a connection attached to an end-system.

Keyword codes: C.2.2, B.4.1

Keywords: Network Protocols, Data Communications Devices

1 Introduction

The advent of Fibre Optic technology, which offers high bandwidth and low bit error rates, has shifted the performance bottleneck from the communications channel to the communications processing in the end-points of the system [26]. Other trends such as improved quality-of-service guarantees will reinforce this effect. The heavy processing load is due to a combination of operating system overhead, protocol complexity, and per-octet processing on the data stream. To alleviate the end-system bottleneck one may consider new protocols [10], improved software implementation of existing protocols [5, 35], parallel processing techniques [14, 21, 38], special protocol structures [15, 30] and hardware assist [22] by offloading all or part of the protocol functions to an adaptor. This paper takes the latter approach.

The key problems associated with offboard processing include:

- Partitioning the functionality between the host and the adaptor is difficult and may easily lead to a complex additional protocol between the two parts, which may cancel out or offset the potential gain from offloading. For example, the buffer management task [36] may be offloaded, but this leaves the problem of control for accessing it within the full protocol logic.

¹ This research was done while Dr. Thia was at Carleton University

ROPE for a multiple-layer bypass

- Non-protocol-specific processing is a large part of the protocol stack. Examples include interrupt handling, context switching and in deeply layered protocol stacks.
- The choice of hardware for the adaptor depends on the protocol supports. In [2, 22] where the transport protocol layer is bypassed, the full protocol stack can be offloaded, general purpose hardware because of the complexity of existing protocols, VLSI data link layer has been disappointing so far. In [8] a support TCP checksums. Also, some newer lightweight protocols designed for VLSI implementation [1, 3].
- There is a tradeoff between performance, flexibility and the frequently executed portion of the protocol. The frequently executed portion of the protocol remains a significant advantage in providing hardware support for tasks in the host software for flexibility.
- As host processing speed continues to outpace memory bandwidth approaches the processor memory bandwidth, movement on the workstations down to the minimum.

This paper presents a feasibility study for a new approach that combines the relatively simple operations needed for data transfer provides a hardware "fast path" for them, which will be based on the "protocol bypass concept" [37] which is a "good Prediction" algorithm [20] for TCP/IP. Bypass solves the problem of how to may limit the use of offboard processing, by implementing bypass layers for certain cases. This simplifies the interface between the bypass layers and minimizes their interaction, which is supported by an interface and a simple command protocol. The chip design based on the Reduced Operation Protocol Engine. The contribution of the interface and the chip operation, and to report on a VLSI chip design. It appears to be feasible to support an end-system approaching 1 Gbps.

The next section introduces the bypass concept, its implementation. Section 3 analyzes the key protocol processing overheads for a bypass VLSI implementation. Sections 4, 5 and 6 describe the chip using the industry standard hardware description language. Section 7.

2 The Bypass Concept

A bypass adds an additional path for certain operations in the original software. Conformance to the protocol is maintained through the normal "heavyweight" path. A bypass path can be used or for both together, and is compatible with other end-systems.

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.