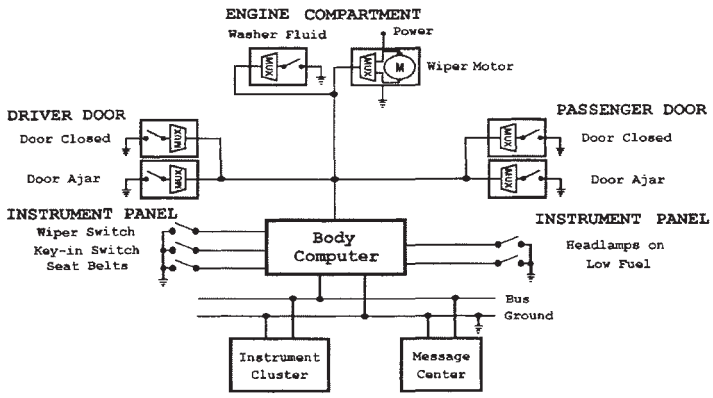


FIGURE 26.9 Base vehicle with Class B data link, body computer, instrument cluster, message center, and Class A network for sensors.

Class C Real-Time Control. The Class C network is the least mature network, and consensus of opinion on requirements does not yet exist. Experts cannot agree on many facets and many of the requirements are controversial. Many automotive engineers believe that an adequate statistical latency achievable with a bit-by-bit arbitration-based media access protocol is sufficient for real-time distributed Class C multiplexing. Others believe a token-passing media access protocol is required because a maximum latency is guaranteed, because with an arbitration-based media access only a statistical maximum latency is achievable. There are still others who argue that both the arbitration-based and token-passing media access is not good enough for tightly looped distributed processing because both methods have too great a variation in latency time. They argue that a time-triggered media access method is required because the network variations in latency should not affect tightly looped processing times. Other factors such as required data rates and the physical media type also remain open. It is clear that more research and development is required to resolve these questions.

26.2 ENCODING TECHNIQUES

The data encoding technique[4] has a significant effect on the radiated EMI. In order to achieve the highest possible data rate, it is important to choose a data-encoding technique that has the fewest transitions per bit with the maximum amount of time between transitions and bit-synchronized so that invalid bit testing can be effective. PWM, for example, has two transitions per bit with ⅓ bit times between transitions. NRZ has a maximum of one transition per bit but is increased to provide for synchronization. Some of the disk drive encoding techniques such as modified frequency modulation (MFM) are synchronous with fewer than one transition per bit. (See Table 26.1 for a comparison chart of a selection of encoding techniques used in vehicle multiplexing.)

The variable column in the table describes an attribute whereby the transmission time for data byte is a variable quantity depending on the data value. VPWM and Bit-Stuf NRZ both have variable byte repetition rate (*data variability*).

Some of the bit-encoding techniques synchronize on transitions that fall on or within the bit boundaries. 10-bit NRZ, Bit-Stuf NRZ, and E-MAN all employ added transitions for synchronization (*clock synchronization*).

TABLE 26.1 Comparison of Multiplexing Bit-Encoding Techniques

	PWM	VPWM	10-Bit NRZ	Bit-Stuf NRZ	L-MAN	E-MAN	MFM
Variable	No	Yes	No	Yes	No	No	No
Synchronizing	Yes	Yes	No	No	Yes	No	Yes
Arbitrates	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Transition/bit	2	1	≤1.25	≤1.015	≤2	≤1.25	≤1
Max data rate	7.1 K	11.2 K	13.5 K	16.6 K	8.4 K	13.5 K	16.8 K
dBV < PWM	Base	9	11	14	5	11	15
Oscillator tolerance	±29.2%	±29.2%	±5.1%	±9.7%	±29.2%	±9.7%	±10.7%
Integrity	Perfect	Good	Fair	Fair	Perfect	Fair	Superb

All of the encoding techniques considered are capable of bit-by-bit arbitration. This is not commonly recognized with some of the encoding techniques, e.g. MFM, and will be addressed in Sec. 26.2.7 (*arbitrates*). Bit-by-bit arbitration is calculated on the number of *transitions per bit* of data.

A suitable data-encoding technique should not generate excessive levels of EMI, and this consideration is a dominating challenge in making an encoding choice. The CISPR Standard* is usually considered adequate. This factor determines the *maximum allowable data rate* of the encoding technique, in order to maintain a level of EMI below the CISPR standard break point, i.e., –60 dBV at 500 kHz. The values predicted in Table 26.2 used the same technique described in the next section.

Equation (26.1) in Fig. 26.10 can be used to predict[5] the EMI levels radiated by a single wire in a vehicle wiring harness. The technique was used to calculate and plot a Fourier series of a sample trapezoid wave to determine the values given in Table 26.2. The calculations assumed a 10.4 Kbps data rate at a 42 percent factor of the minimum feature size (minimum pulse width) to determine the rise time. Consider the trapezoidal wave shown in Fig. 26.10. The shortest rise time (42 percent of shortest pulse width), shortest pulse time, and fastest repetition rate should yield the worst-case EMI in dBV. The actual measured EMI will be a few dBV better than the calculated dBV because the output driver frequency bandwidth does act as a low-pass filter [EMI below PWM (dBV < PWM)].

* CISPR/D/WG2 (Secretariat) 19 Sept 1989 Radiated Emissions Antenna & Probe Test Document has been generally interpreted by most RF engineers to specify a break point at 500 kHz of –60 dBV.

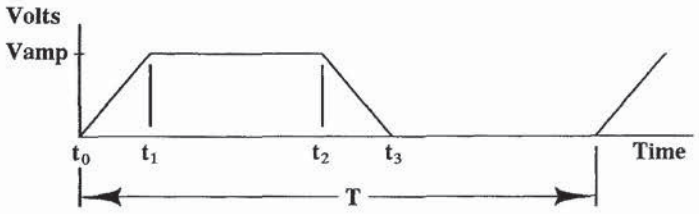


FIGURE 26.10 Trapezoidal wave shaping.

$$\omega_1 = \frac{2 \cdot \pi}{T}$$

$$\text{freq} = \frac{n}{T} \qquad \text{where } n \text{ is an integer}$$

$$a = n \cdot \omega_1 \cdot t_1$$

$$b = n \cdot \omega_1 \cdot t_2$$

$$c = n \cdot \omega_1 \cdot t_3$$

$$\Re = \frac{-1}{t_1} + \frac{Cos(a)}{t_1} + \frac{Cos(b) - Cos(c)}{t_3 - t_2}$$

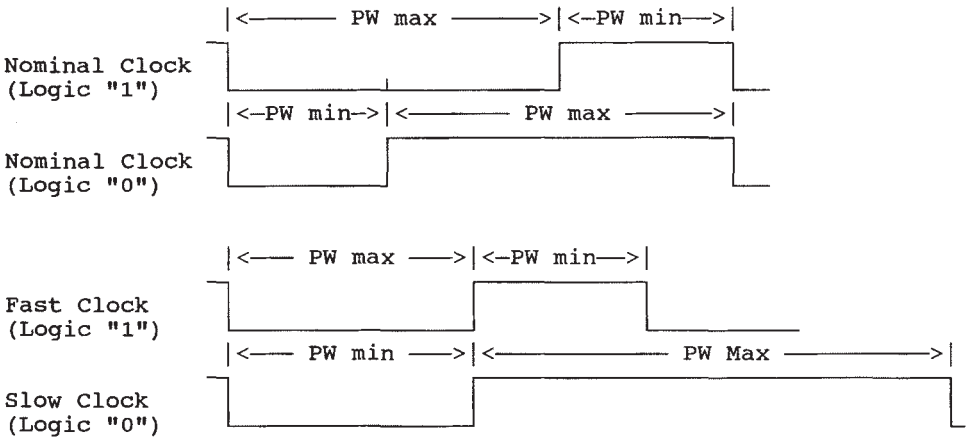
$$\Im = \frac{-Sin(a)}{t_1} + \frac{Sin(c) - Sin(b)}{t_3 - t_2}$$

$$MAG = 20\log \frac{Vamp \cdot T}{(2 \cdot n \cdot \pi)^2} \sqrt{R^2 + F^2} \qquad (26.1)$$

There are a number of hardware constraints that affect network synchronization and *oscillator tolerance.* The values given in Table 26.2 are calculated without considering these constraints because they are not generally considered a factor for evaluating encoding techniques. For all encoding techniques, the same nominal bit rates or average bit rate, as in the case of VPWM, was used. The small decrease in data rates for 10-Bit NRZ, Bit-Stuf NRZ, and E-MAN, due to the added bits for synchronization, is normally neglected; i.e., Baud rate was used.

The technique used by the receiver to detect a synchronizing transition plays a role in determining oscillator tolerance. Many different sampling or integration techniques could be used for a comparison, but for the sake of obtaining a reasonable judgment, for the encoding techniques under consideration, a very simple pulse width counter technique was assumed. A 12.5 percent of minimum pulse width (PW min) was assumed for variability in integration time (IT). The maximum time for synchronization was either the maximum pulse width (nominal) or time (nominal) between synchronization transitions.

Equation (26.2) in Fig. 26.11 yields the natural oscillator tolerance for the encoding technique. Figure 26.11 illustrates the maximum fast clock and minimum slow clock that can determine the logic value, either a "1" or a "0", for the symbol decoded by the symbol decoder. The IT is the time of uncertainty in determining the pulse width. The example demonstrated is for PWM encoding technique. All the other encoding techniques follow the same method. The actual tolerance would be affected by the application and the specific hardware used in the network. The variabilities introduced by the specific hardware will be needed to adjust parameters in Eq. (26.2) in order to find the final node oscillator tolerance.



$$Tol\% = \frac{PW\,\max - PW\,\min - IT}{PW\,\max + PW\,\min} * 100 \qquad (26.2)$$

FIGURE 26.11 Example of oscillator tolerance calculations.

There are generally three types of oscillators used with vehicle multiplex circuits: quartz crystal for very tight oscillator tolerances; ceramic resonators for low-cost, tight tolerances and fast startup time; and RC oscillators for very low cost and very fast startup time at a very loose oscillator tolerance.

The noise filter used is usually a digital filter or some type of sampling process. RC filters are usually not used because they are not precise enough. For all of the encoding techniques, a 12.5 percent of minimum pulse width was used for IT in calculating the oscillator tolerance.

In a single-wire network, ground offsets between nodes cause an added received pulse-width variability. This condition is especially acute when trapezoidal waveforms are used to reduce EMI. Figure 26.12 illustrates the pulse-width timing (T) variability introduced by ground offset. This pulse-width variability must be accounted for because it causes a reduction in minimum pulse width and an increase in maximum pulse width, thus having the effect of reducing oscillator tolerance.

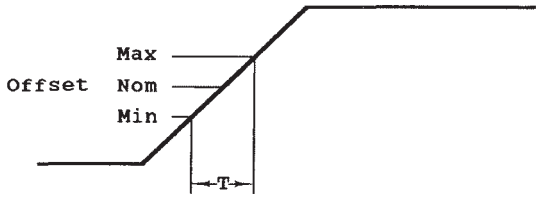


FIGURE 26.12 Ground offset on pulse-width timing.

The output drivers are the source of another pulse-width variability. The effect is the same as with ground offset only not nearly as acute. The problem is caused by line drivers used to permit arbitration having a longer delay time when going from the active to passive state than from a passive to active condition.

Data integrity is judged on a scale from poor, fair, good, superb, to perfect. Data integrity is generally considered to be affected by the EMI. The ambient levels of EMI in a vehicle are very low. This condition must remain in order to operate a communications receiver (consumer radio) in a vehicle. The problem is that very high levels of "bursty" noise for a short period at random intervals can completely disrupt multiplex communications for the duration of the noise. The only other effect of this bursty noise is a barely noticeable pop in the radio speaker. During these events, data integrity is compromised. The accepted practice for data communication (Class B) multiplexing is to simply detect this data corruption and throw out the full message rather than try to recover the data. This practice is acceptable because the amount of corrupted data compared to noncorrupted data is considered negligible, and/or can be retransmitted without causing bus bandwidth problems.

A thorough noise immunity study is very complex, and the criteria for judging would consider many factors. If something is known about the noise environment and the detector hardware, as is the case with the automotive situation, a study of data integrity may be useful. For the purpose of this discussion, assume that the criteria for judging which data-encoding method is acceptable is mainly dependent on its natural ability to detect corruption. Also, the corruption detection ability is often determined by the interface hardware capability and its message-handling protocol.

A number of validation tests can be performed on the message level. Bit-error algorithms such as a parity bit, checksum, or CRC are the most common test. Also, some protocols can perform message length by either message type or defining the message length in the data. These and other message level tests are independent of the bit-encoding method and should not influence data integrity of the bit-encoding technique.

The natural ability of the encoding technique to detect corruption is known as invalid bit detection. Usually three types of data integrity factors are considered for vehicle multiplexing because the effects of EMI environment are basically known:

1. *Low pass filtering.* For this factor, the data bit is passed through a low pass filter, i.e., an integrator; the longer the shortest pulse duration, the more effective the filtering.
2. The bursty noise detection test checks for a short duration of EMI.
3. Two independent data bit tests confirm valid data. PWM, for example, has two unique sample periods per bit and both periods must complement each other.

26.2.1 Pulse-Width Modulation (PWM)

The PWM encoding technique[6] is composed of two sample periods or phases (T_1 and T_2) per bit, as shown by Fig. 26.13. PWM encoding has the advantage that the time per bit remains constant, but has the disadvantage of generating more EMI because it has two transitions per bit. This time per phase of PWM also affects the generated EMI noise and, to minimize the EMI effect, one phase time is usually defined to be two times the other phase time in duration.

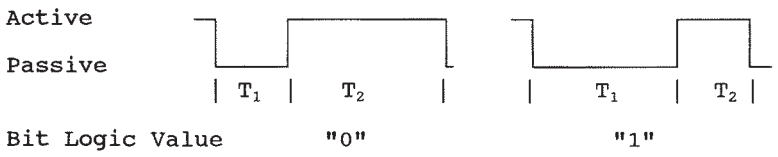


FIGURE 26.13 PWM encoded data.

Arbitration of PWM. PWM has the ability to perform bit-by-bit arbitration. Figure 26.14 illustrates that a "0" bit dominates and takes priority when bit-by-bit arbitrating over a logic "1".

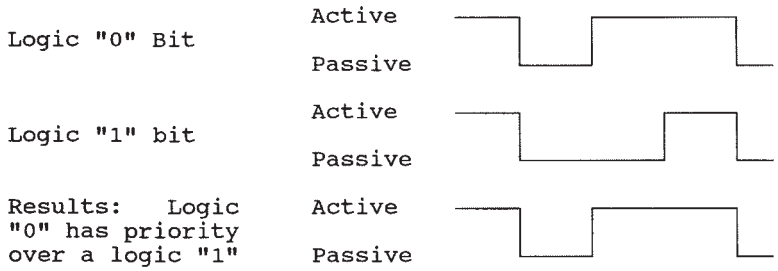


FIGURE 26.14 A logic "0" arbitrating with a logic "1".

Data Integrity of PWM. Consider a hardware sampler that has the capability of detecting (1) transition and (2) phase (ϕ) every sample window, as shown in Fig. 26.15. The sampler starts sampling at a transition, then sequentially samples window 1, window 2, and then window 3. If a transition is not detected by window 3, then data has been corrupted and the message is thrown out. When this type of sampler is used for PWM encoded data the sampler would sample five windows per bit and yield dual transition and phase information per bit. The transition and

Window	1	2	3
Error	$1 + \phi$	X	X
Short	0	$1 + \phi$	X
Long	0	0	$1 + \phi$

FIGURE 26.15 A three-window sampler.

phase information must be consistent for a correct PWM encoded data or corruption would be assumed and the message will be thrown out. If at any time a transition of either phase is detected in sample window 1, the data has been corrupted and the message is thrown out.

PWM encoding is judged to have very good "perfect" invalid bit-testing capabilities even though the effectiveness of the low-pass filter is poor. Otherwise, it has two of the three (e.g., dual periods confirmation of data and burst noise) validation tests. PWM is "perfect" encoding technique used in vehicle multiplexing when data integrity has the highest priority. However, this encoding technique has multiple transitions per bit and would not allow operation at data rates near the natural EMI limits for single-wire or twisted pair transmission media.

26.2.2 Variable Pulse-Width Modulation (VPWM)

VPWM (sometimes referred to as VPW modulation) is a variation of PWM. Normal PWM has two phases per bit as shown by Fig. 26.16. T_1 is illustrated as a passive short and T_2 as an active long. This combination is defined as a logic "0" bit. Notice that a logic "0" bit takes priority when arbitrating over the opposite pattern of a passive long and an active short.

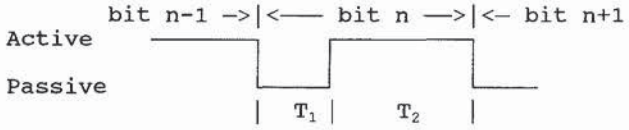


FIGURE 26.16 A PWM encoded logic "0" bit.

One of the most attractive features of VPWM is that the pulse-width variability introduced by factors such as ground offset and output driver timing variabilities can be added to the pulse-width timing without severely reducing the oscillator tolerance.

Arbitration of VPWM. VPWM encodes each phase as a data bit. Figure 26.17 illustrates a passive short arbitrating with a passive long. Figure 26.18 illustrates an active long arbitrating with an active short. In both cases, a logic "0" takes priority over a logic "1" bit. Therefore, arbitration using VPWM data encoding can be achieved.

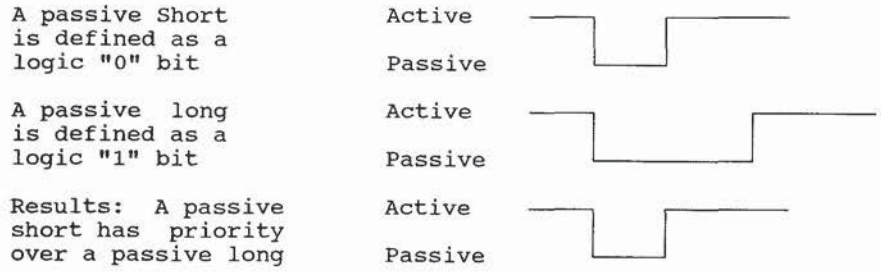


FIGURE 26.17 A passive short arbitrating with a passive long.

VPWM is utilized by SAE J1850; i.e., it uses a pulse width of 64 μs for a short and 128 μs for a long and approximates the same average data rate (10.4 Kbps) as regular PWM using a pulse width of 32 μs for a short and 64 μs for a long. The VPWM minimum pulse width for a short is 64 μs and permits a rise time of 16 μs for T as illustrated in Fig. 26.12. Compare this rise time to conventional PWM where a 32-μs short permits only an 8-μs rise time. The result of the proportionally longer rise time and wave shaping is an approximate 9-dBV improvement in EMI over PWM. The disadvantage of VPWM encoding is that the data rate per byte

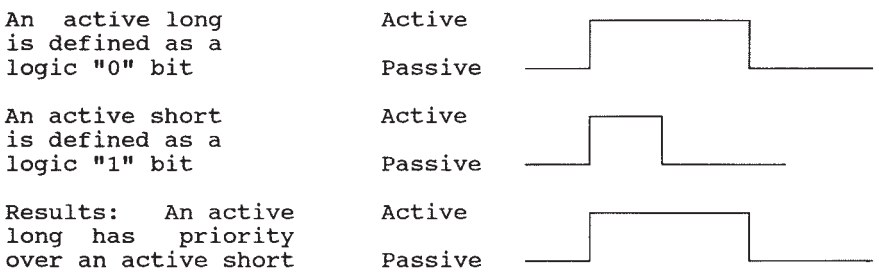


FIGURE 26.18 An active long arbitrating with an active short.

transmitted will vary in time depending on the data value. The microcomputer interfacing transmitter/receiver polling rate with VPWM is required to be less than ≈ 512 μs per byte, whereas with PWM, less than ≈ 768 μs per byte is required.

Data Integrity of VPWM. VPWM has good data integrity by sampling up to three times every pulse width as shown in Fig. 26.15. The sampler is designed to detect a transition and phase (ϕ) every sample window and have an average number of 2.5 samples per bit. If at any time a transition of either phase is detected in sample window 1, the data has been corrupted and the message is thrown out.

The sampling sequence is initiated by a transition of either phase. A short symbol is then sensed by not detecting a transition (0) in window 1 and detecting a transition ($1 + \phi$) and proper phase in window 2. Sampling in window 3 is a "don't care" (X), because sampling is terminated and the procedure is repeated. Window 3 is actually window 1 on the next sampling sequence.

A long symbol is likewise sensed by not detecting a transition (0) in window 1 or 2 and detecting a transition ($1 + \phi$) and proper phase in window 3.

The proper phase detection, when a transition is sensed, is used to ensure that the sequence does not get scrambled. It is also used to define which logic level, "1" or "0", has been received.

VPWM has been judged to have "good" data integrity because low-pass filtering of the data pulse width is good. Every transition is validated by an error-sampling window, and pulse duration measurements are validated by the proper phase test, i.e., two of the three invalid bit tests.

26.2.3 Standard 10-Bit NRZ

This is an asynchronous serial I/O (standard UART) 10 bits-per-byte of data. A start bit and a stop bit are added to provide data byte synchronization. The standard UART used in RS232 is bit-ordered least significant bit (LSB) first. Figure 26.19 illustrates this 10-bit NRZ waveform. Vehicle multiplex networks that use 10-bit NRZ make use of the available hardware that have this asynchronous I/O, i.e., the serial communications interface (SCI) available on many microcomputers.

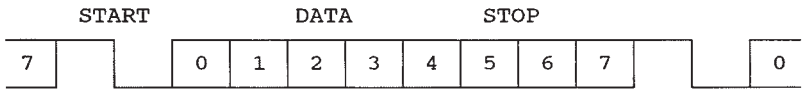


FIGURE 26.19 A 10-bit NRZ waveform (LSB first).

Arbitration of 10-Bit NRZ. Figure 26.20 illustrates 28H from transmitter #1 arbitrating with 44H from transmitter #2. An active "0" is defined to win arbitration over a passive "1". Take note that bus has a 28H on it and, therefore, transmitter #2 shuts off its output when it tries to transmit bit #2. This loss of arbitration action is the usual method employed by all arbitrating protocols.

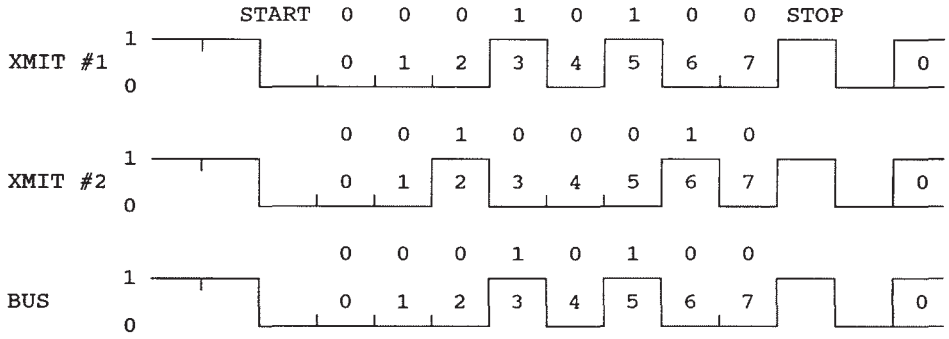


FIGURE 26.20 Arbitration of a 10-bit NRZ network.

Data Integrity of 10-Bit NRZ. The bit-synchronized sampling technique used for PWM and VPWM could be used for 10-bit NRZ encoded data, but it would be much more complex because it could be guaranteed to synchronize only on the stop-to-start transition. It would not sample only one bit, it may have to sample all eight. The normal technique is to use a start bit detector to sense a valid start bit and then sample all eight of the data bits sequentially.

As with all decoding techniques, the data is passed through a low-pass filter. However, filtering for NRZ is very effective because of the long data pulse duration. 10-bit NRZ encoding has been judged to have "fair" data integrity, mainly because the addition of a transition between the stop bit and start bit is not unique in the sequence and the detector hardware could get scrambled. Adding an invalid bit detection for bursty noise between data bits would improve the data integrity, but it could not validate every bit.

26.2.4 Bit-Stuf NRZ

Bit-stuffing is another way of synchronizing NRZ encoded data. The concept is to insert a bit (i.e., two transitions) after a specified number (X) of bits of contiguous "1" or "0" bits and if the X + 1 bit is the same logical value as the other contiguous bits. The proper number of contiguous bits is chosen as a compromise between the oscillator tolerance and the generated EMI. The higher the number of contiguous bits before inserting a stuff-bit, the better the synchronizing oscillator tolerance must be, but the lower the EMI. There is also a receiver decoding complexity consideration with bit-stuf NRZ. Figure 26.21 illustrates waveform used by CAN for X = 5.

The number of stuff-bits in a frame is dependent on the data value, and the transmission time for a data byte is a variable quantity depending on this data value. A number of the factors used to evaluate bit-stuf NRZ require a knowledge of the average number of data bytes per stuff-bit (see Fig. 26.22). This average number can be derived because the nature of a data bit in a message has equal probability of being a "1" or "0".

Arbitration of Bit-Stuf NRZ. As with all arbitrating encoding methods, the bit-stuf NRZ transmitter utilizes a driver that has an active state and a passive state, thereby supporting bit-by-bit arbitration.

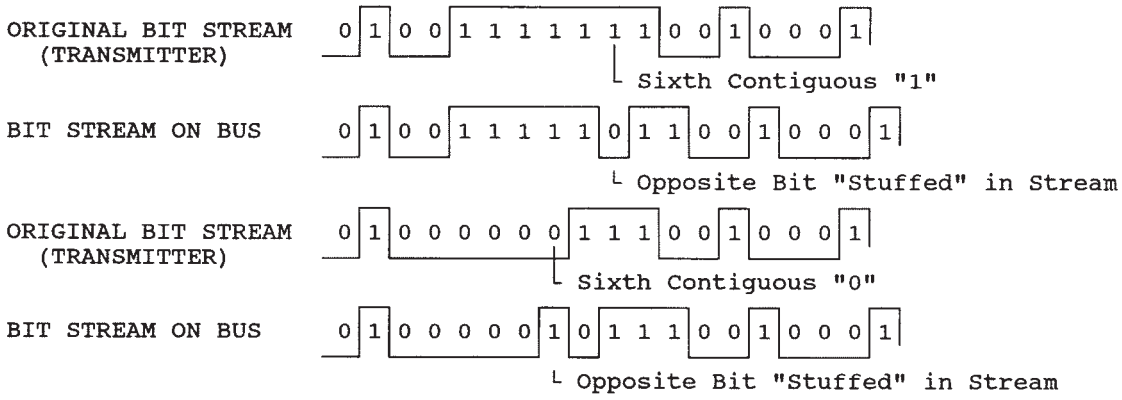


FIGURE 26.21 NRZ bit-stuffing.

The probability of there being a stuff-bit before B_i in the stuffing algorithm where X = 5 is as follows:

$$B_0,\ B_1 \bullet\ \bullet\ \bullet\ B_i \bullet\ \bullet\ \bullet\ B_{n-1}$$

$$p_i = \begin{cases} 0 & when\ i < 5 \\ 1/32 & when\ i = 5 \\ 1/64 & when\ i > 5 \end{cases}$$

$$F(N) = No.\ of\ BYTES/STUF$$

$$F(N) = \frac{N}{\sum_{i=0}^{n-1} p_i} \quad where \quad n = No.\ of\ Bits, \quad N = \frac{n}{8} = No.\ of\ Bytes$$

$$\lim_{N \to \infty} F(N) = 8$$

$$F(12) = 8.348$$

FIGURE 26.22 Derivation of average number of stuff-bits.

Data Integrity Bit-Stuf NRZ. The bit-synchronized six-window sampling technique illustrated in Fig. 26.23 could be used for bit-stuf NRZ encoded data and would be guaranteed to synchronize on the stuff-bit. It must accommodate sampling from one to five data bits sequentially. All bits of data prior to sampling a transition are assigned the same logic level as the level detected by transition and phase detector. If transition is detected in window #1, which is due to bursty noise, the message would be thrown out. This detector could somewhat improve the data integrity, but it could not validate every bit. As with all decoding techniques, the data is passed through a low-pass filter. However, filtering for NRZ is very effective because of the long data pulse duration.

Bit-Stuf NRZ encoding has been judged to have "fair" data integrity, mainly because the addition of a synchronizing stuff bit is not unique in the sequence and the detector hardware could get scrambled.

Window	1	2	3	4	5	6
Data		D_n	D_{n+1}	D_{n+2}	D_{n+3}	D_{n+4}
Error	$1+\phi$	X	X	X	X	X
Bit 1	0	$1+\phi$	X	X	X	X
Bit 2	0	0	$1+\phi$	X	X	X
Bit 3	0	0	0	$1+\phi$	X	X
Bit 4	0	0	0	0	$1+\phi$	X
Bit 5	0	0	0	0	0	$1+\phi$

FIGURE 26.23 A six-window sampler.

26.2.5 L-Manchester (L-MAN)

The L-MAN encoding technique is composed of two sample periods of opposite phases per bit, as shown by Fig. 26.24. L-MAN encoding has the advantage that the time per bit remains constant, but has the disadvantage of generating more EMI because it can have an average of one-and-a-half and maximum of two transitions per bit.

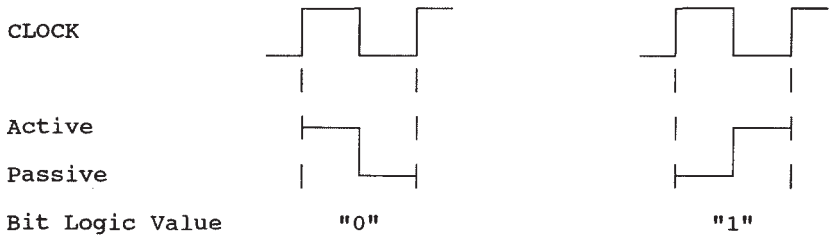


FIGURE 26.24 L-MAN encoded synchronizing bits.

A transition from active to passive level will be decoded as a logic "0" and a transition from passive to active level will be decoded as a logic "1". A synchronizing transition is always generated in the center of the bit period but may not be generated at the beginning of a bit period, depending on the data. As illustrated by Fig. 26.25, when there is a "0" to "1" or "1" to "0" data sequence the transition is not generated.

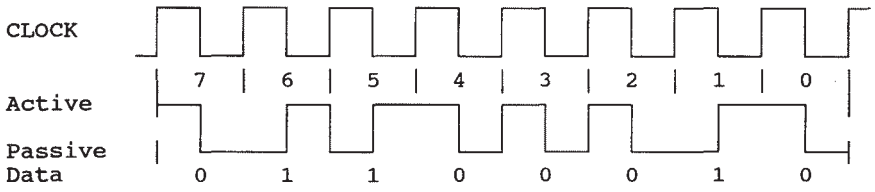


FIGURE 26.25 One byte of L-MAN encoded data.

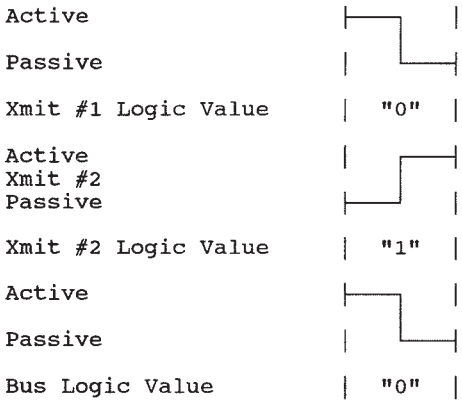


FIGURE 26.26 A logic "0" arbitrating with a logic "1".

Arbitration of L-MAN. Figure 26.26 illustrates how a logic "0" arbitrating with a logic "1" always wins arbitration. This situation is true because the active portion of the signal overrides the passive portion and also shuts off the output of the passive contender before it would become active.

Data Integrity of L-MAN. Consider a three-window sampler that has the capability of detecting a transition (1) and phase (ϕ) every sample window as shown in Fig. 26.15. The circuit starts sampling at a transition and then sequentially samples window 1, window 2, and then window 3. If a transition is not detected by window 3, then data has been corrupted and the message is thrown out. When this type of sampler is used for L-MAN encoded data, the sampler would sample four to five windows per bit and yield complementary transition and phase information per bit. If D_n and D_{n+1} have the same logic level—i.e., "1s" or "0s"—then a transition must not occur at the bit boundary or a corrupted data would be assumed and the message will be thrown out. If at any time a transition of either phase is detected in sample window 1, the data has been corrupted and the message is thrown out.

L-MAN encoding is judged to have very good "perfect" invalid bit-testing capabilities even though the effectiveness of the low-pass filter is poor. Otherwise, it has two of the three validation tests: dual validation of data by proper periods at the bit boundary and bursty noise test every bit. L-MAN has "perfect" encoding technique used in vehicle multiplexing when data integrity has the highest priority. However, this encoding technique has multiple transitions per bit and would not allow operation at data rates near the natural EMI limits for single-wire or twisted pair transmission media.

26.2.6 E-Manchester (E-MAN)

E-Manchester, or enhanced manchester, utilizes an L-Manchester encoded data bit for synchronization combined with three bits of NRZ encoded data bits. Figure 26.24 illustrates the L-Manchester synchronizing bit values and Fig. 26.27 is an illustration of four bits of E-MAN encoded data.

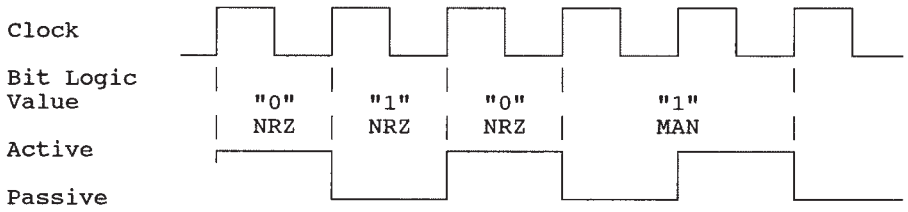


FIGURE 26.27 Four bits of E-MAN encoded data bits.

Arbitration of E-MAN. When arbitrating, an active (logic "0") takes priority over the opposite pattern (logic "1") for both the NRZ bits and the MAN encoded synchronization bit. This domination of a logic "0" over a logic "1" is easily understood for the NRZ encoded

portion of an E-MAN encoded byte. The dominance of a logic "0" synchronization bit, which seems confusing, can be easily realized by considering the fact that the active portion of the signal overrides the passive portion and also shuts off the output of the passive contender before it would become active.

The main advantage of E-MAN over PWM or VPWM is that the shortest pulse width at 10.4 Kbps is ≈ 76.8 μs, and permits a 42 percent rise time of 32.3 μs compared to a 32 μs short and 13 μs rise time with conventional PWM. The result of the proportionally longer rise time and wave shaping is an approximate 11-dbV improvement in EMI over PWM. Another advantage of E-MAN over VPWM is that the data rate per byte transmitted is constant. The microcomputer transmitter/receiver polling rate with E-MAN is required to be a constant of less than ≈ 768 μs per byte.

Data Integrity of E-MAN. If the same sampling technique is used for E-MAN as was used for the bit-stuf NRZ case, it is capable of detecting (1) a transition and (2) a phase (ϕ) every sample window. The E-MAN sampling hardware can sample up to six times every pulse width as shown in Fig. 26.23.

The sampling sequence is initiated by a transition of either phase. If there is a transition (1 + ϕ) in window 2, then the value of D_n is determined by the logic level and phase.

If there is a transition (1 + ϕ) in window 3 in the sampling sequence, then $D_n = D_{n+1}$ and is determined by the logic level and phase. If there is a transition (1 + ϕ) in window 4 in the sampling sequence, then $D_n = D_{n+1} = D_{n+2}$ and is determined by the logic level and phase.

If there is a transition (1 + ϕ) in window 5 in the sampling sequence, then $D_n = D_{n+1} = D_{n+2}$ and is determined by the logic level and phase. The value of D_{n+3} is determined by the phase (ϕ) because it is the L-MAN encoded bit and will be confirmed by a transition (1 + ϕ) in window 2 on the following sampling sequence.

If there is a transition (1 + ϕ) in window 6 in the sampling sequence, then $D_n = D_{n+1} = D_{n+2}$ and is determined by the logic level and phase. The value of D_{n+3} is determined by the phase (ϕ) because it is the L-MAN encoded bit.

The L-MAN encoded bit is not unique in the sequence and the detector hardware must keep track of where the L-MAN bit should be, because if a transition (1 + ϕ) for the L-MAN encoded bit falls in a window other than window 6, then the value of D_{n+3} is determined by the phase (ϕ) of the transition.

E-MAN encoding has been judged to have "fair" data integrity, mainly because the L-MAN encoded bit is not unique in the sequence and the detector hardware could get scrambled. If a transition is detected in window 1, an invalid bit was detected, which helps data integrity but it could not validate every bit. As with all decoding techniques, the data is passed through a low-pass filter. However, filtering for E-MAN is very effective because of the long data pulse duration.

26.2.7 Modified Frequency Modulation (MFM)

Modified frequency modulation (MFM), a modulation technique developed during the latter 1960s, was used in disk drives and is adaptable to vehicle multiplexing. The advantage of using the MFM encoding technique is that it would be synchronous with an average of 0.75 and a maximum of 1 transition per bit. The encoding technique permits a transition rise time that can be maximized and wave-shaped to significantly reduce EMI. Disk drives have a similar requirement where the modulation technique allows pulses to be recorded on a disk at maximum density. The diagram shown in Fig. 26.28 demonstrates one method of applying MFM encoding technique to a data communication network.

The rule for encoding simply causes a transition at the data time when the data at that time slot is a logic "1". A transition is also generated at the clock time slot when the data before and after the time slot was a logic "0" (or two "0"s in a row).

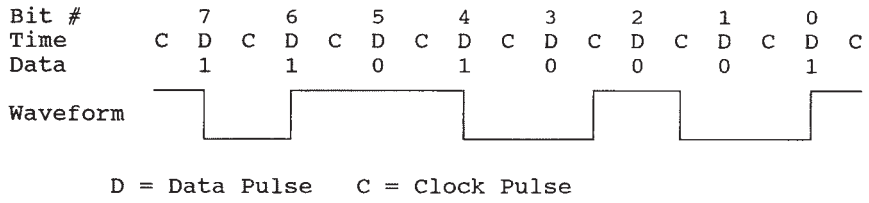


FIGURE 26.28 MFM encoded byte of data.

Arbitration of MFM. A requirement for vehicle multiplexing is that the data from one device shall bit-by-bit arbitrate with the data from another device. The arbitration bit-ordering is defined MSB first, and 00H has the highest priority. To support arbitration, the output driver is defined and designed to have an active state that has priority over a passive state. Figure 26.29 demonstrates the four encoding rules that can be used to generate a waveform "A" that always wins arbitration.

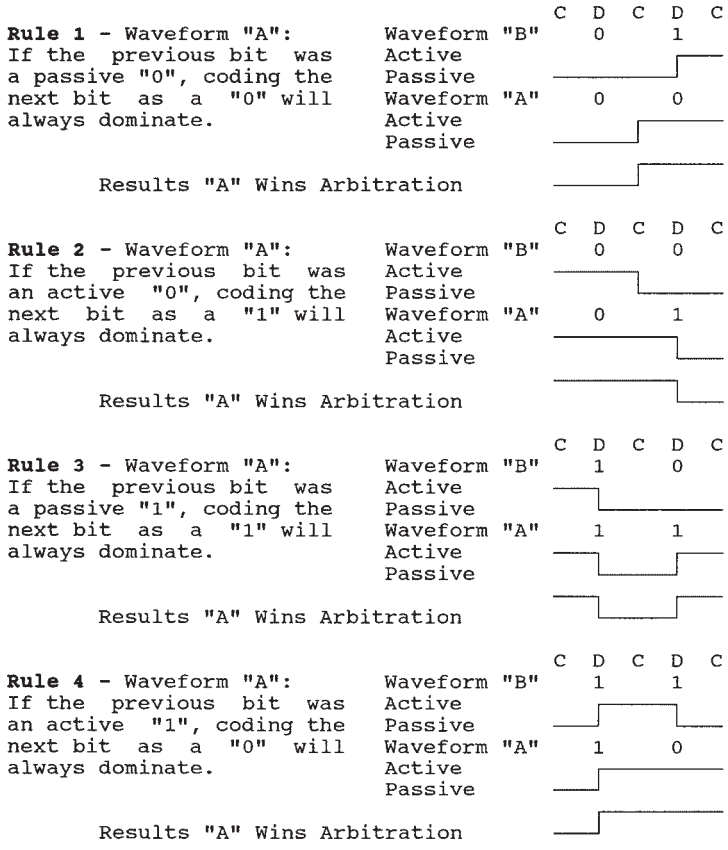


FIGURE 26.29 The four rules for winning arbitration.

Assume that the existence of four rules for winning arbitration demonstrates that it is possible to convert data into a form that will correctly arbitrate. This assumption means that data can be encoded into a different byte, which will have to be decoded back after arbitration. Applying the four rules, the process required to code a "0" in the original byte to win, and a "1" to lose, is: start with the MSB, move toward the LSB, i.e., left to right. When encoding, make sure all the "0s" encountered are of the type that will win arbitration, i.e., Rule 1 and 4. When a "1" is encountered make sure the type of "0" that will be following the previous bit will win arbitration over the "1" in the present bit, i.e., Rule 2 and 3. For each "1" encountered in a row, make sure the other byte that has the same bits up to that point, but now has a "0", will win arbitration with that "0".

Encoding and decoding of data into an MFM format can be accomplished by hardware in the interface circuit. A two-step process is required. First the data bytes to be transmitted must be translated into the correct form for arbitration using the rules illustrated by Fig. 26.28. The operation of the MFM encoder depends on a starting value of a dominant "1", which is provided by the start of frame (SOF).

After the data is translated into the correct form for arbitration, it can be encoded by the circuit. The data is then ready to be transmitted by the I/O. The received data requires the reverse sequence of first decoding by the circuit and then translation into the correct binary form. Translation can be accomplished by the circuit.

Data Integrity of MFM. The MFM encoding receiver samples up to four times every pulse width when starting at a data transition, and up to three times every pulse width when starting on a clock, as shown in Fig. 26.30.

Window	1	2	3	4
Clock	D_n	C	D_{n+1}	
Data	C	D_n	C	D_{n+1}
Error	$1+\phi$	X	X	X
Bit 1	0	$1+\phi$	X	X
Bit 1½	0	0	$1+\phi$	X
Bit 2	0	0	0	$1+\phi$

FIGURE 26.30 MFM data integrity capability.

The sampling sequence is initiated by a transition of either phase. The sampler can detect a transition $(1 + \phi)$ of either phase in every sample window. The following sequences begin with a transition in a data window:

1. If next $1 + \phi$ in data window 1, then an error has been detected.
2. If next $1 + \phi$ in data window 2, then the value of $D_n = 1$.
3. If next $1 + \phi$ in data window 3, then the value of $D_n = 0$ and $D_{n+1} = 0$.
4. If next $1 + \phi$ in data window 4, then the value of $D_n = 0$ and $D_{n+1} = 1$.

The following sequences begin with a transition in a clock window:

1. If next $1 + \phi$ in clock window 1, then an error has been detected.
2. If next $1 + \phi$ in clock window 2, then the value of $D_n = 0$ and $D_{n+1} = 0$.

3. If next 1 + ϕ in clock window 3, then the value of $D_n = 0$ and $D_{n+1} = 1$.
4. If next 1 + ϕ in clock window 4, then an error has been detected.

MFM has been judged to have very good ("superb") data integrity because, as with VPWM encoding, every transition is validated by an error-sampling window and a proper phase test. Also, when transitions fall in windows 3 and 4 for data and in 2 and 3 for clock, the value of two data bits is sensed. One sampling confirms the previous, thus improving data integrity capability. With MFM decoding technique, the data is passed through a low-pass filter. However, filtering for MFM is very effective because of the long data pulse duration.

26.3 PROTOCOLS

Table 26.2 describes the protocol sections.[7] These descriptions appear in the order in which they are discussed for each protocol.

The following describes the *intent* of the various sections of the protocol characteristics.

The *application* section briefly identifies the applications for which the protocol was designed to serve: military, aircraft, industrial, land vehicles, and trucks. The *affiliation* section identifies the organization(s) that originally developed the protocol, specified the protocol, or which now endorse the protocol.

The *transmission media* section describes the physical medium generally associated or required by the given protocol: single-wire, dual-(parallel) wire, twisted pair, twisted pair with shield, dual twisted pair, and fiber optics.

The *physical interface* section describes the basic circuitry used to connect the nodes to the network. In some cases, the schematic of a typical interface may be shown. In others, a reference to a generally known interface technique may be made. This section may also include additional data about aspects of the interface not readily shown. An example would be that receiver nodes synchronize to the signal from a transmitting node, or that receiver nodes adjust their receiver clock to the received data signal.

The *bit encoding* section describes the way in which the logical bits, "1"s and "0"s, are translated into signals on the transmission medium by the physical interface (NRZ, PWM, and MANCHESTER).

The *network access* section describes the method used to award the communication network to one of the nodes for the transmission of a message: master/slave, token passing, and CSMA/CD.

The *message format* section describes the fields that make up the basic message(s) used in the protocol. This includes the order, name, and size of the fields.

The *handshaking* section describes the interaction of nodes within a network in order to effect a transfer of data. This may include such things as negative and positive acknowledgment, and in-message acknowledgment.

The *error detection management* section describes the types of errors the protocol detects and the recovery techniques it uses: wrong message length and CRC.

The *fault tolerance* section describes the ability of the protocol to continue operation, possibly at a degraded level, when various parts of the physical layer or medium of the network on which the protocol is operating fails (i.e., node connections are broken, bus wires are opened, bus wires are shorted to ground or to vehicle battery voltage).

The *data rate* section identifies the maximum data rate supported by the protocol.

The *framing overhead* section briefly shows the amount of nondata overhead, i.e., framing overhead, associated with the given protocol. If possible, the calculation of overhead is shown. Because some protocols offer significantly different message formats and/or message sizes, several overhead calculations may be necessary to give an accurate picture of the range of the protocol's overhead requirements.

TABLE 26.2 Protocol Descriptions

	A-BUS	CAN	D2B	SAE J1567 C^2D	SAE J1850 PWM	SAE J1850 VPWM	SAE J2058 CSC	SAE J2106 token slot	TTP	VAN
SAE class		Class B & C		Class B	Class B	Class B	Class A	Class C	Class C	
Affiliation	VW	Proposed ISO Bosch	Philips	Chrysler	SAE RP Ford	SAE RP Chrysler, GM	Chrysler	GM	University Wien Austria	Proposed ISO
Application	Auto in-vehicle	Auto in-vehicle	Audio/video	Auto in-vehicle	Auto in-vehicle	Auto in-vehicle	Auto in-vehicle	Auto in-vehicle	Auto in-vehicle	Auto in-vehicle
Transmission media	Single-wire	Twisted pair/ fiber optic	Twisted pair	Twisted pair	Twisted pair	Single-wire	Single-wire	Twisted pair/ fiber optic	Twisted pair/ fiber optic	Twisted pair
Bit-encoding	NRZ	NRZ with bit-stuffing	PWM	10-bit NRZ	PWM	VPWM	Analog, NRZ, & PWM	NRZ with bit-stuffing	MFM	L-MAN E-MAN
Media access	Contention	Contention	Contention	Contention	Contention	Contention	Master/slave	Token slot	Time-triggered	Contention
Error detection	Bit only	CRC	Parity	Checksum	CRC	CRC	Parity	CRC	CRC	CRC
Data field length	2 bytes	0–8 bytes	2–128 bytes	1–6 bytes	0–8 bytes	0–8 bytes	1–32 bits	0–256 bytes	2–8 bytes	0–8 bytes
In-message acknowledge		Yes			Yes	Yes	Yes	Yes	Yes	
Maximum bit rate	500 Kbps	1 Mbps	100 Kbps	7.812 Kbps	41.6 Kbps	10.4 Kbps	1 Kbps	2 Mbps	1 Mbps	User definable
Maximum bus length	Not specified typical 30 m	Not specified typical >40 m	150 m	Not specified typical >30 m	40 m	40 m	Not specified typical >40 m	Not specified typical 30 m	Not specified typical 20 m	20 m
Maximum number of nodes	Not specified typical 32	Not specified typical >16	50	Not specified	Not specified	Not specified	Not specified	32 (transmit capability)	Not specified	16
Hardware available	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No	Yes

The *latency* section describes the factors that affect the delay between the availability of a message to be transmitted and the beginning of the reception of that message by the intended receiver.

The *power reduction* section has general information about any modes of operation that require less power than normal operation. As a minimum, this section identifies the lower power level(s). It also includes a brief description of the criteria used in transitioning to the lower power mode(s) and to return to normal power mode. Some of this information may be device-version-specific and will be so identified.

26.3.1 Automotive Bit-Serial Universal Interface System (A-BUS)

Application/Affiliation. Designed for automotive applications by Volkswagen AG.

Transmission Media. Not specified. Single-wire suggested.

Physical Interface. Not specified.

Bit Encoding. NRZ with eight samples/bit, which means each sample is ⅛th the length of the bit. A valid bit has to have either four or six complementary samples (see Fig. 26.31). This choice of either 4 or 6 matching samples is a user selectable function.

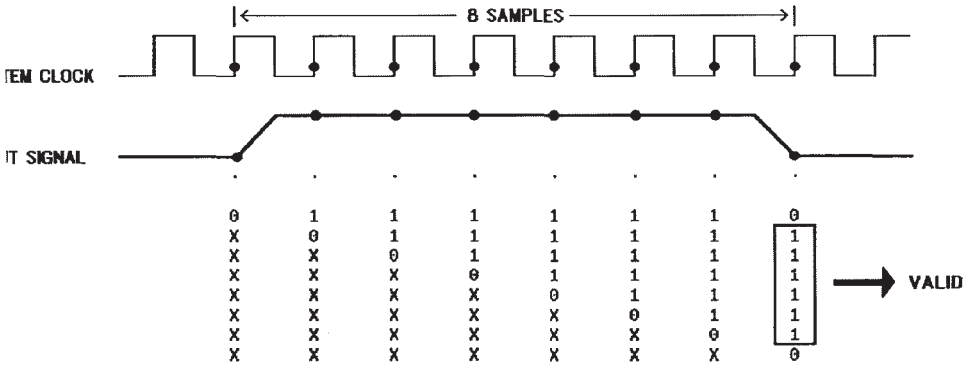


FIGURE 26.31 NRZ with eight samples/bit.

Network Access. Network access is achieved by a contention process that occurs through the end of the identifier field using a nondestructive bit-by-bit arbitration operation.

Message Format. Message length is constant and consists of 1 start bit, 1 bit (NC/DAT) indicating whether it is a data message or a command message, an 11-bit identifier, 16 bits of data, and 2 stop bits (STP0, STP1). Further detail is provided in Fig. 26.32. Two different types of messages are possible: the data message and the command message. Command messages may be used to ensure that a following command will not be accepted on the bus until the receiver has read the command. The ABUS IC can be programmed in a way that every following command will not be accepted on the bus until the master controller unit has read the command last received. In this case, no commands are lost.

Handshaking. Negative acknowledgment by receiver after error is detected. Any receiving device that notices a protocol error notifies all other bus members by pulling down the STP1

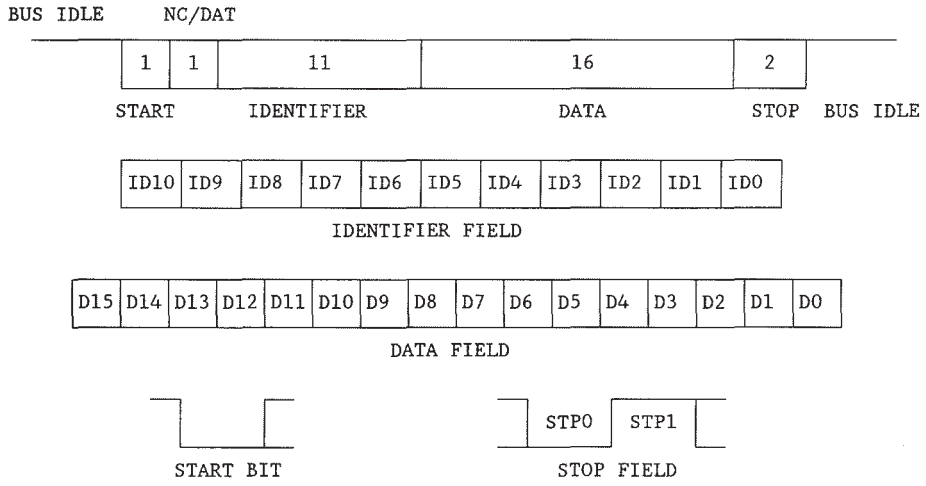


FIGURE 26.32 Message format.

bit. If the STP1 bit is low, the message is regarded as invalid by all members. There is no required or dedicated positive acknowledgment.

Error Detection Management. The transmitter and receiver monitor the bus for errors. The transmitter reads its own message back from the bus and compares it with the message that it intended to send. The receiver detects four different types of code errors by sampling the bus and when it has not been possible to compare the samples.

Start-Bit Error. This occurs when it has not been possible to generate a start bit at the beginning of the transmission process.

Transmit Error. A transmit error is monitored when, during a message transmission, the value read back was not equal to the value sent out a total of Y times* consecutively between the arbitration and STP1 bit.

Receive Error. A receive error is monitored when, during a message reception, an error has been detected a total of X times* consecutively prior to the STP1 bit.

Short Circuit. This occurs when no logical "1" has been read for a period of 256 clock pulses after a high to low transition.

Fault Tolerance. Not specified.

Data Rate. Maximum specified bit rate = 500 Kbps.

Framing Overhead. The message length is 31 bits; 16 of these are data. To transmit four bytes of data, two messages must be sent. Using the formula:

$$\frac{\text{OVERHEAD}}{\text{MESSAGE}} = \frac{\text{FRAMING}}{(\text{FRAMING} + \text{DATA})}$$

Approximate framing overhead/message calculated is: $(15+15)/((15+16)+(15+16)) = 48\%$.

* X and Y are programmable values (to 8, 16, and 32). In the present implementation, these error occurrences are stored in a status register and cause an interrupt. The sender tries to send a message for 8 to 32 times before it is recognized as an error.

Latency. The ABUS protocol uses nondestructive bit-by-bit arbitration in contention to determine bus access. In the case of two or more nodes beginning transmission simultaneously, the message with the highest priority will win the arbitration and continue transmission. As a result, the maximum latency for the highest priority message is the number of bits in the maximum length message multiplied by the time per bit. A 31-bit message will require 64 μs at 500 Kbps. Lower priority messages may encounter additional delay in the event that they lose arbitration. Their latency may be determined based on a statistical analysis of the system, bus load, priority, and other.

Power Reduction Mode. The power consumption of the ABUS IC can be reduced by using the sleep mode. In this mode, the oscillator is turned off and the power consumption is reduced to 10 to 100 μA. The sleep mode is initiated by the host microprocessor. The IC will wake up either by a reset or by bus activity, but will go through a reset in either case. After the reset it will take about 50 ms for the oscillator to work properly; e.g., the first message works as an "alarm clock," which implies it is not received completely.

26.3.2 Controller Area Network (CAN)

Application/Affiliation. Both standard (S) and extended (E) message formats are intended for automotive in-vehicle applications. An ISO draft standard and an SAE Information Report[8] have been published.

Transmission Media. Not specified. Most of the announced production-intent systems use a wire-shielded or unshielded bus. Fiber optic systems using CAN have been demonstrated.

Physical Interface. User defined. One specific implementation is defined in Bosch presentations and documents to ISO.

Bit Encoding. NRZ (Nonreturn to Zero) with bit-stuffing (see Fig. 26.33). Logic level is constant for entire bit field, i.e., either "1" or "0", and bit of opposite state is inserted into bitstream by a transmitter if five contiguous bits of the same state are seen. Receivers remove the inserted bit from the bitstream, resulting in restoration of the original data stream. Implementations are programmable to allow either three or one samples per bit and specify the location of samples within a bit.

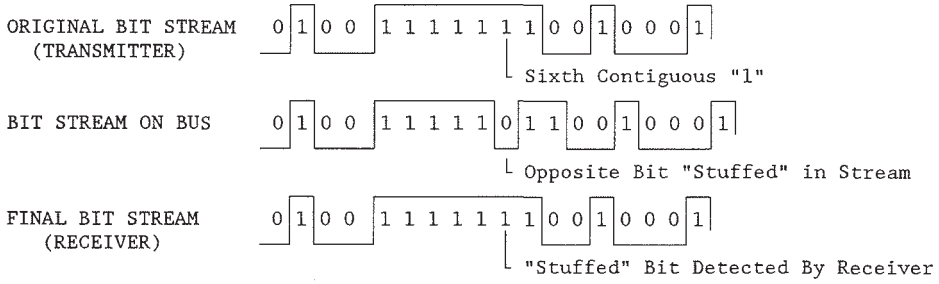


FIGURE 26.33 NRZ bit-stuffing.

Network Access. Contention using nondestructive bit-by-bit arbitration. Any node may transmit if the bus is idle. In the case of simultaneous transmissions, arbitration is resolved through the value in the identifier field. The message priority is defined in the identifier. Each message has a unique identifier, and, as a result, a unique priority. These identifiers/priorities are defined by the user, i.e., the system designer.

Message Format. There are primarily three message types: data frame (see Fig. 26.34), remote frame (see Fig. 26.35), error frame (see Fig. 26.36), and overload frame (used in events where individual node has not had complete time to store message, see Fig. 26.37).

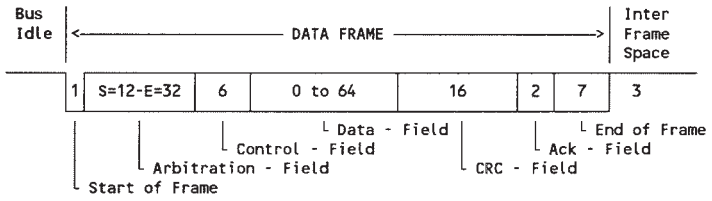


FIGURE 26.34 Data frame.

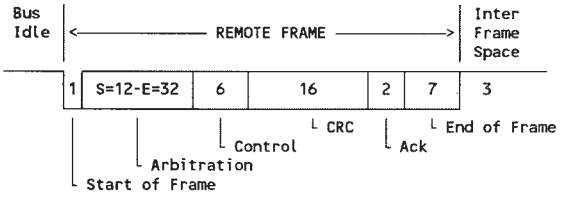


FIGURE 26.35 Remote frame.

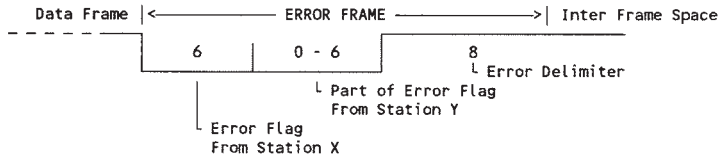


FIGURE 26.36 Error frame.

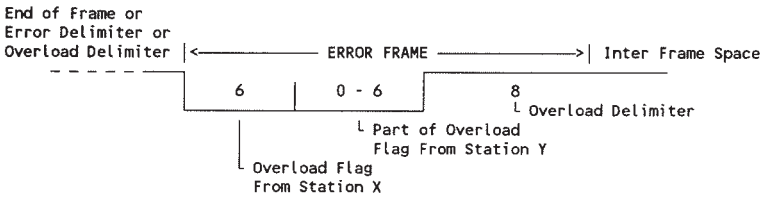


FIGURE 26.37 Overload frame.

Handshaking. Handshaking is provided within the message via either positive or negative acknowledgment. Positive acknowledgment is provided by a dedicated two-bit field in the message frame; one bit for acknowledgment and one bit for delimiter. All nontransmitting nodes will confirm uncorrupted message reception by transmitting a "dominant" bit in this dedicated field. As a result, the transmitting node receives confirmation that the message was received uncorrupted and does not have independent acknowledgments from individual nodes. Negative acknowledgment is provided through the error frame. See Fig. 26.34 for additional detail.

Error Detection Management. All nodes monitor all messages. If an error is detected within a message, then the node(s) detecting that error destroy that message by transmitting an error frame. The result of this error frame is that all nodes (including the transmitting node) know that an error has been detected within the present message. The transmitter will retransmit the message at its next opportunity through normal bus access arbitration. Error-checking is provided on CRC, message length, message format, and bit level and timing. The message length is specified in the control field.

Fault Tolerance. Protocol is intended to treat all node address faults in the same manner. Fault confinement is provided by each node constantly monitoring its performance with regard to successful and unsuccessful message transactions. Each node will act on its own bus status based on its individual history. As a result, graceful degradation allows a node transmitter to disconnect itself from the bus. If the bus media is severed or shorted, the ability to continue communications is dependent upon the condition and the physical interface used.

Data Rate. Bit rate of up to 1 Mbit/s.

Framing Overhead. Maximum message length, which is the maximum time between messages, is 111 bit times for standard format and 131 bit times for extended format, i.e., 111 and 131 μs at 1 Mbps. For the highest priority message, if a message has just begun and the message in question is queued up, the latency will be 111/131 μs, and 222/262 μs maximum until its transmission is complete.

The maximum time between messages with four bytes data is 79 bits for standard format and 99 bits for extended format. Please note that this includes interframe space. For a message transmitting four bytes of data, using the formula OVERHEAD/MESSAGE = FRAMING/(FRAMING + DATA), the approximate framing overhead/message calculated for standard format is 47/(47 + 32) = 59%. For eight data bytes, the approximate framing overhead/message calculated is 47/(47 + 64) = 42%. For extended format, it is 67/(67 + 32) = 68% and 67/(67 + 64) = 51%, and does not include bit-stuffing.

Latency. The CAN protocol uses nondestructive bit-by-bit arbitration in contention to determine bus access. In the case of two or more nodes beginning transmission simultaneously, the message with the highest priority will win the arbitration and continue transmission. As a result, the maximum latency for the highest priority message is the number of bits in the maximum length message multiplied by the time per bit. In other words, it will have 111 bit times or 111 μs at 1 Mbit/s for standard format and 131 bit times or 131 μs at 1 Mbit/s for extended format. In the event that they lose arbitration, lower priority messages may encounter additional delay. Their latency may be determined based on a statistical analysis of the system, i.e., bus load, priority, and other.

Power Reduction Mode. Not specified.

26.3.3 Digital Data Bus (D2B)

Application/Affiliation. Digital data bus is a product of Philips for use in audio/video communications, computer peripherals, and automotive.

Transmission Media

Twisted pair

Physical interface

Differential floating pair (see Fig. 26.38)

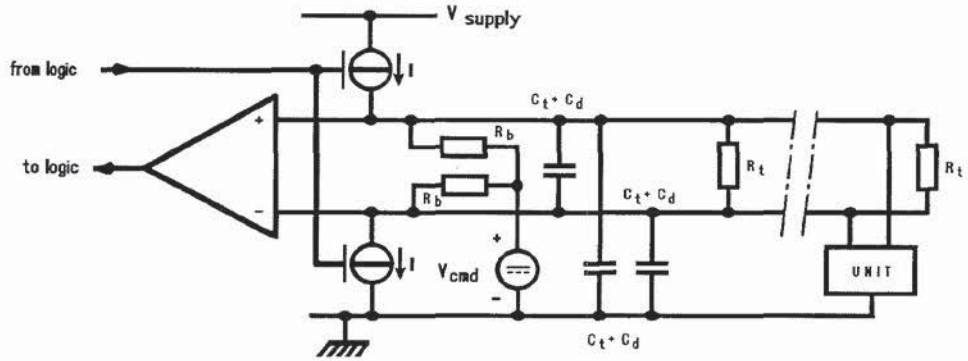


FIGURE 26.38 D2B physical interface.

Bit Encoding

Pulse-Width Modulation (PWM). The general bit format is composed of four sections: the preparation period, the sync period, the data period, and the stop period. The duration of the periods and the bit is dependent on the speed of the bus and the type of the bit. The speed of the bus is determined during contention. Low speed is dominant. There are three speeds possible. The general bit format is shown in Fig. 26.39.

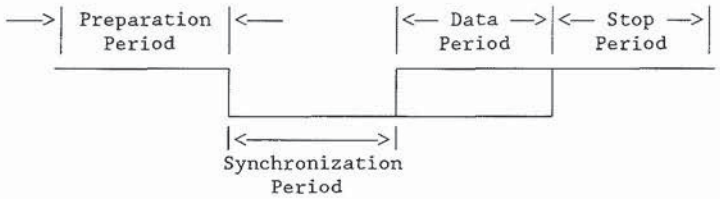


FIGURE 26.39 Pulse-width modulation bit format.

Network Access. Access is achieved by contention using nondestructive prioritized bit-by-bit arbitration. Competing nodes arbitrate first on the mode in which the node will operate in a three-bit field, where low mode is dominant. All nodes in a common mode then arbitrate based on the unique address bits of the competing masters. Low address is dominant. The mode designates the speed at which the bus will operate during the message transfer. A unit may use the bus for one time slot. The amount of data transferred in the time slot depends on the speed mode determined during arbitration.

Message Format. The frame consists of six fields. A parity bit follows the master, slave, control, and data fields. An acknowledge bit follows the slave field, control field, and the data field. An end-of-data bit follows each data byte. The total length of the frame is 47 bits. See Fig. 26.40 for the frame.

Handshaking. Handshaking is accomplished with positive acknowledgment in the transfer message. No reply from the slave is interpreted as a negative acknowledgment. The master can retry the message provided time remains in the slot. During every transfer, there are three different acknowledge bits: after the slave address, after the control bits, and after each data byte.

A master has the ability to lock a slave node to its address, having the effect of disabling the node from communicating with any other master on the network. This is done when a data

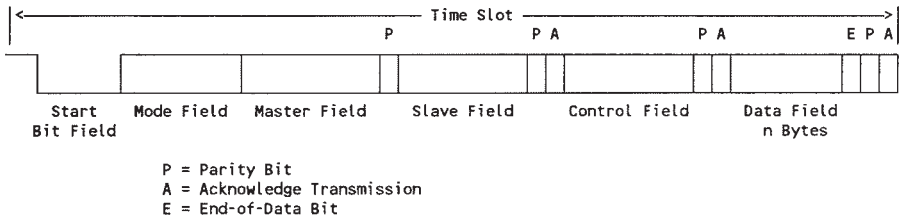


FIGURE 26.40 Six-field message format.

transfer exceeds the time slot and the master must arbitrate again for the bus to complete the data transfer.

Error Detection Management. Error checking is performed through odd parity on the slave address, control field, and after each data byte. The acknowledge bit in the transfer message will not be transmitted by the addressed slave if there is a parity error, the speed mode is too high, there is a timing error, slave locked to another master, or the receive buffer is full.

Fault Tolerance. Fault tolerance for nodes is not specified.

Data Rate. The maximum bit rate is 1Mbps. Three different transmission speeds are allowed.

Framing Overhead. The total frame size is 34 bits including interframe separation. In speed mode 1, 32 data bytes can be transferred from master to slave. Therefore, the percentage of overhead is $34/(34 + 256) = 11.7\%$.

Latency. D2B allows for three different speed modes for transmission and arbitrates on the address of the competing nodes once in a speed mode. Therefore, a low-priority node may experience high latency times vs. the average. Latency is also affected by the ability of a master to lock a slave node; a locked node will not respond to any messages. In certain situations, this could degrade the overall performance of the system.

Power Reduction Modes. Power reduction modes are available for the bus controllers.

26.3.4 Chrysler Collision Detection (C^2D), SAE J1567

Application/Affiliation. The serial communications network and bus interface special function integrated circuit[9] was developed by Chrysler Corporation and is supplied commercially by Harris Corporation. The interface IC was intended to provide a simple, yet reliable, data communications network between members of a distributed processing vehicle multiplex system. The communications protocol chosen minimizes the software support overhead requirement of the modules on the multiplex bus.

Transmission Media. Conventional 120-ohm automotive dual twisted pair >1 twist/in.

Physical Interface. The differential transceiver is a serial interface device which accepts digital signals and translates this information for transmission on a two-wire differential bus. The transmitter section, when transmitting, shall provide matched constant current sources to the bus "+" and bus "–" drivers (Refer to Fig. 26.41) sourcing and sinking current, respectively. When a logic "0" is supplied to the "transmit data" input, the differential amplifier shall cause the bus "+" driver to provide source current and the bus "–" driver to provide a matched cur-

rent sink. A logic one at the transmit data input must cause the bus "+" and bus "–" drivers to simultaneously provide a high impedance state.

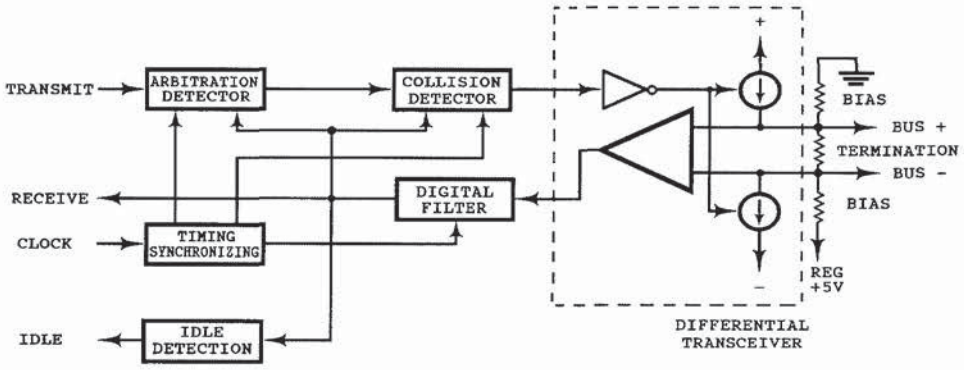


FIGURE 26.41 Simplified block diagram of network interface.

The wired OR action of the transmitting section allows more than one device to transmit at the same time, thus permitting data collisions. The nonsymmetrical action of the bus drivers will allow a transmission of a logic "0" from one device to overpower the transmission of a logic "1" from other devices. In this manner, two or more devices can simultaneously transmit and contend for the bus, each using a unique message ID byte. The winner is determined by the value or priority of the ID byte without losing bus time. A logic "0" bit in one message ID byte has priority over a logic "1" bit in another message ID byte.

The bus shall depend on external resistor and other components for bias and termination. Clamping diodes may be added to provide a high level of transient protection.

In addition to the transmission of data, the differential transceiver receives data at its bus "+" and bus "–" terminals. The received data is translated back into the standard digital logic levels by a differential amplifier. The microcomputer always receives the actual transmitted data and in this manner can test for loss of arbitration.

Bit Encoding. The bit encoding chosen is standard 10-bit NRZ, an asynchronous serial I/O. A start bit and a stop bit is added to provide data byte synchronization. Figure 26.42 illustrates this 10-bit NRZ waveform. The interface makes use of the available hardware that has this asynchronous I/O, e.g., the serial communications interface (SCI) available on many microcomputers.

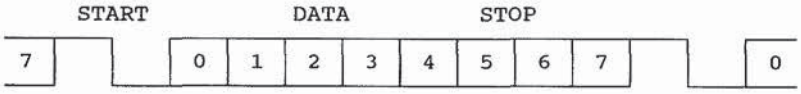


FIGURE 26.42 10-bit NRZ waveform (LSB first).

Network Access. The network access method of resolving contention is by nondestructive bit-by-bit arbitration.

Message Format. The message format shown in Fig. 26.43 will support a number of higher level protocols. Take note that idle periods, i.e., interbyte separations (IBS), are allowed between each byte of data. This permits the use of firmware control and direct connection to the host microcomputer's asynchronous serial I/O port.

```
(SOM),(id 1),(id 2),(data 1),(data 2)···(data n),(EOM)

1.   SOM, defines start of message
2.   id 1, 8 bit firmware addressing scheme
3.   id 2, optional identifier
4.   Data, may take any form, i.e., data value, CRC, checksum, number of
     bytes in message, acknowledgment, etc.
5.   EOM, defines end of message (10 bits of Idle bus)
```

FIGURE 26.43 Frame format.

Handshaking. The IC utilizes a low-cost serial universal interface to most microcomputers by three modes of operation that are supported in one device: SCI, SPI, and buffered SPI.

The circuits of the interface IC used when connected to the microcomputer SCI are basic to the operation of all the other modes of serial communications. Therefore, this mode will be explained first. The components of the device (See Fig. 26.41) include the following: a contention permitting differential transceiver, a collision detector, an arbitration detector, a digital filter, a bus idle detector, and a timing and synchronizing circuit.

For a contention permitting differential transceiver, see the "Physical Interface" section for details. With a collision detector, data collision detection occurs because the transceiver output is reflected back into its input. The data collision detector samples the transmitted signal and the received signal. The timing of this sampling is determined by the timing circuit. When the collision detector determines that a logic "1" bit is being transmitted, but a logic "0" bit is being received, the collision detector blocks the transmitted signal. In this way, the data collision detector will permit only the interface with the highest priority to continue transmitting. The collision detector action of blocking transmission is also reset by detection of bus idle (10 consecutive idle bits).

The arbitration detector works in conjunction with the timing and synchronizing circuit to arbitrate between the start of data to be transmitted with the start of a received message from the bus. The arbitration detector blocks a transmission that could corrupt a message that is already in progress. It also allows the device that starts transmission first, after a bus idle, to pass its data through the interface and out onto the bus. In all other nontransmitting devices, the arbitration detector blocks transmission of data until the detection of a bus idle condition. When more than one device wants to transmit at about the same time, greater than ¼ bit time, the arbitration detector will allow transmission on a first-come first-served basis. If data transmission from more than one device on the bus is attempted in near synchronism—i.e., less than or equal ¼ bit time—the arbitration detector will allow the transmission. However, the data collision detector will permit only the one with the highest priority to continue transmission. The arbitration detector is also reset by the detection of a bus idle.

A low-pass digital filter is placed between the transceiver and the received data output. This circuit functions to filter out any received EMI from the desired digital data signal before being processed by the other circuits of the interface.

The function of the bus idle detector circuit is to detect when the bus is idle (not active) or busy (active) and then feed this information back to the microcomputer. It accomplishes idle detection by sensing a received stop bit followed by 10 bits of continuous idle or logic "1"s. Normally, an active or busy period follows an idle period. The sensing of an active or busy bus is accomplished by detecting a start bit. During unusual conditions such as node startup, any transition from a logic "1" to a logic "0" that is maintained for a period longer than ¼ bit time sets the active or busy flag.

The timing and synchronizing circuit uses an external clock and establishes the synchronizing and Baud rate timing signal. This generator circuit first synchronizes on the negative edge of a start bit and then generates a timing signal at the center (½ bit time) of each bit. This timing signal is used by the arbitration and collision detector circuit for sampling received data. This timing signal is also used by the idle detection circuit to determine an idle bus.

Error Detection Management. The normal method used to detect message data error is a firmware checksum scheme. Also, the correct number of bytes in a frame is validated by the microcomputer firmware and, in some applications, data byte overrun flags are utilized by the microcomputer hardware.

Fault Tolerance. There is continued network operation when a node loses power or is disconnected from the bus.

Data Rate. A 7812.5 Baud rate is recommended.

Framing Overhead. The typical frame length is four bytes long. Framing consists of 4 start bits, 4 stop bits, 8 id bits, 8 checksum bits, and 10 end of message bits = 34 bits total framing, not including IBS. Data = 16 bits.

$$\frac{\text{OVERHEAD}}{\text{MESSAGE}} = \frac{\text{FRAMING}}{(\text{FRAMING} + \text{DATA})}$$

$$\frac{\text{OVERHEAD}}{\text{MESSAGE}} = \frac{34}{(34 + 16)} = 68\% \text{ not including IBS}$$

Latency. In a nondestructive bit-by-bit arbitration scheme, a node will experience varying amounts of latency based on the priority of the message to be transmitted. When more than one device wants to transmit at the same time—i.e., less than ¼ bit time—the arbitration detector will allow transmission on a priority basis. If more than one device wants to transmit at about the same time—i.e., greater than ¼ bit time—the arbitration detector will allow transmission on a first-come first-served basis.

Power Reduction Mode. This supports a "sleep state" under microcomputer control by a <10-μ source or sink from bus "+" or bus "−" of input leakage shutdown current.

26.3.5 Class B Data Communication Network Interface, SAE J1850 PWM

The SAE J1850 Standard[10] defines two versions of vehicle multiplex networks. This section covers the PWM encoded at 41.6 Kbps and the following section (26.3.6) discusses the VPWM data encoded at 10.4 Kbps version.

Application/Affiliation. The Society of Automotive Engineers (SAE) developed a vehicle data network for Class B data communications. The latest revision, MAY94, is in publication.

Transmission Media. The physical layer approach is a dual-wire voltage drive. The media for dual-wire is either a twisted or parallel wire pair.

Physical Interface. A representative circuit diagram for the receiver/transmitter is shown in Fig. 26.44.

Bit Encoding

Pulse-Width Modulation. A "1" bit and "0" bit are shown in Fig. 26.45. All bits are encoded in this manner except for a few unique symbols differentiated by the pulse timing. Some of the symbols include start of frame (SOF), end of data (EOD), and end of frame (EOF).

Network Access. Nondestructive prioritized bit-by-bit arbitration.

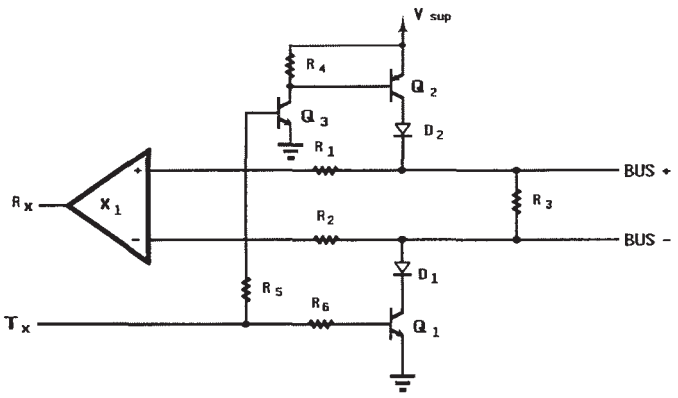


FIGURE 26.44 Representative diagram of PWM physical interface.

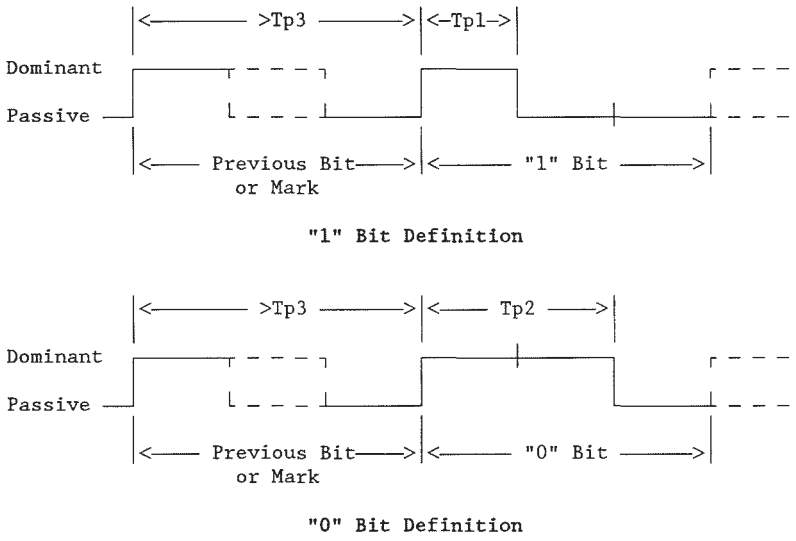


FIGURE 26.45 SAE J1850 PWM bit representation.

Message Format. The maximum length for a frame is 101 bit times. The error detection byte is included in the data field at the discretion of the designer. Another possible use of the data field could be a message/address identifier. The response byte is explained more fully in the handshaking section following. Interframe spacing is nominally 2 bit times. The message frame is shown in Fig. 26.46.

Handshaking. Acknowledgment is provided in the message frame using the response bytes. The response byte appears after the EOD. If an acknowledgment is not expected, a response byte will not be sent and the bus will remain in the passive state signifying an EOF. If the in-message acknowledge/response feature is active, then the response byte is an 8-bit acknowledge identifier or one or more response bytes followed by an ERR byte. One or more nodes may attempt to respond to the requesting node and arbitration will occur during the response time period.

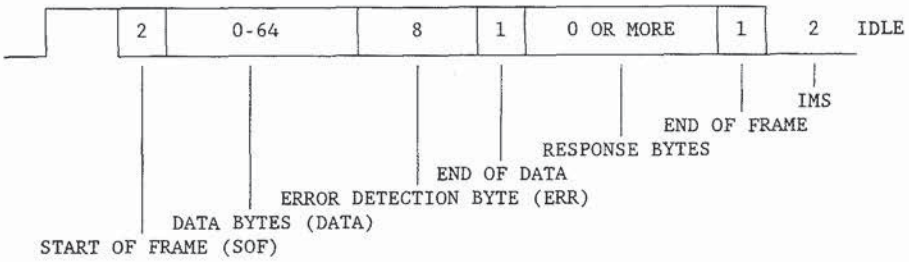


FIGURE 26.46 SAE J1850 PWM version message frame.

Error Detection Management. Includes detection of invalid bit value and invalid message structure. An invalid bit or an invalid message will cause the receive process to be terminated until the next SOF. The in-message error detection field (ERR) uses an 8-bit CRC based on the polynomial $x^8 + x^4 + x^3 + x^2 + 1$.

Fault Tolerance. Communications may be interrupted to/from a node when a node loses power, there is a bus short to ground, a bus short to battery, or a transceiver failure, but there shall be no damage to any other node. The remaining nodes are capable of communications when a node loses power, there is a transceiver failure, and for a loss of connection to network.

Data Rate. The bit rate specified is 41.6 Kbps.

Framing Overhead. The total length for the frame is 101 bit times and, for the overhead calculation, add two bits for IMS. The total length for the calculation becomes 103. The total allowed data is 80 bits for a one-byte form of header, a message identifier, and 64 bits for a three-byte form of header. The percentage of overhead is therefore $23/(80 + 23) = 22.3\%$ and $39/(64 + 39) = 37.9\%$.

Latency. In a nondestructive bit-by-bit arbitration scheme, the highest priority message/address will gain access to the bus. In a message priority scheme, a node will experience varying amounts of latency based on the average priority of messages to be transmitted. A node in an address priority system will experience a delay proportional to the priority level of its address and the activity on the bus. An example of such a delay is a low-priority node, which will experience higher than average latency during periods of high bus loading.

Power Reduction Mode. A node should enter a "sleep state" if the bus is idle for more than 500 ms. "Wake-up" occurs with any activity on the bus.

26.3.6 Class B Data Communication Network Interface, SAE J1850 VPWM

The SAE J1850 Standard[10] defines two versions of vehicle multiplex networks. This section covers the VPWM encoded data at 10.4 Kbps and the previous section (26.3.5) discusses the PWM encoded data at 41.6 Kbps version.

Application/Affiliation. The Society of Automotive Engineers (SAE) developed a vehicle data network for communications. The latest revision, MAY94, is in publication.

Transmission Media. The physical layer of the VPWM version defines a single-wire voltage drive. The media for single-wire is a single random lay wire.

Physical Interface. The representative circuit diagram for the VPWM receiver/transmitter is shown in Fig. 26.47.

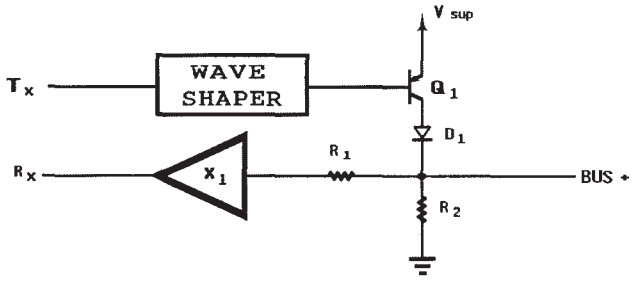


FIGURE 26.47 Representative diagram of a VPWM physical interface.

Bit Encoding. Each bit or symbol in variable pulse-width encoding (except break) is defined by the time between two consecutive transitions and the level of the bus, dominant or passive. Therefore, there is one symbol per transition and one transition per symbol. The end of the previous symbol starts the current symbol.

The "1" and "0" Bits. A "1" bit is either a long 128-μs passive pulse or a short 64-μs dominant pulse. Conversely, a "0" bit is either a short passive pulse or a long dominant pulse (see Fig. 26.48). The pulse widths change between passive and dominant bus states in order to accommodate the arbitration and priority requirements.

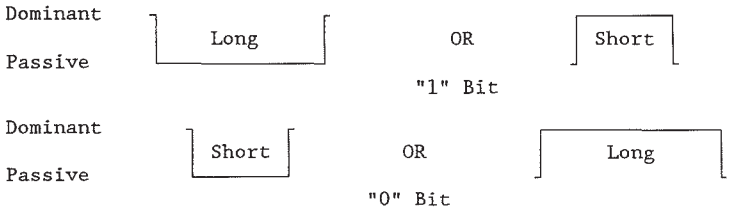


FIGURE 26.48 One and zero bit definitions.

The start of frame (SOF) is a dominant pulse, 200 μs in duration (see Fig. 26.49).

FIGURE 26.49 Start of frame (SOF) symbol.

The end of data (EOD) is a passive pulse, 200 μs in duration (see Fig. 26.50).

The end of frame (EOF) is a passive pulse, 280 μs in duration (see Fig. 26.51).

The In-Frame Response Byte(s)/Normalization Bit. The in-frame response is transmitted by the responder and begins after the

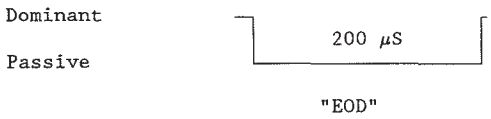


FIGURE 26.50 End of data (EOD) symbol.

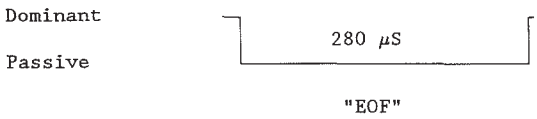


FIGURE 26.51 End of frame (EOF) symbol.

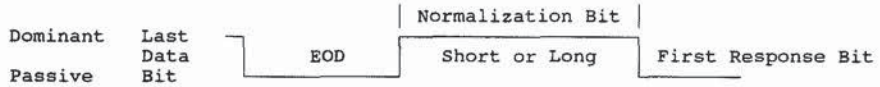


FIGURE 26.52 Normalization bit pulse-width modulation.

passive EOD symbol. For variable pulse-width modulation, the first bit of the in-frame response data is also passive. It is necessary to generate a normalization bit to follow the EOD symbol. The responding device generates the normalization bit prior to sending the IFR data. This normalization bit defines the start of the in-frame response and can take two forms. The first type is a dominant short period. The second type is a dominant long period and may be used to define an in-frame response with a CRC. Figure 26.52 illustrates the in-frame response using the normalization bit.

Network Access. Network access is by nondestructive prioritized bit-by-bit arbitration.

Message Format. The maximum length for a frame is 101 bit times. The error detection byte is included in the data field at the discretion of the designer. Another possible use of the data field could be a message/address identifier. The response byte is explained more fully in the handshaking section that follows. Interframe spacing is nominally 300 μs in duration bit times. The message frame is shown in Fig. 26.53.

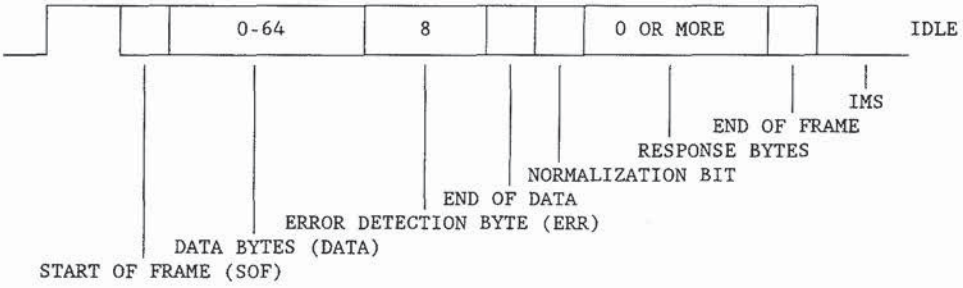


FIGURE 26.53 SAE J1850 VPWM message frame.

Handshaking. Acknowledgment is provided in the message frame using the response bytes. The response byte appears after the EOD. If an acknowledgment is not expected, a response byte will not be sent and the bus will remain in the passive state signifying an EOF. If the in-message acknowledge/response feature is active, then the response byte is an 8-bit acknowledge identifier or one or more response bytes followed by an ERR byte. One or more nodes may attempt to respond to the requesting node and arbitration will occur during the response time period.

Error Detection Management. Includes detection of bus out-of-range, invalid bit value, and invalid message structure. An invalid bit or an invalid message will cause the receive process to be terminated until the next SOF. The error detection field (ERR) uses an 8-bit CRC based on the polynomial: $x^8 + x^4 + x^3 + x^2 + 1$.

Fault Tolerance. Communications may be interrupted to/from a node when a node loses power, there is a bus short to ground, a bus short to battery, or a transceiver failure, but there shall be no damage to any other node. The remaining nodes are capable of communications when a node loses power, there is a transceiver failure, and for a loss of connection to network.

Data Rate. The bit rate specified is 10.4 Kbps.

Framing Overhead. The total length for the frame is 101 bit times. For the overhead calculation, add 2 bits for IMS. The total length for the calculation becomes 103. The total allowed data is 80 bits for a one-byte form of Header (message identifier) and 64 bits for a three-byte form of header. The percentage of overhead is therefore $23/(80+23) = 22.3\%$ and $39/(64+39) = 37.9\%$.

Latency. In a nondestructive bit-by-bit arbitration scheme, the highest priority message/address will gain access to the bus. In a message priority scheme, a node will experience varying amounts of latency based on the average priority of messages to be transmitted. A node in an address priority system will experience a delay proportional to the priority level of its address and the activity on the bus. For example, a low-priority node will experience higher than average latency during periods of high bus loading.

Power Reduction Mode. A node should enter a sleep state if the bus is idle for more than 500ms. Wake-up occurs with any activity on the bus.

26.3.7 Chrysler Sensor and Control (CSC), SAE J2058

Application/Affiliation. A proprietary multiplexing technique,[11] the Chrysler Sensor and Control (CSC) bus, yields the flexibility in expansion to meet the future demands of automotive customers. The CSC bus components were developed to provide simple, yet reliable, communication between a host-master module and its sensors and actuators. The scheme chosen provides the ability to communicate in both polling mode and direct addressing modes. This form of multiplexing will permit smaller module connectors and reduce the number of wires crowding through the congested areas without introducing more modules. The (CSC) bus is a style of multiplexing that meets these objectives and allows the design of the base vehicle while attaching the complete cost of optional features to the option.

Two CSC components are available as of this publication: (1) CSC bus two-pin, CSC Bus Hall Effect Sensors, Allegro P/N A3054U, and (2) Driver/Receiver Master Interface, Cherry Semiconductor, Automotive IC Data Book, P/N CS-8425 Hall-Effect Sensor.

Transmission Media. The CSC network utilizes a single-wire random lay.

Physical Interface. The output waveform of the driver/receiver master interface must be wave-shaped to limit the rise and fall time. Empirical vehicle testing has confirmed acceptable EMI levels if the waveform transients exceed 20 μs at data rates of 1 Kbps. The susceptibility to EMI is of greater concern. (See Fig. 26.54).

The preferred solution is to reference the CSC sensor at the driver/receiver master interface ground. This solution virtually eliminates this longitudinal noise current and, at the same time, significantly reduces the effects of ground offset voltage. In a production vehicle, returning the CSC sensor references to the master module usually does not add a wire circuit because these sensors originally had an independent ground wire return to the body or chassis. Further improvement to EMI susceptibility can be achieved by placing a small bypass capacitor across the CSC bus at the sensor.

Bit Encoding. Continuous Polling Mode Sensor Multiplexing. Figure 26.55 contains the typical voltage waveform used to communicate with multiplexed sensors. As illustrated, the sensors use current to respond back to the master that generates the voltage waveform. In this scheme, each sensor has an internal preprogrammed address. The voltage begins at a reset (zero volt) level and climbs to 6 V. This initial 6-V level provides power to the sensors. During

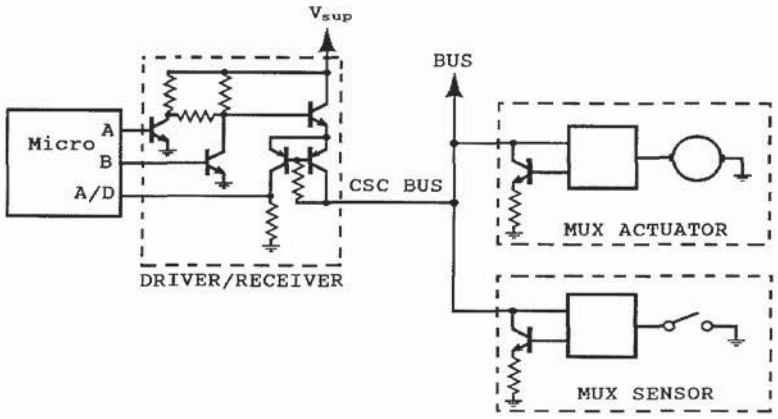


FIGURE 26.54 Representative diagram of a CSC sensor actuator bus.

this time, the master reads the amount of current required to keep the sensors powered. This current is called the sensor power current. At each change from 6 V to 9 V, a counter contained in the sensor is incremented. The sensors are addressed consecutively so this mode of CSC bus communication is called the *continuous polling mode.*

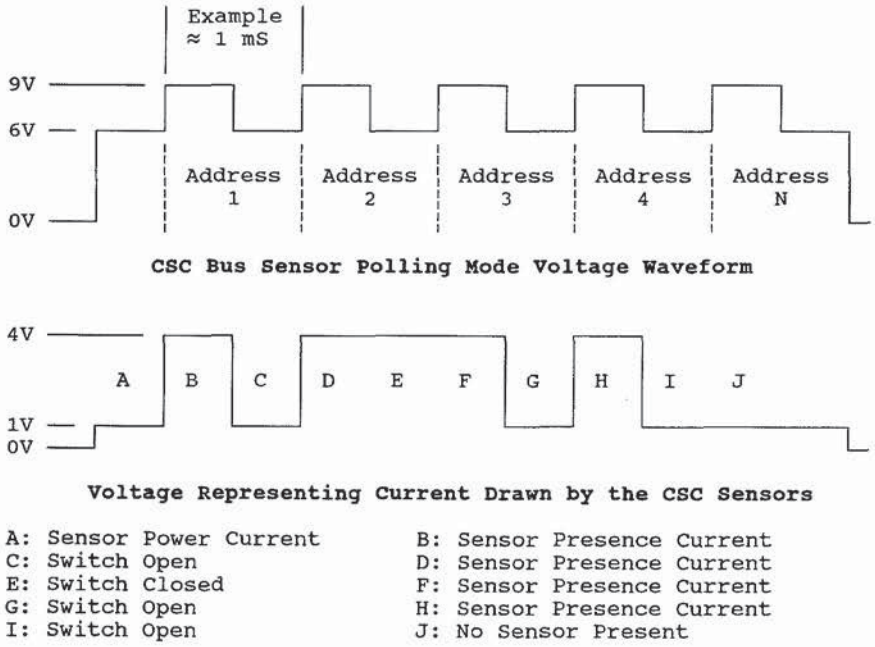


FIGURE 26.55 CSC bus sensor polling mode waveform.

While the voltage is at approximately 9 V, the sensors compare the value in their counter to their preprogrammed address. If a sensor detects a match between these two values, the sensor will increase the current drain on the CSC bus. This *response current* informs the mas-

ter that a sensor has recognized its address. This condition remains until the voltage falls to about 6 V.

When the sensor being addressed detects that the voltage is below its threshold of about 7.5 V, it will determine the status of the sensing element, i.e., magnetic field detecting Hall effect sensor, optical sensor, or mechanical switch to ground. If the sensing element is active—i.e., a magnetic field is detected—light is detected, or a mechanical switch to ground is closed, the sensor continues to draw the response current so that the master can sense the sensor's status. If the sensing element is not active, response current will cease and only the sensor power current will be drawn.

Actuator Polling Multiplexing. This effort to control actuators utilizes the CSC bus multiplexing technique used as an extension of the sensor polling mode. A particular actuator is assigned an address, just as the sensor is assigned an address. Each actuator monitors the CSC bus to count the 6- to 9-V transitions in the same way as the sensor does. When the value in the counter of the actuator matches the actuator's address during the 6-V portion of the address, the actuator draws current to tell the master that the actuator is recognizing its address.

To activate an actuator output, the status must first be monitored by checking the current drawn during the second half of the address cycle. In contrast to the sensor polling scheme, which uses 6-V and 9-V levels only, the actuator multiplexing scheme adds a third 3-V level (see Fig. 26.56). During the second half of the address cycle, the level is driven to 3 V by the master when the output of the actuator is to be toggled. The actuator monitors the CSC bus during its address. If the actuator detects the 3-V level, a latch is set. The actuator does not change its output, because of noise considerations, after the first 3-V level is detected.

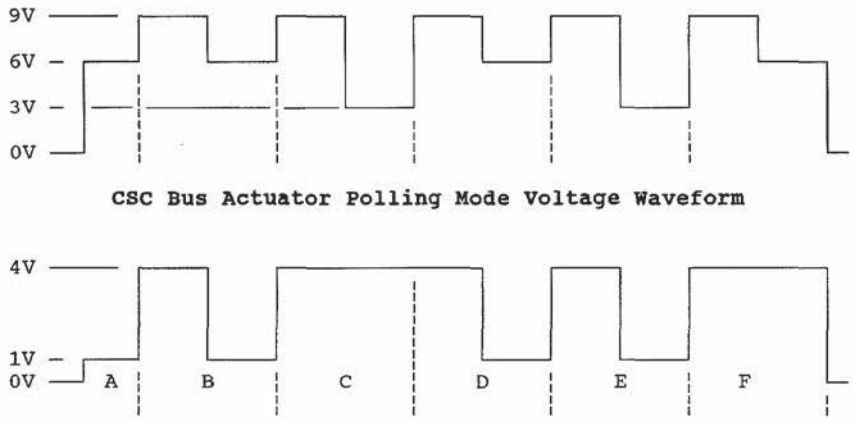
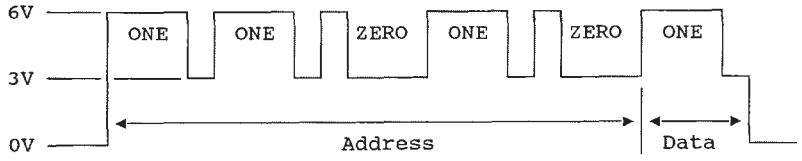


FIGURE 26.56 Continuous polling actuator multiplexing waveforms.

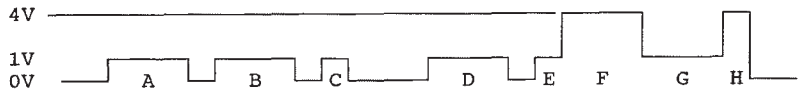
The actuator monitors the following polling cycle. If the second half of the actuator's address period in the very next polling cycle is 3 V then the actuator will toggle its output. Every subsequent polling cycle must contain the 6-V level during the actuator's address period for the output to remain constant. The current drawn by the actuator during this second half indicates the status of the output. When the output is to change state again, two consecutive polling cycles must contain 3-V levels during the second half of the actuator's address period.

Actuator Command Mode Multiplexing. In order to increase the flexibility of the communication scheme, the system designer has as an optional complementary actuator multiplexing capability. In order to provide all polling addresses to sensors and permit direct addressing of a particular actuator, a scheme was devised that complements the polling mode. This scheme has been called the *command mode, direct addressing,* or *control mode* of the CSC bus.

Instead of sequentially addressing the actuators as in the polled method, the master sends a 6-ms voltage signal to the actuators (Fig. 26.57). This waveform consists of transitions between 6 V and 3 V. The example 6-ms waveform is divided into six 1-ms bits and is called a 6-bit word. A 75%/25% pulse-width modulation technique is used to define the bit value. Each bit begins with a transition to 6 V. For example, a "1" bit is defined as 750 μs at 6 V and 250 μs at 3 V. A "0" bit is defined as 250 μs at 6 V and 750 μs at 3 V.



CSC Bus Command Mode Actuator Multiplexing Voltage Waveform



A, B, C, D, E, and G: Sensor Power Current
F: Actuator Response Current
H: Actuator Output Status High

Voltage Representing Current Drawn by Sensors and Actuators

FIGURE 26.57 CSC bus command mode actuator multiplexing waveform.

The first five bits of the 6-bit word are used to address the particular actuator and the sixth bit is used to control the state of the actuator's output. The master provides the voltage waveform. The CSC bus is initially at reset (≈0 V). From reset the voltage waveform is driven to 6 V. The waveform stays at 6 V for either 750 or 250 μs, depending on whether the bit is a "1" or a "0", respectively. The CSC bus then falls to 3 V for the remainder of the 1-ms bit period. During the 6-V portion of the first bit, the master monitors the current drawn by the components on the CSC bus. The master will use this current later as a reference to determine if an actuator has recognized its address.

All six bits are transmitted the same as just described. During the 3-V portion of the fifth and final address bit, the master can determine that an actuator has recognized its address by measuring the amount of current being drawn.

Network Access. The CSC bus utilizes a master-slave protocol. This protocol is appropriate because the master is usually the present major feature module and its associated sensors and actuators are the slaves. The feature module microcomputer is the host to the driver/receiver interface IC.

The CSC bus driver/receiver master interface integrated circuit contains the circuitry required to provide a DC offset square wave output. This output is controlled by two digital CMOS inputs: A and B. These two inputs are provided by a host microcomputer acting as the "brains" of the master control module. The IC is able to sense the CSC bus current and con-

vert it to an analog voltage. This voltage is provided by the IC output for use by the microcomputer analog input.

Message Format. The network method for this communication system is a master-slave polling and/or direct address method. The master uses a voltage waveform to communicate to the sensors and actuators. A sensor is addressed through successive and ordered polling of each address (time slot or period) in ascending order.

```
<SOM>, Wake-Up Period, Addr 1, Addr 2, ..., Addr 32
```

An actuator may be controlled by either the polling mode shown or the direct address, command mode message below. The start of message (SOM) is defined as the rising edge from 0 to 6 V in the voltage waveform of Fig. 26.55.

```
<SOM>, <Five-Bit address>, <1 to N data bits>, {<parity bit>}
```

Handshaking. Both sensors and actuators respond to the master node when polled or directly addressed, with a response current informing the master that an address has been recognized.

Error Detection Management. Actuator data can be protected from unwanted actuation by a parity bit in the command message. The normal solution for eliminating EMI susceptibility that caused false sensor data is to software filter the data in the master control module.

In order to validate the proper addressing of a sensor or actuator in a noisy vehicle environment, the following procedure is suggested. If this current is not above the reference current measured, the sensor is not present or no actuator is listening. If two or more sensors or actuators are listening (determined by double the expected response current), the master can reset (output zero volts) the CSC bus. If the master detects that the sensor or actuator output is not in the correct state, the command can be repolled or resent.

Fault Tolerance. Handshaking between the master node and sensors allows operation and detection when sensors or actuators are removed from the network. The driver/receiver has a current limit that protects it from a bus short.

Data Rate. The data rate is determined by the master module software and need not be fixed. A rate of 1 Kbps is suggested.

Framing Overhead. The framing required time is equal to the data time therefore:

$$\frac{\text{OVERHEAD}}{\text{MESSAGE}} = \frac{\text{FRAMING}}{(\text{FRAMING} + \text{DATA})}$$

$$\frac{\text{OVERHEAD}}{\text{MESSAGE}} = \frac{1}{2} = 50\%$$

Latency. The master node is in control and can interrupt sensor or actuator polling to command an output to an actuator within a few milliseconds and 32 sensors can be polled within 32 ms, or a 1-Kbps rate.

Power Reduction Mode. The master node can control the power by not polling or addressing the network. The current draw will then be the sensor actuator standby power.

26.3.8 Token Slot Protocol, SAE J2106

Application/Affiliation. General Motors developed protocol[12] for high-performance vehicle control and general information sharing.

Transmission Media. Not specified. Electrical twisted pair or fiber optic media are recommended. Fiber optic token slot networks operating at 1 Mbps have been demonstrated.

Physical Interface. Not specified. Multiple access to a logical common bus is required.

Bit Encoding. NRZ (nonreturn to zero) with opposite logic level bit insertion (stuffing) after five contiguous bits of the same state. Receiving nodes detect and remove inserted bits.

Network Access. The token passing bus network is open, peer-oriented, and multimaster. It is noncontention and uses a time slot token passing technique. See Fig. 26.58, 26.59, and 26.60.

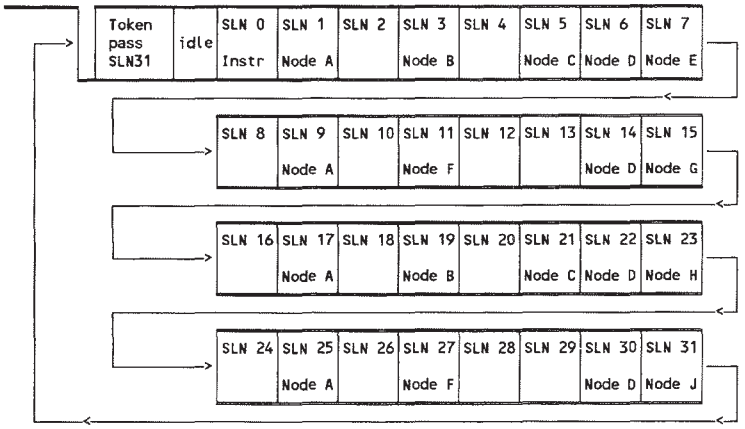


FIGURE 26.58 A typical token slot node assignment and slot sequence cycle pattern.

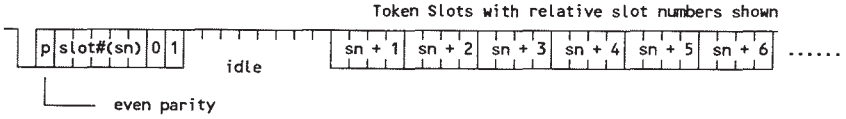


FIGURE 26.59 Token pass message format.

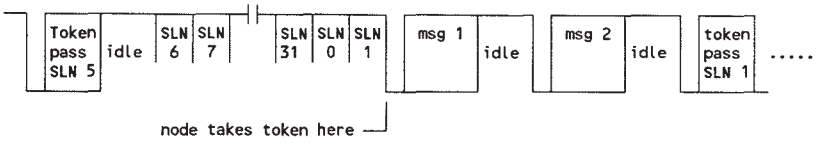


FIGURE 26.60 Typical token pass sequence.

The intent of this bus access protocol is to guarantee periodic opportunities for message transmission by each node on the bus. It is to also ensure that the bus remains operational when devices are dynamically added or deleted and it must provide for quick recovery from error conditions.

After a node has completed sending its message traffic, a sequenced scan of short, equal time intervals (slots) offer bus transmit privileges to the node slot owners as follows (see Fig. 26.59): A token pass message or a *bus jam* instructs all nodes to begin the token slot timing mode. Each node is assigned one or more specific time slots and will activate its transmitter to send a message during its slot only if it is operational and has message traffic to send. Otherwise, the token slot interval is allowed to pass. When the transmitter is activated, all other nodes recognize that the token has been taken and they enter the receive mode.

The new token owner next proceeds to send its message traffic (see Fig. 26.60). Token hold times are individually assigned to each node and are strictly limited to assure a system maximum message latency limit. Individual message transmit priorities are determined by each node's application and are not restricted by the data communications network.

A node concludes a transmit session by sending the token pass message that contains the current slot number (see Fig. 26.60). In the ensuing token slot sequence, the node that owns the next sequential slot number may take the token or let it pass. When the maximum slot number is reached, the sequence wraps around to slot 0 and continues until the slot is picked up or until the original token passer sees its slot, at which time a new token pass message is generated and the cycle begins again.

Message Format. There are three basic message types which are distinguished by the 2-bit control field which is found in the first byte:

- *Token pass* (see Figs. 26.59 and 26.60). This is a single-byte message which contains the message control field (2 bits), the current slot number (5 bits), and a single parity (even bit). It is followed by an idle line (8 bits) delimiter.
- *Data* (see Figs. 26.61 and 26.62). This includes the message control field (2 bits), a message ID field (14 bits), up to 256 bytes of data, a 16-bit cyclic redundancy check (CRC) field, and a message delimiter bus idle line (8 bits). The message control field is used to request an "acknowledge" message response.

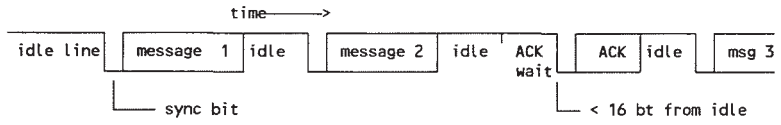


FIGURE 26.61 Token slot network general message framing.

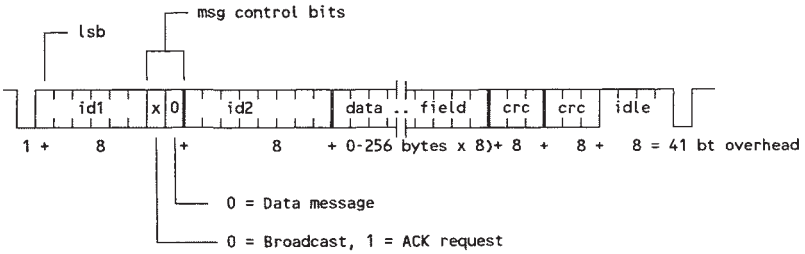


FIGURE 26.62 Token slot network data message format.

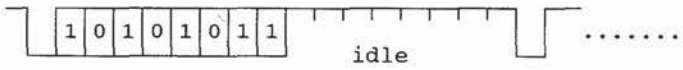


FIGURE 26.63 Token slot network acknowledge message format.

- *Acknowledge* (see Fig. 26.63). This is a fixed, single-byte (Hex D5) message plus an 8-bit idle line delimiter (16 total bits). It is initiated by the previous data message control field.

Handshaking. Any data message can be dynamically programmed to command an immediate returned acknowledge message from one receiving node. If after a short wait interval the requested acknowledge has not been received, the sender may retry and/or proceed to send other messages. Note that the responding node does not possess the token.

Error Detection Management. Both the receiving and the transmitting nodes independently monitor transmissions on the bus. The transmitting node checks messages for a 1:1 received to transmitted bit correspondence. All nodes check for correct timing, CRC, intermessage gaps, and, if requested, an acknowledge message. Receiving nodes do not acknowledge erroneous messages.

The 16-bit CRC conforms to the CCITT standard and detects all single-bit errors, all parity errors, and all burst errors less than 17 bits long. For burst errors longer than 16 bits, the CRC misses 0.0015 percent of errors.

A transmitter detected *bus time out* (BTO) error occurs when the bus is idle for more than a complete token slot sequence period. When a BTO is detected, all nodes start a new token pass slot sequence beginning at slot 0.

Bus errors or collisions cause the detecting node to generate a bus jam signal, a dominant line for 8-bit times, before the end-of-message idle line. This declares the current operation or message invalid and instructs all nodes to start a new token pass slot sequence beginning at slot 0.

Fault Tolerance. Each transmitting node monitors its own bus performance and fault history. Appropriate degraded mode operations are controlled by the node. The loss of any node or even a separated bus will not affect the continued bus operation by the remaining nodes.

Data Rate. Data rate limit is specified at 2 MHz. However, the data rate is only limited by bus media bandwidth and future data rate growth is possible.

Framing Overhead. The message framing overhead is summarized in Tables 26.3 and 26.4. See Fig. 26.64 for total message latency calculation methods.

TABLE 26.3 Token Passing Slot Overhead in Bit Times (bt)*

Slot width (assume xmtr ON aqt mid slot = 2 bit)	2
Token pass message	8
Delimiter gap	8
Token pass overhead per node	18 bit

* See Fig. 26.59 and Fig. 26.60

TABLE 26.4 Token Slot Data Message Overhead*

Synchronization bit	1
ID	16
Data (system determined limit, e.g., 0–256 bytes)	var
CRC	16
Intermessage delimiter gap	8
Acknowledge response (if requested) + gap	16
Per message overhead—with ACK	57 bits
or per message overhead—without ACK	41 bits

* See Fig. 26.61, 26.62, and 26.63

Token Slot Message Overhead (in bit times = bt):

Synchronization bit	1
ID	16
Data (system determined limit - bytes)	(0-256 bytes)
CRC	16
Intermessage delimiter gap	8
Acknowledge response (if requested) + gap	16
Per message overhead - with ACK:	57 bt
or Per message overhead - without ACK:	41 bt

Token Passing Slot Overhead:

Slot width (assume xmtr on at mid slot = 1 bt)	1
Token Pass Message	8
Delimiter gap	8
Token pass overhead per node:	17 bt

Summary of Loop Time Calculations:

For P nodes sending an N message loop with M total message data bytes:

Total message overhead (no ACK)	41N
Total token overhead	17P
Total message data time (m x 8 bits)	8M
Unused slots = slot width x (max #slots - #usedslots) = 1(32-P)	
Total Loop Time	41N + 17P + 8M + 4(32-P)

Example Token Slot Timing Calculation

For 8 nodes sending a 16 message loop with 32 total message data bytes (2 msgs x 2 bytes per node x 8 nodes):

Total message overhead (no ACK)	41x16	=	656
Total token overhead	17x8	=	+ 136
			792
Total message data time (32 x 8 bits)		=	+ 256
Unused slot time	(1x24)	=	+ 24
Total Loop Time (bt)			1072

Data-to-total time overhead efficiency: 256/1072 = 24.0%

FIGURE 26.64 Determination of token slot message latencies.

Latency. The protocol is noncontention and deterministic. As such, message latencies in the token slot network are both predictable and bounded, which is a requirement for feedback control systems.

Factors that affect message latency times are discussed in the following. See Fig. 26.64 for methods of latency calculation and prediction.

The token loop time determines the interval between opportunities to transmit a message. It is defined as the total elapsed time between token possessions by a particular node. It includes all message traffic, token pass slot times, and all token hold times.

Token slot time length is important during the token pass sequence when each time slot must provide sufficient time for worst-case signal propagation delays in order to allow nodes to detect that the token has been taken.

Token hold time is the maximum number of bit times that each node is allowed to hold the token. All message IDs, data fields, CRCs, intermessage gaps, message synchronization bits, NRZ5 bit insertions, acknowledge messages or acknowledge time outs, and token pass messages must not exceed this limit. Each node monitors and controls this time to stay within its assigned limit.

Power Reduction Mode. Not specified. Could be implemented.

26.3.9 Time Triggered Protocol (TTP)

Knowledge about the future (i.e., a priori knowledge) behavior of the TTP system is available to the system designer and is controlled by the progression of time.[13] For example, the point in time when a node is supposed to send a message can and must be determined by the real-time control algorithms and programmed into the module before release for production. The main advantage to TTP is to support high-speed distributed time-triggered real-time control of systems.

Application/Affiliation. TTP was developed by the Institute for Technical Information, Technical University Wien, Austria, and is an integrated communications protocol for Class C in-vehicle applications that provides all services required for the implementation of a distributed fault-tolerant high-speed real-time control system.

Transmission Media. A twisted pair or fiber optics is suggested for the transmission media.

Physical Interface. The basic system I/O structure consists of nodes connected by two redundant physical interfaces to dual networks to protect for failures in cabling, contacts, connectors, etc. To tolerate a node failure, two nodes are connected in parallel. Four configurations are shown in Fig. 26.65.

Bit Encoding. The bit encoding is not specified. However, modified frequency modulation (MFM) is suggested as the encoding technique because it has fewer than one transition per bit.

Network Access. The network access is accomplished using a time division multiple access (TDMA) controlled by a global time base generated by time triggered protocol (TTP). A TDMA round is defined to be a complete cycle during which each vehicle module has been granted at least one sending access.

Message Format. All information transmitted on a communications channel must be properly framed. A TTP frame consists of the following fields: start of frame (SOF), a control field, data field, and a CRC field. An interframe delimiter (IFD) exists between any two TTP frames. See Fig. 26.66.

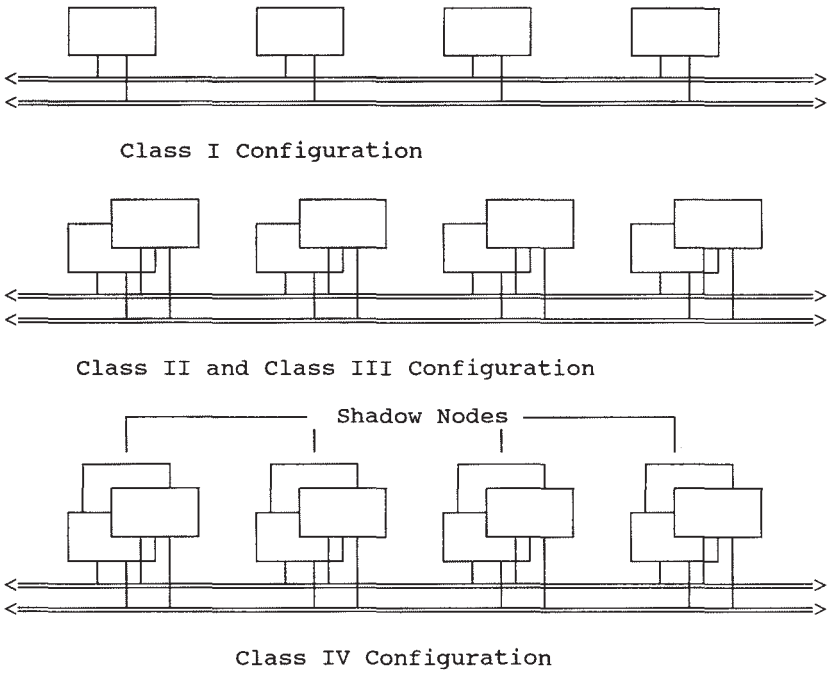


FIGURE 26.65 Fault-tolerant configurations.

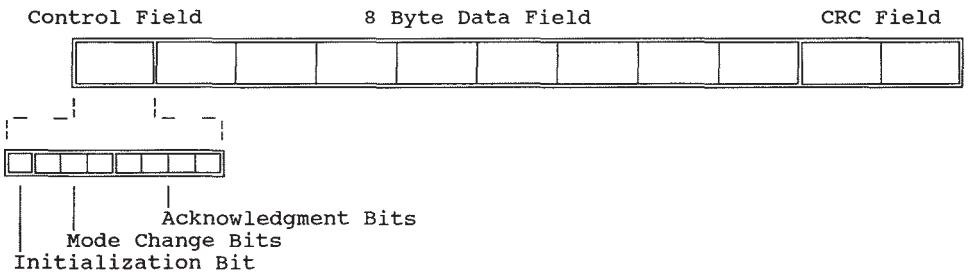


FIGURE 26.66 Typical frame format.

Start of Frame (SOF). This identifies the beginning of a new frame.

Control Field. The control field has three subfields.

Initialization Bit. This specifies an initialization frame (I-frame) or a normal frame (N-frame). I-frames are required to initialize a node. The state of the communications controller node (i.e., C-state) consists of three fields: a node field, a time field, and a membership field. Typically, each one of these fields will have a length of two bytes, or 16 bits. When a node is initialized, these three fields are filled from the data field. N-frames are normal data frames containing the application data in the data field.

Mode Change Bits (3 bits). If the initialization bit is unequal to zero, it allows the specification of seven successor modes to the current mode. Therefore, the protocol supports a rapid change from one mode to another mode, e.g., startup, normal operation, emergency, etc.

Acknowledgment Bits (4 bits). These bits contain an acknowledgment for the frames sent by the preceding vehicle module. The question of which module is the preceding module depends on the current membership. The length of the acknowledgment field makes it possible to acknowledge each one of the four frames sent by a module in a class III or Class IV configuration.

Data Field. The data field consists of the concatenation of one or more messages containing application data. The length of each message is statically defined in the mode definition. It is not necessary to carry a name field in the frame since the message name can be inferred from the mode field and the point in time of sending.

Cyclic Redundancy Check (CRC) Field. The CRC field has a length of two bytes. For N-frames, the CRC is calculated over the C-state of the controller concatenated with the control field and the data field of the frame. A normal frame is only accepted if the sender and receiver have identical C-states, i.e., if they agree on mode, time, and membership. Since the receiver knows a priori the time of sending of each frame, it is not necessary to carry the value of the send time in the frame.

Interframe Delimiter (IFD). The interframe delimiter is required for proper bit synchronization of sender and receiver.

Handshaking. As shown in Fig. 26.65, two nodes are connected in parallel to tolerate a node failure in replicated vehicle communications channels. These replicated channels perform the same state changes at about the same time and are synchronized to within a known precision by TTP.

Error Detection Management. TTP is based on the assumption that the communications channels have only omission failures and the nodes support the fail-silent abstraction; i.e., they either deliver correct results or no results at all, which helps to enforce error confinement at the system level. A sender attaches a CRC to each frame and a receiver can detect when a frame has been mutilated and discard the corrupted frame.

For correct operation, the node must assure, by use of space or time redundancy, that all internal failures of a node are detected and the node is turned off before an erroneous output message is transmitted. Moreover, a membership service is required to detect omission failures of incoming and outgoing communications links. This membership service is part of the protocol.

Fault Tolerance. With dual duplex buses and redundant node communications channels, the fault tolerance capability is excellent. Table 26.5 shows the fault tolerance capability achieved with the four class configurations shown in Fig. 26.65. The recovery interval for a transient event depends on the length of the transient blackout period and the time TTP takes to detect, monitor, and recover from a blackout. This time for TTP is in the millisecond range.

TABLE 26.5 Fault Tolerance Capability

Tolerance of	Class I	Class II	Class III	Class IV
Permanent node failure	0	1	1	2
Permanent bus failure	1	1	1	1
Transient node failure	0	1 per event	1 per event	1 per TDM round
Transient bus failure	1 of 2	1 of 2	3 of 4	3 of 4

Data Rate. The data rate is not specified, but 1 Mbps is suggested.

Framing Overhead. The length of SOF and IFD depends on the bus propagation delay, the quality of the clock synchronization, and bit-encoding method. For transmission speeds below

1 Mbit and a bus length below 20 m, the SOF = 1 and IFD = 3. The framing overhead is given by the following: OVERHEAD/MESSAGE = FRAMING/(FRAMING + DATA). For a message transmitting 4 bytes (32 bits) of data, using the formula: 28/(28 + 32) = 47%. For a message of 8 bytes (64 bits) of data, using the formula: 28/(28 + 64) = 30%. The total framing overhead is slightly higher to account for the periodic transmission of initialization frames.

Latency. Given a 1-Mbit channel for eight nodes sending a 16-message loop with 32 total message data bytes, the TDMA round of TTP is 0.48 ms in Class I or Class II configuration. This is also the worst-case delay for a node switch. If a Class III or Class IV configuration with four replicated messages is selected, the TDMA round is doubled, i.e., just below 1 ms.

Power Reduction Mode. The power reduction is not specified but could be specified as a mode of operation. The change to a power reduction could be done at any time.

26.3.10 Vehicle Area Network (VAN)

Application/Affiliation. VAN (vehicle area network) is a multiplex bus protocol proposal being considered by the ISO Technical Committee 22/SC3/WG1.[14]

Transmission Media. Twisted pair.

Physical Interface. Transmission is on differential pair using current sources. An optional analog filter is provided to increase noise immunity. See Fig. 26.67.

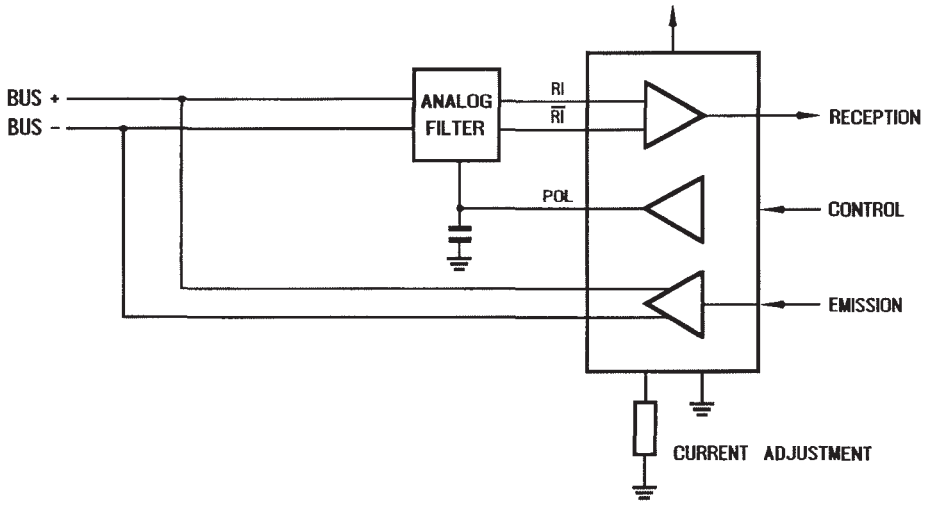


FIGURE 26.67 Fault-tolerant bus interface.

Bit Encoding. Two different bit representations are allowed: L-Manchester and E-Manchester. The bit representation is selected by the user. When L-Manchester is selected, all the bits in the frame are Manchester encoded. E-Manchester will be NRZ encoded except for the last bit of each nibble. With E-Manchester idle, IMS, and SOF are NRZ encoded, and ACK is Manchester encoded. See Fig. 26.68 for an example of E-Manchester encoding.

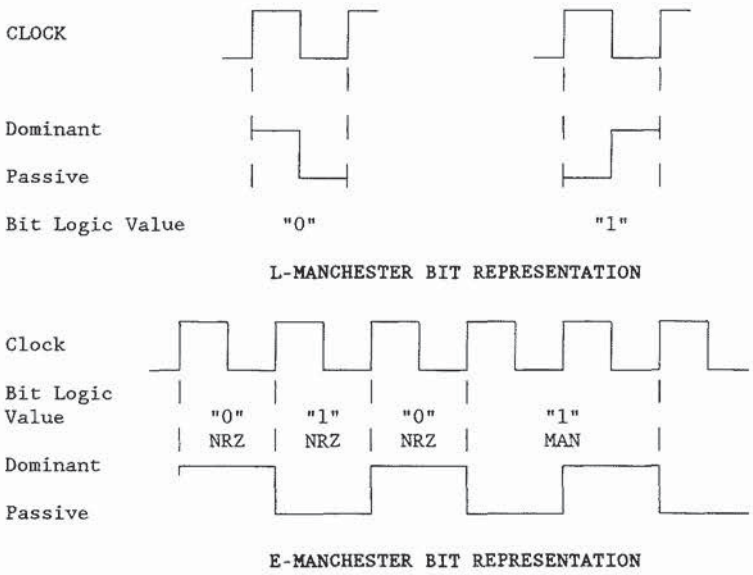


FIGURE 26.68 VAN bit encoding.

Network Access. Network access is by prioritized nondestructive bit-by-bit arbitration. Arbitration is resolved using the unique 12-bit identifier field at the start of the message. The format of this field is user-defined. VAN allows in-frame access based on a media access rank R. A node can access the frame, provided the previous R-1 bits of the arbitration field have been emitted and the previous time slot was recessive.

Message Format. The frame consists of eight fields. The start of frame (SOF) provides a common time reference that allows receiving nodes to correct their local clock. The start message bit initializes the frame. The two-byte frame identification field includes the unique 12-bit message identifier followed by three control bits and the remote transmission request bit (RTR). The RTR specifies if the frame includes data (0 bit) or if data is requested (1 bit). The RTR allows in-frame response immediately or later in a separate frame. The message frame is shown in Fig. 26.69.

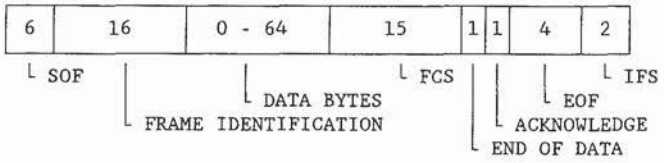


FIGURE 26.69 Single type frame format.

Handshaking. Message acknowledgment is achieved in one of two ways: no acknowledge or positive acknowledge, which means at least one station has received and accepted the message. If the receiving station cannot make an in-frame acknowledge, a separate acknowledge message must be sent later.

Error Detection Management. Methods of error detection include level monitoring, CRC, code violation detection, and frame check. Level monitoring is performed by the transmitting

node. The transmitted bit levels are compared with the bit levels detected on the bus. Frame checking is performed through a 15-bit CRC code:

$$\frac{(x^8 + x^4 + x^3 + x^2 + 1)}{(x^7 + 1)}$$

Fault Tolerance. Single-wire operation is possible with the differential drive scheme due to the ac-coupling if the other wire is shorted to ground, shorted to V_{batt}, or open circuited.

Data Rate. The data rate is not specified.

Framing Overhead. The total frame size (including data) is 109 bits. The total frame size includes start, stop, and idle bits. The maximum amount of data allowed in a frame is 64 bits. The percentage of overhead is therefore 45/(45 + 64) = 41.3%.

Latency. As with all arbitration-based protocols, the latency amount varies depending on the priority of the message.

Power Reduction Mode. Not specified.

26.4 SUMMARY AND CONCLUSIONS

Throughout the 20th century the auto industry has seen many changes. The electrical components in the horseless carriage were essentially a magneto ignition system. In the 1920s, the electric starter became popular but the first real use of the semiconductor in the auto industry was in the 1960s, first in electronic voltage regulators and then in brakerless ignition systems. Toward the end of the 1970s, the full engine control computer was in production. Then by the 1980s, consumers were demanding electronically controlled turbo, electronically driven instrument clusters, antilock brake systems, and navigation and trip computers. The electronic content of passenger vehicles had doubled by the 1990s.

26.4.1 The Future of Automotive Electronics

In the future, electronics will play an even larger roll. The automotive electronics field is presently going through a number of noteworthy changes. Integration, diagnostics, design for manufacturability, and system engineering are the buzzwords of the 1990s. The past add-a-feature, add-a-module mode of operation is replaced by integration. For example, the common practice is to package many of the feature items such as intermittent wipers and automatic door locks into a single module. The manufacturer will have a built-in diagnostics technique that can computer-verify that the product is functioning properly at the time of construction. Also, the dealer will have the capability of accurately and economically determining the failed module. Integration, diagnostics, and systems engineering promise higher quality, better performance, and lower cost for the manufacturer and the consumer.

26.4.2 The Class B Data Communications Network

The Class B data network is the main enabler and driving force to module integration and service diagnostics. The data network interconnects these integrated systems, allows the modules to communicate with each other, and provides for quick service and maintenance. These inte-

grated systems must be coordinated to make sure that everything functions together properly. The Class B data communications network is applicable because most of these features will not require real-time control processing.

Electronics and vehicle multiplexing means more than just new innovative gadgets in a car. This relatively new field of automotive engineering is a highly developed technology that has the potential for enormous benefits to the consumer in that it promotes safety and provides convenient and useful features in the automobile. The data network and electronics should make it easier and more economical to manufacture a car, drive a car, and service a car.

Even though the electronic content will have doubled, the car of the mid 90s will be significantly easier to manufacture because there will be half the number of modules, due to feature content integration. The data network that interconnects these modules will also reduce the size and number of interconnecting cables and cut the number of circuits by 25 percent.

The objective of the industry is to deliver a quality, defect-free product to the customer. As previously illustrated, integration plays a major role in reducing the number of modules that can fail, the number of parts that can break and the number of interconnecting circuits that can fail, thereby substantially improving the reliability. The data network and built-in diagnostics also play a key role in verifying that the product is manufactured properly. Proper diagnostics is also accomplished more perfectly by computer during manufacturing, and reduces or eliminates the arduous task of manual verification on the assembly line.

The computerized vehicles of the future need logically acute ergonomics for the driver. Safety, reliability, ease of use, buttons that are easy to reach, and gages or dials that are easy to see can all be characterized as "slickness." Our neoteric generation of customers is rightfully demanding these innovations and world competition makes it a top priority.

At the heart of these ease-of-driving innovations is the data network that allows the various integrated modules to coordinate their activity so that the buttons that control the displays can be placed at the best ergonomic locations. The display is then located for convenient viewing while operating the vehicle.

With the aid of market research, the integrated module may be chosen to contain just the mix of features the customer desires. The data network can significantly simplify delivery of the required data to that module. This gives the customer greater freedom than ever to pick and choose a personally designed content in his new vehicle, thus promoting customer personalization and satisfaction.

The auto industry designs for reliability, but when things fail, the objective is to economically fix it right the first time. Vehicle multiplexing again plays a major role in allowing the service technician to communicate with each of the modules using a diagnostic tool through a centrally located diagnostic connector. This method uses the power of the computer in the vehicle and the diagnostic tool to walk the technician through the diagnostic flowchart to deliver the solution to the problem in a language the service technician can understand.

26.4.3 Class A Multiplexing

With all these benefits why is multiplexing taking so long? Over the last two decades the automotive component manufacturers of electronic equipment have been touting the virtues of Class A vehicle multiplexing (low-speed body wiring and control functions). Previously, articles were illustrated with dramatic pictures of the amount of wire that could be saved by multiplexing. Other articles projected immense cost savings and technical benefits to be derived through the utilization of vehicle multiplexing. Now 20 years later, few, if any, of these predictions have become a reality. Thus, the domestic vehicle manufacturers have not generally endorsed these concepts.

For years it was postulated that vehicle multiplexing would be practical once a semiconductor device was developed that would replace the relay and have the capability of driving lights and electric motors. The recently developed MOS power driver has this multiplexing

potential. The semiconductor industry hopes that this device is the real breakthrough that will make Class A vehicle multiplexing a reality. However, with this development, the industry is only closer to a solution. The real situation is that Class A multiplexing is still not cost effective. A closer examination of the problems of Class A multiplexing from a vehicle manufacturers' perspective is warranted. The effectiveness of multiplexing must consider the following factors:

- The ability to reduce the average vehicle system cost
- The ability to allocate the cost of the option to the option
- Wiring reductions such as number of circuits and bundle size
- The support of built-in diagnostics for manufacturing and service
- Bus throughput (capacity) and how well the network architecture handles time-critical messages.
- Reductions in weight and ease of assembly

26.4.4 Comparison of Class A and B Data Networks

Is the Class B multiplexing situation any different than the Class A? A careful system cost analysis for Class B vehicle multiplexing shows that the added cost of the multiplexing electronic components is not offset by the cost savings in vehicle wiring harnesses. The condition is very similar to Class A data network leading one to adopt the theory that vehicle multiplexing by itself is not cost effective. The higher the cost of the electronic multiplexer, the larger the problem of finding effective cost offsets. Therefore, if the Class A data network is too complex it may not be cost effective.

There are other driving forces, such as increased content, packaging, and wire bundle size, that have the potential of outweighing the cost disadvantage. The situation with the Class B data network is much different. Class B vehicle multiplexing is the enabler to other cost-offsetting methods that are not possible with Class A multiplexing. Cost reductions such as module integration and diagnostics can be effectively used to more than offset the cost of the electronic multiplexer.

26.4.5 The SAE J1850 Standard

The SAE J1850 is a standard for a Class B data communications network. The entire automotive industry will benefit from the development of this data network. In the past, development of proprietary data networks inefficiently used scarce industry resources. Standardization will save manpower and resources, in both the semiconductor and automotive industry, and make the resources previously dedicated to proprietary data networks available for concentration on more competitive electronic developments.

The transition to an industry standard data network will be difficult and will take several years to accomplish effectively. The first introduction of the full industry standard vehicle multiplex network will be found on only luxury vehicles and then only after the system economics warrant support. Economics will play a major role in determining when the average vehicle, manufactured domestically or abroad, will have an industry standard data network. It will take the dedication and talent of electronic engineers in both the automotive and the semiconductor industries to develop the components that will meet the economic requirements. The development of a family of components is required to support the economical use on more than just the more expensive and luxury type vehicles. The application for data networks varies between manufacturers' product lines and there will be a need for different levels of industry standard data network interfaces to meet the full application requirements.

Acknowledgments

The author would like to thank the SAE support staff and all his colleagues on the Vehicle Networks for Multiplexing and Data Communications Standards Committee for their support in developing the original SAE documents from which the excerpts in this chapter originated. He would also like to thank Chrysler Corporation for its encouragement and use of its facilities. Without this material and support, this chapter would not have been possible.

GLOSSARY

This glossary contains generally accepted terminology for automotive electronic application. The terms may have additional definitions depending on usage in other disciplines.

Arbitration The process of resolving which frame or in-frame response data continues to be transmitted when two or more nodes begin transmitting frames or in-frame response data simultaneously.

Arbitration detection Refers to a contention-based arbitration circuit, whereby the contention created by simultaneous access of multiple nodes on the network is resolved in a bit-by-bit arbitration circuit by means of collision detection where dominant bits in the arbitration field survive without destruction and all others discontinue transmission. (See **Bit-by-bit arbitration** and **Collision detection**.)

Architecture The organizational structure of a vehicle multiplex network, mainly referring to the application structure and communications protocol.

Balanced current I/O An input/output circuit configuration in which signals are transmitted as currents that travel down one conductor and return on the other, and these currents are balanced, i.e., of equal magnitude.

Baud rate A measurement or transfer rate; a number of discrete conditions or signal events per second.

Bipolar data Data that is driven both positively and negatively from a common point such as a reference voltage or ground (0) potential.

Bit-by-bit arbitration A contention-based arbitration, whereby the contention created by simultaneous access of multiple nodes on the network is resolved bit by bit. Bits may be represented as dominant or passive on the physical layer with dominant bits overriding passive ones in case of contention. The message with a dominant bit in the arbitration field survives without destruction and all others discontinue transmission. This procedure is repeated through all bits of the arbitration field.

Bit encoding The smallest unit of information in the binary system of notation.

Bit rate Bits per time during transmission, independent of bit representation.

Bit-stuf NRZ The insertion of extra bits into an NRZ data stream to avoid the appearance of unintended control sequences for synchronization.

Bit synchronized Transmission of a frame in which the data bits are transmitted with the transmitter and receiver bit transitions aligned in time (synchronized).

Broadcast type messages The transmission of information to more than one receiver as differentiated from node-to-node communications.

Bus Topology of a communications network where all nodes are reached by links, which allow transmission in both directions.

Bursty noise Unwanted electromagnetic disturbances that are manifested as relatively short period barrages (bursts) at random or repetitive rates.

Checksum An error-detecting code based on a simple eight-bit summation series of all the bytes in the frame that are to be checked.

Class A system A multiplex system whereby vehicle wiring is reduced by the transmission and reception of multiple signals over the same signal bus between nodes that replaces the conventional wiring in vehicles. The nodes used to accomplish multiplexed body wiring typically did not exist in the same or similar form in a totally conventionally wired vehicle.

Class B system A multiplex system whereby data (e.g., parametric data values) is transferred between nodes to eliminate redundant sensors and other system elements. The nodes in this form of a multiplex system typically already existed as stand-alone modules in a conventionally wired vehicle.

Class C system A multiplex system whereby high data rate signals typically associated with real-time control systems, such as engine controls and antilock brakes, are sent over the signal bus to facilitate distributed control and to further reduce vehicle wiring.

Collision detection Collision detection and bit-by-bit arbitration are sometimes used interchangeably and they both refer to a contention-based arbitration, in which the contention created by simultaneous access of multiple nodes on the network is resolved on a bit-by-bit arbitration basis utilizing a collision detection means. (See **Bit-by-bit arbitration**.)

Command mode A mode of operation of a master-slave system in which the master node takes prompt control of the network to achieve the input and/or output function.

Common mode rejection ratio The ratio of the common mode input voltage to output voltage commonly expressed in dBV, i.e., the extent to which a differential amplifier rejects an output when the same signal is applied to both inputs.

Contention process A state of the bus in which data from two or more transmitters are simultaneously attempting to use a single shared network medium. A collision detection or arbitration process can be used to resolve the conflict.

Contiguous bits A condition where a string of data bits is continuous and without dead time between bits.

Control field A field in a frame which designates command information.

Control mode Control mode and command mode are used interchangeably and refer to a mode of operation of a master-slave system in which the master node takes prompt control of the network to perform the input and/or output function.

Cyclic redundancy check (CRC) An error-detecting code in which the code is defined to be the remainder resulting from dividing the bits to be checked in the frame by a predetermined binary number.

Data collision A state of the bus in which two or more transmitters are turned on simultaneously to conflicting states.

Data consistency A feature of communications in some multiplex wiring systems whereby it is determined and ensured that all required recipients of a message have received the message accurately before acting upon it simultaneously. This feature is desirable in, for example, ensuring that all four lamps are turned on at once or that all four brakes are energized simultaneously.

Data decoding technique The process of retrieving a signal on the transmission medium that was encoded (e.g., NRZ, PWM, Manchester) back into the original logical, "1"s and "0"s bits.

Data encoding technique Data bit encoding defines the way in which the logical bits, "1"s and "0"s, are translated into signals on the transmission medium by the physical interface (e.g., NRZ, PWM, Manchester).

Data field Data (data field) are bytes between header bytes and error detection byte. Data and data field are sometimes used interchangeably and they both refer to a field within a frame that may include bytes with parameters pertaining to the message and/or secondary ID and/or extended addresses and/or test modes, which further define a particular message content being exchanged over the network.

Decibel volts (dBV) A measure of the relative strength of two signals where the value is 20 times the log of the ratio of the voltage of the two signals.

Deterministic A signal is said to be deterministic when the future behavior of the signal can be predicted precisely.

Differential receiver The node receiver that contains a differential input. (See **Balanced current I/O**.)

Direct addressing mode Direct addressing, control mode, and command mode are used interchangeably and they refer to a mode of operation of a master-slave system in which the master node takes prompt control of the network to perform the input and/or output function.

Dominant bit A bit which wins arbitration when contending for the bus. For SAE J1850, a logic "0" is the dominant bit.

Driver A solid state device used to transfer electrical power to the next stage, which may be another driver, an electrical load (power driver), a wire or cable (line driver), a display (display driver), etc.

Duplex bus A multiplex bus where both transmission and reception occur simultaneously on the same network media. Also referred to as "full duplex."

Dynamic range The difference between the overload level and the minimum acceptable signal level in a multiplex system, sometimes expressed in dBV.

Event-based The attribute of transmission of data on a manually triggered event or on change of parametric value.

Event-driven The attribute of an event-based network protocol.

Fault tolerance Ability of a system to survive a certain number of failures while performing its required functions, but possibly with some degraded characteristics.

Frame One complete transmission of information, which may or may not include an in-frame response. The frame is enclosed by the start of frame and end of frame symbols. For Class B networks, each frame contains of only one message. (See **Message** and **Message frame**.)

Framing overhead The framing overhead defines the amount of nondata overhead associated with the given protocol, i.e., framing overhead.

Functional addressing Functional addressing allows a message to be addressed or sent to one or more nodes on the network interested in that function. Functional addressing is intended for messages that may be of interest to more than a single node. For example, a vehicle speed message could be sent to all nodes requiring the vehicle speed using a functional address. Functional addressing is labeling of messages based on their operation code or data content.

Functional superset A Class C multiplex network is defined as a functional superset of Class B and Class A multiplex network, networks that have both physical and functional properties. As a functional superset, the network must be capable of communications that would perform all of the functions of the networks in that set.

Gate A minimum cell composed of transistors which form a circuit to perform a logic function such as NAND or NOR, and typically is used as a size or complexity measure of a component.

Gateway A node used to connect networks that use different protocols, as differentiated from a bridge. A gateway acts as a protocol converter.

Global address The predefined address or ID used as a broadcast to all nodes on the network.

Global time base A clock or timing device relating to, or involving, the entire vehicle network and providing the time base for the time-triggered protocol.

Ground offset Difference in voltage at a ground point as compared to a reference ground point. (See **Longitudinal noise**.)

Handshaking Defines the interaction of nodes within a network in order to effect a transfer of data. This may include such things as negative and positive acknowledgment and in-message acknowledgment.

Header field The header or header field, often used interchangeably, is a one- or three-byte field within a frame which directly or implicitly contains information about the message priority, message source and target addressing, message type, and in-frame response type.

Hexadecimal (Hex) A four-bit digital numbering system using 0, 1, ... A, B, C, D, E, and F to represent all the possible values of a decimal equivalent 0 to 15.

Identifier (ID) The primary ID identifies the target for this functional message and is the primary discriminator used to group functions into main categories.

Idle detection The capability of a circuit to detect the condition of a nondata period.

In-frame acknowledgment The form of the acknowledgment that is expected within that frame.

In-frame response (IFR) The form of the response that is expected within that frame. (See **Response**.)

Initialization Parameterization and eventual configuration of a system during startup.

Interbyte separation (IBS) A condition under which data bytes of an asynchronous serial transmission within a frame are disjointed or separate with variable amounts of dead time between bytes.

Interframe delimiter (IFD) Interframe delimiter (IFD), interframe separation (IFS), and interframe spacing are used interchangeably and refer to a condition under which the frames of an asynchronous serial transmission on a multiplex network are disjointed or separate with variable amounts of dead time between messages as a result of system clock tolerances in order to support synchronization of frames.

Invalid bit A detector system that determines when a data bit has deviated outside the established requirements.

Invalid message structure A detector system that determines when the message frame composition has deviated outside the established requirements.

Latency The time required to transfer a message from the transmitting node measured from the moment it is prepared to send the message until it is correctly received by the targeted receiver. It may include a retry strategy delay if the initial exchange is not successful.

Line driver A solid state device (driver) used to transfer electrical energy to a wire or cable communications medium (signal bus) performing the transmit portion of the transceiver function.

Local area network (LAN) A local multiplex network that can serve a variety of devices. Typically in automotive systems it is used for collecting data from sensors and controlling actuators for one host module.

Longitudinal noise Difference in voltage between two ground points as a result of ground offset electrical noise currents. (See **Ground offset**.)

Manchester (MAN) A digital signaling technique in which there is a transition in the middle of each bit time. A "1" is encoded with a high level during the first half of the bit time and a "0" is encoded with a low level during the second half of the bit time. Therefore, there is a maximum of two transitions per bit time.

Master (node or module) The master node and master module are used interchangeably and are defined as the device which controls the transfer of information on a multiplex network. (See **Master-slave**.)

Master-slave A type of system whereby one node, a module, acts as a master or central unit and controls the actions of the other nodes designated as slaves or remote units.

Media access The method used to award the communication network to one of the nodes for the transmission of a message, e.g., master slave, token passing, CSMA/CD.

Message All of the data bytes contained in a frame. The message is what is left after the frame symbols have been removed from the frame. As such, the message is the sequence of bytes contained in the frame.

Message frame A portion of a communication protocol within the message transfer specifying the arrangement and meaning of bits or bit fields in the sequence of transfer across the transmission medium. The message frame is what is left after the message has been removed from the frame.

Message latency The time required by a system to access the medium so as to begin the delivery of information. Message latency is measured from the time that a node is ready to send specific information to the time of the start of the transmission of this information, which will ultimately be successful. Thus, the total time required to successfully send a desired message will be the sum of the message latency and the message transmission time.

Message source An identifier that defines the physical origin of a frame of data.

Message transfer The portion of the protocol dealing with the organization, meaning, and timing associated with the bits of data. Message transfer deals with what bits must be sent and when they must be sent to accomplish the transmission of a message.

Message type A classification of the different categories or classes of messages, such as functional or physical.

Modified frequency modulation (MFM) An encoding technique that defines two symmetrically spaced phases, data and clock, to a synchronizing signal. Modulating data causes transitions at these phases depending on the logic level.

Multiple-byte header protocol A protocol that utilizes a number of bytes in the header field within a frame which directly contains information about the message priority, message source and target addressing, message type, and in-frame response type.

Multiplex bus (signal bus) Multiplex bus and signal bus are sometimes used interchangeably and refer to the wiring serving all multiplex system nodes and includes the signal, power, and ground buses.

Multiplexing The process of combining several messages for transmission over the same signal path. There are two widely used methods of multiplexing: time division and frequency division.

Negative acknowledgment A control character on a communications network transmitted from a receiving point as a negative response to the reception of the message. The response signifies that the message was not received correctly.

Network A system capable of supporting communications by three or more nodes.

Network access Method used to award the communications network to one of the nodes for the transmission of a message.

Network topologies The layout of elements capable of supporting communications by three or more nodes.

Node Any subassembly of a multiplex system which communicates on the signal bus, i.e., a transceiver. In addition to modules, nodes may include other devices that contain the intelligence necessary to support these communications.

Nonreturn to zero (NRZ) A data bit format in which the voltage or current value, which is typically voltage, determines the data bit value, i.e., one or zero.

Nondestructive bit-by-bit arbitration Nondestructive bit-by-bit arbitration and bit-by-bit arbitration are used interchangeably and both refer to a contention-based arbitration, whereby the contention created by simultaneous access of multiple nodes on the network is resolved bit by bit. (See **Bit-by-bit arbitration**.)

Normalization bit A VPW modulation bit symbol that follows an end of data symbol used to initialize an in-frame response with the proper phase.

OSI model The open system interconnect (OSI) model defines a seven-layer model for a data communications network.

Parametric data values A parameter is the variable quantity included in some messages. The parameter value, scaling, offset, units, transfer function, etc., are unique to each particular message.

Parity (odd or even) The parity check bit is said to be odd or even when the simple sum of all the binary bits in the frame, including the check bit, is always odd or always even. (See **Parity bit**.)

Parity bit A check bit appended to a frame composed of binary bits to make the simple sum of all the binary bits, including the check bit, always odd or always even.

Parity error An error is determined when the locally calculated parity check bit disagrees with the parity check bit received in the frame.

Physical addressing Labeling of messages for the physical address location of their source and/or destination(s). This is independent of their geographic location, connector pin, and/or wire identification assignments. The information in these messages are only of relevance to particular nodes, so the other nodes on the bus should ignore the message.

Physical layer The properties of the communications medium (signal bus) which can be determined by electrical measurements, such as voltages, currents, impedances, rise times, etc.

Poll The process by which a master device invites a slave device, such as a sensor or actuator, one at a time, to transmit data or to act on command.

Positive acknowledgment A control character on a communications network transmitted from a receiving point as a positive response to the reception of the message. The response signifies that the message was received correctly.

Priority Attribute of a message controlling its ranking during arbitration. A high priority increases the probability that a message wins the arbitration process.

Propagation delay The worst-case or maximum propagation time through a medium such as the circuits of an IC or a multiplex network.

Protocol A formal set of conventions or rules for the exchange of information between nodes, including the procedures for establishing and controlling transmissions on the multiplex signal bus (message administration) and the organization, meaning, and timing associated with the bits of data (message transfer).

Pulse-width variability The variations in pulse-width tolerances associated with variable pulse-width modulation caused by such things as ground offset and the bus driver.

Response A message or portion of a message initiated by a receiving node as a result of a message transmitted by a different node. A response can be an acknowledgment or response data, and it can be appended to the original message (immediate response) or a unique message (separate response).

Response current A system that utilizes change in current signal which is used to indicate whether a message has been received properly.

Response data A response to a message which provides the data or information requested in the message. This may be an in-frame response or a report to requested data.

Serial communications interface (SCI) A common microcomputer interface that provides a standard mark/space (NRZ) which produces one start bit, eight data bits, and one stop bit in a serial data format.

Shadow nodes A node in a time triggered protocol architecture which receives input messages but does not produce any output as long as the other two nodes of the network are operational. As soon as one of these other two nodes fails, the shadow node takes the time division multiple access (TDMA) slot from the failed node and produces output.

Single-byte header protocol A protocol that utilizes a single byte in the header field within a frame which implicitly contains information about the message priority, message source and target addressing, message type, and in-frame response type.

Single-wire random lay Refers to a transmission medium of a multiplex network that consists of a single conductor and a common return that is randomly placed in the wiring harness with all of the other vehicle circuits. The return conductor could be the vehicle chassis or a common ground conductor.

Sleep state (sleep mode) Sleep state and sleep mode are sometimes used interchangeably and refer to the behavior whereby a node is on a low-power consumption standby state waiting to be switched on by a frame or other activity. This is distinct from an off mode where there is no power consumption and it is disconnected from the power supply.

Start bit The bit encoded within an asynchronous transmission that synchronizes the receiver clock to terminate the end of that block or byte of data.

Stop bit The bit encoded within an asynchronous transmission that synchronizes the receiver clock to the start of that block or byte of data.

Symbol The individual elements that compose the message frame such as start of frame (SOF), end of data (EOD), end of frame (EOF), and CRC.

Synchronization Procedure to ensure a desired timing for interrelated actions and/or processes.

System architecture The organization of a multiplex system including, but not necessarily limited to, the location and ranking of logic or decision-making elements and the types and methods of communications between these elements.

T-tap connection A splice in a wiring harness forming a "T" connection. This configuration is associated with an automated insulation displacement type connection at a connector.

Target address The address of the node for which the message is intended. This address is usually the physical address of a particular node.

10-bit NRZ A common microcomputer interface that provides a standard mark/space (NRZ) which produces a total of 10 bits, 1 start bit, 8 data bits, and 1 stop bit in a serial data format. [See **Serial communications interface (SCI)**]

Tightly looped distributed processing A control strategy that acts within the actual time the physical events take place and whereby control elements are physically located in several different places.

Time-critical message The attributes of a message that require action in a very short period of time bordering on real-time control requirements.

Time division multiple access (TDMA) A general classification of multiplexing that utilizes time division multiplex protocols.

Time division multiplex protocol A protocol in which the meaning of a piece of information on the signal bus is determined by its relationship, i.e., first, second, third, etc., to the start of the message or bitstream. In a time division multiplex protocol, data can be interleaved on a bit-by-bit, byte-by-byte, or block-by-block basis.

Time triggered media access Bus access is controlled by a global time base which opens slots to data depending on the network protocol.

Time triggered protocol (TTP) A real-time control system architecture where all system activities are triggered by the progression of real time. This distributed time triggered architecture requires clock synchronization by a global time base.

Token The symbol of authority passed between nodes in a token-passing protocol. Possession of this symbol identifies the node currently in control of the medium.

Token-passing protocol A node that has communicated passes the control of the bus, including the right to communicate to another node, at the end of the message via a token.

Token slot protocol A protocol where bus access is controlled by a time base which opens a time slot to a number of nodes that, in turn, take control of the network when there is data to communicate to another node.

Transceiver An electrical circuit which both transmits (line driver portion) and receives (line receiver portion).

Transitions (bit) The process of changing from one voltage level to another voltage level.

Translated The conversion from one binary number to another binary number in order to achieve correct bit-by-bit arbitration.

Trapezoidal waveforms A sawtooth waveform superimposed onto a square wave.

Twisted pair A transmission line consisting of two similar conductors that are insulated from each other and are twisted around each other to form a communications channel. The purpose for twisting the conductors around each other is to reduce the electric and magnetic field interaction with other conductors.

Variable pulse-width (VPW) modulation (VPWM) A method of using both bus state and pulse width to encode bit information. This encoding technique is used to reduce the number of bus transitions for a given bit rate. One embodiment would define a "1" as a dominant short pulse or a passive long pulse while a "0" would be defined as a long dominant pulse or a short passive pulse. Since a message is composed of random "1"s and "0"s, general byte or message times cannot be predicted in advance.

Wake-up The process of activating a node that is in the sleep state.

Wave-shaped A technique of rounding the corners of a trapezoidal waveform in order to significantly minimize the EMI.

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Fred Miesterfeld is engineering supervisor of the advanced electronic development at Chrysler Corporation. A graduate of Johns Hopkins University with over 25 years of experience in automotive electronics, he has been an active member of various SAE Standards Committees since 1975. Presently, he is serving as chairman of the Vehicle Networks for Multiplexing and Data Communications Committee and previously has served as Secretary of the EMI Standards and Test Methods Committee.

P · A · R · T · 6

ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY

CHAPTER 27
ELECTROMAGNETIC STANDARDS AND INTERFERENCE

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27.1 SAE AUTOMOTIVE EMC STANDARDS

27.1.1 Overview

The Society of Automotive Engineers (SAE) has been involved in writing electromagnetic compatibility standards since 1957 with SAE-J551. In its original form, SAE-J551 was intended to protect "roadside receivers," particularly television, from vehicle ignition noise. There have been several revisions to SAE-J551 and new electromagnetic compatibility standards due to the evolution of digital electronics. With the implementation of digital electronic systems on vehicles, a new set of radio noise problems prompted a new standard to be written in 1987.

This chapter will review the Society of Automotive Engineers (SAE) Electromagnetic Compatibility (EMC) standards on both vehicle system level and component-level test methods. The Electromagnetic Radiation (EMR) and Electromagnetic Interference (EMI) Standards Committees are working together to cover all aspects of the EMC field and to develop test methods and limits relating to vehicle and other motorized equipment. Each of the committees has representation from automotive corporations, truck and bus corporations, suppliers, consumers, test houses, and government.

Presently, the Society of Automotive Engineers EMC Standards Committees are revising SAE J1113 and SAE J551 to create documents made up of multiple parts, covering all aspects of component and vehicle testing. SAE EMC standards are being harmonized with those of the International Standards Organization (ISO). The vehicle-level EMC standard, SAE J551, is divided into emissions test parts numbered 2 through 10 (Table 27.1) and immunity test parts numbered 11 through 20 (Table 27.2). The component-level EMC standard, SAE J1113, is divided into immunity test parts numbered 2 through 40 (Table 27.3) and emissions test parts numbered above 40 (Table 27.4). Part 1 of both documents contains an introduction and definitions. The SAE standards are structured to be living documents to accept changes and additions without the need to revise or renumber parts.

TABLE 27.1 EMC Emissions Tests for Vehicles—SAE J551

SAE J551 part	Bandwidth	Frequency range	Test distance	Comparable standard
2	Broadband	30 MHz—1 GHz	10 m	CISPR 12
3	Narrowband	10 kHz—1 GHz	3 m	CISPR TBD
4	Narrow & broad	150 kHz—1 GHz	1 m	CISPR TBD
5	Narrow & broad	20 kHz—1 GHz	10 m	CISPR TBD

TABLE 27.2 EMC Immunity Tests for Vehicles—SAE J551

SAE J551 part	Test type	Frequency range	Comparable standard
11	Off vehicle source	500 kHz—18 GHz	ISO 11451/2
12	On vehicle source	1.8 MHz—1.2 GHz	ISO 11451/3
13	Bulk current injection	1—400 MHz	ISO 11451/4
14	Reverberation chamber	200 MHz—18 GHz	None
15	Electrostatic discharge	N/A	ISO 10605
16	Transients	N/A	None
17	Power line magnetic field	60 Hz—30 kHz	None

TABLE 27.3 EMC Immunity Tests for Components—SAE J1113

SAE J1113 part	Test type	Frequency range	Comparable standard
2	Conducted immunity	30 Hz—250 kHz	None
3	Conducted immunity	100 kHz—400 MHz	ISO 11452/7
4	Bulk current injection	1—400 MHz	ISO 11452/4
11	Transients	N/A	ISO 7637-1
12	Coupled transients	N/A	ISO 7637-3
13	Electrostatic discharge	N/A	ISO 10605
21	Semi-anechoic chamber	30 MHz—18 GHz	ISO 11452/2
22	Power line magnetic	60 Hz—30kHz	None
23	RF stripline	10 kHz—1 GHz	ISO 11452/5
24	TEM cell	10 kHz—200 MHz	ISO 11452/3
25	Triplate	10 kHz—1 GHz	None
26	Power line E-field	60 Hz—30 kHz	None
27	Reverberation chamber	500 MHz—2 GHz	None

TABLE 27.4 EMC Emissions Tests for Components—SAE J1113

SAE J1113 part	Test type	Frequency range	Comparable standard
41	Narrowband	10 kHz—1 GHz	CISPR TBD
42	Transient	N/A	ISO 7637-1

27.1.2 SAE J551

Note: This section contains portions reprinted with permission from Draft SAE J551 ©1993 Society of Automotive Engineers, Inc.

SAE J551 combines all of the vehicle-level automotive-related EMC test methods for emissions and immunity tests into one document. The contents of the SAE J551 are as follows.

SAE J551/1 General and Definitions

Absorber lined chamber A shielded room with absorbing material on its internal reflective surfaces (floor absorber material optional).

Amplitude modulation (AM) The process by which the amplitude of a carrier wave is varied following a specific law. The result of that process is an AM signal.

Antenna correction factor The factor that is applied to the voltage measured at the input connector of the measuring receiver to give the field strength at the antenna.

Antenna matching unit A unit for matching the impedance of an antenna to that of the 50-ohm measuring receiver over the antenna measuring frequency range.

Artificial network (AN) A network inserted in the supply leads of an apparatus to be tested which provides, in a given frequency range, a specified load impedance for the measurement of disturbance voltages and which isolates the apparatus from the power supply in that frequency range.

Bandwidth The width of the frequency band over which a given characteristic of an equipment does not differ from its reference by more than a specified amount or ratio.

Broadband artificial network (BAN) A network that presents a controlled impedance to the device under test over a specified frequency range while allowing the device under test to be interfaced to its support system. It is used in power, signal, and control lines.

Broadband emission An emission which has a bandwidth greater than that of a particular measuring apparatus or receiver.

Bulk current Total amount of common mode current in a harness.

Bulk current injection probe A device for injecting current in a conductor without interrupting the conductor and without introducing significant impedance into the associated circuits.

Characteristic level The controlling (or dominant) emission level experienced in each frequency subband. The characteristic level is the maximum measurement obtained for both antenna polarizations and for all the specified measurement positions of the vehicle or device. Known ambient signals shall not be considered part of the characteristic level.

Class An arbitrary performance level agreed upon by the purchaser and the supplier and documented in the test plan.

Component continuous conducted emissions The noise voltages/currents of a continuous nature existing on the supply or other wires of a component/module which may cause interference to reception in an on-board receiver.

Compression point The input signal level at which the gain of the measuring system becomes nonlinear such that the indicated output deviates from an ideal receiving system's output by the specified increment in dB.

Coupling A means or a device transferring power between systems.

Current (measuring) probe A device for measuring the current in a conductor without interrupting the conductor and without introducing significant impedance into the associated circuits.

Degradation (of performance) An undesired departure in the operational performance of any device, equipment, or system from its intended performance.

Device A machine equipped with an internal combustion engine but not self-propelled. Devices include, but are not limited to, chain saws, irrigation pumps, and air compressors.

Directional coupler A three- or four-port device consisting of two transmission lines coupled together in such a manner that a single traveling wave in any one transmission line will induce a single traveling wave in the other, the direction of propagation of the latter wave being dependent upon that of the former.

Disturbance suppression Action which reduces or eliminates electrical disturbance.

Disturbance voltage; interference voltage Voltage produced between two points on separate conductors by an electromagnetic disturbance, measured under specified conditions.

Electromagnetic compatibility (EMC) The ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbance to anything in that environment.

Electromagnetic disturbance Any electromagnetic phenomenon which may degrade the performance of a device, equipment, or system or adversely affect living or inert matter.

Electromagnetic immunity (to a disturbance) The ability of a device, equipment, or system to perform without degradation in the presence of an electromagnetic disturbance.

Electromagnetic interference (EMI) Degradation of the performance of an equipment, transmission channel or system caused by an electromagnetic disturbance.

Electromagnetic radiation The phenomena by which energy in the form of electromagnetic waves emanates from a source into space; energy transferred through space in the form of electromagnetic waves.

Forward power Power supplied by the output of an amplifier (or generator) traveling towards the load.

Ground (reference) plane A flat conductive surface whose potential is used as a common reference.

Ignition noise suppressor That part of a high-voltage ignition circuit intended to limit the emission of impulsive ignition noise.

Immunity level The maximum level of a given electromagnetic disturbance incident on a particular device, equipment, or system for which it remains capable of operating at a required degree of performance.

Impulse electric field strength The root-mean-square value of the sinusoidally varying radiated electric field producing the same peak response in a bandpass system, antenna, and bandpass filter, produced by the unknown impulse electric field.

Impulse noise Noise characterized by transient disturbances separated in time by quiescent intervals. The frequency spectrum of these disturbances must be substantially uniform over the useful pass band of the transmission system. The same source may produce impulse noise in one system and random noise in a different system (from ANSI/IEEE Std 100).

Impulsive ignition noise The unwanted emission of electromagnetic energy, predominantly impulsive in content, arising from the ignition system within a vehicle or device.

Interference suppression Action which reduces or eliminates electrical interference.

Measuring instrument impulse bandwidth The maximum value of the output response envelope divided by the spectrum amplitude of an applied impulse.

Narrowband emission An emission which has a bandwidth less than that of a particular measuring apparatus or receiver.

Net power Forward power minus reflected power.

Peak detector A detector, the output voltage of which is the peak value of the applied signal.

Polarization (of a wave or field vector) The property of a sinusoidal electromagnetic wave or field vector defined at a fixed point in space by the direction of the electric field strength vector or of any field vector; when the direction varies with time, the property may be characterized by the locus described by the extremity of the considered field vector.

Quasi-peak detector A detector having specified electrical time constants which, when regularly repeated identical pulses are applied to it, delivers an output voltage which is a fraction of the peak value of the pulses, the fraction increasing toward unity as the pulse repetition rate is increased.

Receiver terminal voltage (antenna voltage) The voltage generated by a source of radio disturbance and measured in dB (μV) by a radio interference measuring receiver conforming to the requirements of CISPR Publications 16 or ANSI C63.2.

Reflected power Power traveling toward the generator reflected by the load due to impedance mismatch between the transmission line and the load.

Resistive distributor brush The resistive pick-up brush in an ignition distributor cap.

RF ambient (electromagnetic environment) The totality of electromagnetic phenomena existing at a given location.

Shall Used to express a command, i.e., conformance with the specific recommendation is mandatory and deviation is not permitted. The use of shall is not qualified by the fact that compliance with the standard is considered voluntary.

Shielded enclosure A mesh or sheet metallic housing designed for the purpose of separating the internal from external electromagnetic environment.

Standing wave ratio (SWR); voltage standing wave ratio (VSWR) The ratio, along a transmission line, of a maximum to an adjacent minimum magnitude of a particular field component of a standing wave.

Tracking generator A narrowband radio frequency source synchronized to the instantaneous receive frequency of a scanning receiver or spectrum analyzer.

Transmission line system (TLS) A transmission line system is a stripline or parallel plate or similar device to generate an E-field.

Vehicle A self-propelled machine (excluding aircraft, rail vehicles, and boats over 10 m in length). Vehicles may be propelled by an internal combustion engine, electrical means, or both. Vehicles include, but are not limited to, mopeds, automobiles, trucks, agricultural tractors, snowmobiles, and small motorboats.

SAE J551/2 Performance Levels and Methods of Measurement of Electromagnetic Radiation from Vehicles and Devices, Broadband, 30 to 1000 MHz. This document provides test procedures and recommended levels to assist engineers in the measurement of broadband electromagnetic radiation and control of radio interference.

SAE J551/3 Performance Levels and Methods of Measurement of Electromagnetic Radiation from Vehicles and Devices, Narrowband, 10 kHz to 1000 MHz. This document covers methods of measuring incidental narrowband radiation from vehicles and devices and establishes performance levels intended to protect nearby communication and broadcast receivers.

SAE J551/4 Test Limits and Methods of Measurement of Radio Disturbance Characteristics from Vehicles and Devices, Narrowband, 150 kHz to 1000 MHz. This document provides measurement techniques and test limits intended to protect radio receivers installed in a vehicle from disturbances produced by components/modules in the same vehicle.

SAE J551/5 Performance Levels and Methods of Measurement of Electromagnetic Radiation from Electric Vehicles, Broadband and Narrowband, 9 kHz to 1000 MHz. This document provides electric vehicle test procedures and performance levels for the measurement of both radiated magnetic and electric field strengths.

SAE J551/11 Vehicle Electromagnetic Immunity—Off-Vehicle Source. This document adopts ISO CD11451-2: Road Vehicles—Electrical Disturbances by Narrowband Radiated Electromagnetic Energy—Vehicle Test Methods—Part 2: Off-vehicle Radiation Source.

SAE J551/12 Vehicle Electromagnetic Immunity—On-board Transmitter Simulation. This document adopts ISO CD11451-3: Road Vehicles—Electrical Disturbances by Narrowband Radiated Electromagnetic Energy—Vehicle Test Methods—Part 3: On-board Transmitter Simulation.

SAE J551/13 Vehicle Electromagnetic Immunity—Bulk Current Injection (BCI). This document adopts ISO CD11451-4: Road Vehicles—Electrical Disturbances by Narrowband Radiated Electromagnetic Energy—Vehicle Test Methods—Part 4: Bulk Current Injection.

SAE J551/15 Vehicle Electromagnetic Immunity—Electrostatic Discharge (ESD). This document adopts the portions of ISO TR10605 which pertain to ESD calibration and vehicle ESD testing.

27.1.3 SAE J1113

Note: This section contains portions reprinted with permission from Draft SAE J1113 ©1993 Society of Automotive Engineers, Inc.

SAE J1113 combines all of the module-level automotive-related EMC test methods for emissions and immunity tests into one document. The contents of the SAE J1113 are as follows.

SAE J1113/1 General and Definitions

Ambient Level Those levels of radiated and conducted signal and noise existing at a specified test location and time when the test sample is not in operation. Atmospherics, interference from other sources, and circuit noise or other interference generated within the measuring set compose the ambient level.

Conducted emission Desired or undesired electromagnetic energy which is propagated along a conductor.

Device under test (DUT) The device whose immunity is being checked.

Electromagnetic compatibility (EMC) The condition that enables equipment, subsystems, and systems (electronic, chemical, biological, etc.) to function without degradation from electromagnetic sources and without degrading the electromagnetic environment; i.e., it is the condition which allows the coexistence of different electromagnetic sources without significant change in performance of any one in the presence of any or all the other.

Emission Electromagnetic energy propagated from a source by radiation or conduction.

Equipment under test (EUT) The device or system whose immunity is being checked. Synonymous with DUT.

Field decay (voltage) The exponentially decaying negative voltage transient such as developed by an automotive alternator when the field excitation is suddenly removed, as when the ignition switch is turned off.

Field strength The term *field strength* shall be applied to either the electric or the magnetic component of the field, and may be expressed as V/m or A/m. When measurements are made in the far field and in free space, the power density in W/cm^2 may be obtained from field strengths approximately as (V/m)/377 or (A/m) × 377. When measurements are made in the near field and in free space, both the complex electric and magnetic vector components of the field must be fully defined. Power density may then be obtained by use of the Poynting vector.

Ground plane A metal sheet or plate used as a common unipotential reference point for circuit returns and electrical or signal potential.

Immunity A measure of electronic module or system tolerance to external electromagnetic fields. decaying posit

Load dump (voltage) The exponentially live voltage transient developed by an automotive alternator, when disconnected suddenly from its load, while operating without a storage battery or with a discharged storage battery. Removal of the load, the resulting transient, or both in combination are commonly referred to as alternator load dump.

Radiated emission Radiation- and induction-field components in space. (For the purpose of this document, induction fields are classed together with radiation fields.)

Spurious emission Any unintentional electromagnetic emission from a device.

Susceptibility The characteristic of an object that results in undesirable responses when subjected to electromagnetic energy.

Test plan The specific document that details all tests and limits for the particular device in question.

SAE J1113/2 Conducted Immunity (30 Hz to 250 kHz). This document provides the requirements for determining the immunity characteristics of automotive electronic equipment, subsystems, and systems to EM energy injected onto all leads over the frequency range of 30 Hz to 250 kHz. The method is applicable to all input, output, and power leads.

SAE J1113/3 Conducted Immunity (100 kHz to 400 MHz). This document provides the requirements for determining the immunity characteristics of automotive electronic equipment, subsystems, and systems to electromagnetic energy injected onto all leads, including signal and power, over the frequency range 100 kHz to 400 MHz.

SAE J1113/4 Immunity to Radiated Electric Fields—Bulk Current Injection Method (1 to 400 MHz). This document provides a test method for evaluating the immunity of automotive electrical/electronic devices to radiated electromagnetic fields coupled to the vehicle wiring harness. Bulk current injection (BCI) uses a current probe to inject RF current from 1 to 400 MHz into the wiring harness of automotive devices.

SAE J1113/11 Immunity to Conducted Transients on Power Leads. This document provides the methods and apparatus to evaluate electronic devices for immunity to potential interference from conducted transients along battery feed or switched ignition inputs. The test apparatus specifications outlined in this procedure were developed for 12-V passenger cars and light trucks, 12-V heavy-duty trucks, and vehicles with 24-V systems.

SAE J1113/12 Electrical Interference by Conduction and Coupling—Coupling Clamp. This document provides a common basis for the evaluation of devices and equipment in vehicles

against transient transmission by coupling via lines other than the power supply lines. The test demonstrates the immunity of the instrument, device, or equipment to coupled fast transient disturbances, such as those caused by switching of inductive loads, relay contact bouncing, etc.

SAE J1113/13 Immunity to Electrostatic Discharge (ESD). This document provides the test methods and procedures necessary to evaluate electrical components intended for automotive use to the threat of electrostatic discharges.

SAE J1113/21 Radiated Immunity Using an Absorber Lined Chamber—Far Field. This document provides the test methods and procedures for testing electromagnetic immunity (off vehicle radiation sources) of electronic components for passenger cars and commercial vehicles. To perform this test method, the electronic module, along with the wiring harness (prototype or standard test harness) and peripheral devices, will be subjected to the electromagnetic disturbance generated inside an absorber-lined chamber.

SAE J1113/22 Immunity to Radiated Magnetic Fields from Power Lines. This document provides the testing technique for determining the immunity of automotive electronic devices to magnetic fields generated by power transmission lines and generating stations.

SAE J1113/23 Radiated Immunity—Stripline Method. This document provides recommended testing techniques for the determination of electric field immunity of an automotive electronic device when the device equipment harness is exposed to an interference RF field. This technique uses a stripline coupler from 10 kHz to 1 GHz and is limited to harnesses (and/or samples) which have a maximum height of equal to or less than one-third the stripline height.

SAE J1113/24 Radiated Immunity—Transverse Electromagnetic Mode (TEM) Cell. This SAE document adopts ISO CD11452-3: Road Vehicles—Electrical Disturbances by Narrowband Electromagnetic Energy—Component Test Methods—Part 3: TEM Cell. It provides test methods and procedures for testing electromagnetic immunity of electronic components for passenger cars and commercial vehicles. The electromagnetic disturbance, considered in this part of ISO CD11452, will be limited to continuous narrowband electromagnetic fields.

SAE J1113/25 Radiated Immunity—Triplate Line Method. This document provides testing techniques for the determination of electric field immunity of an automotive electronic device when the device equipment harness is exposed to an interference RF field. This technique uses a Tri-Plate Line (TPL) from 10 kHz to 1 GHz and is limited to components which have a maximum height of equal to or less than one-third the height between the driven element and the outer, grounded plates.

SAE J1113/26 Radiated Immunity—60 Hz E-field. This document provides testing techniques using a parallel plate antenna and a low-current, high-voltage generator for the determination of electric field immunity of an automotive electronic device when the device and its equipment harness are exposed to a 60-Hz electric field.

SAE J1113/27 Immunity to Radiated Electromagnetic Fields (Reverberation) Method. This document provides the reverberation test method to evaluate the immunity of electronic devices in the frequency range of 500 MHz to 2.0 GHz. The reverberation test data correlates with vehicle-level radiated immunity test data in the anechoic chamber and mobile transmitter sites.

SAE J1113/41 Test Limits and Methods of Measurement of Radio Disturbance Characteristics from Vehicle Components and Modules, Narrowband, 150 kHz to 1000 MHz. This document provides test limits and procedures for the measurement of radio disturbances produced by components/modules in the same vehicle.

SAE J1113/42 Conducted Transient Emissions. This document provides a component-level test procedure to evaluate the automotive electrical and electronic components for conducted emissions of transients, and for other electromagnetic disturbances. The test apparatus specifications in this procedure were developed for components installed in 12-V passenger cars and light trucks.

27.2 IEEE STANDARDS RELATED TO EMC

Although some of the following standards were not developed in the EMC Society (EMCS), they were developed with EMCS input and coordination. (Following each item, the letters in parentheses are the initials of the developing society, and the numbers in square brackets are IEEE order numbers.)

27.2.1 IEEE Standard 139-1988

IEEE Recommended Practice for the Measurement of Radio Frequency Emission from Industrial, Scientific, and Medical (ISM) Equipment Installed on User's Premises. (EMCS) [SH12377]

27.2.2 IEEE Standard 140-1990

IEEE Recommended Practice for Minimization of Interference from Radio-Frequency Heating Equipment. (EMCS) [SH13581]

27.2.3 IEEE Standard 187-1990

IEEE Standard of Radio Receivers: Open Field Method of Measurement of Spurious Radiation from FM and Television Broadcast Receivers. (EMCS) [SH13698]

27.2.4 ANSI/IEEE Standard 211-1990

IEEE Standard Definitions of Terms for Radio Wave Propagation. (APS) [SH13904]

27.2.5 ANSI/IEEE Standard 213-1987

IEEE Standard Procedure for Measuring Conducted Emissions in the Range of 300 kHz to 25 MHz from Television and FM Broadcast Receivers to Power Lines. (EMCS) [SH12047]

27.2.6 IEEE Standard 291-1969 (Reaff 1981)

IEEE Standards Report on Measuring Field Strength in Radio Wave Propagation. (APS) [SH01800]

27.2.7 IEEE Standard 299-1991

IEEE Standard Method for Measuring the Effectiveness of Electromagnetic Shielding Enclosures. (EMCS) [SH14134]

27.2.8 IEEE Standard 368-1977

IEEE Recommended Practice for Measurement of Electrical Noise and Harmonic Filter Performance of High-Voltage Direct-Current Systems. (COMSOC) [SH07021]

27.2.9 ANSI/IEEE Standard 376-1975 (Reaff 1980)

IEEE Standard for the Measurement of Impulse Strength and Impulse Bandwidth. (EMCS) [SH03764]

27.2.10 ANSI/IEEE Standard 377-1980 (Reaff 1986)

IEEE Recommended Practice for Measurement of Spurious Emission from Land-Mobile Communication Transmitters. (EMCS) [SH07898]

27.2.11 ANSI/IEEE Standard 430-1986

IEEE Standard Procedures for the Measurement of Radio Noise from Overhead Power Lines and Substations. (PES) [SH10801]

27.2.12 ANSI/IEEE Standard 469-1988

IEEE Recommended Practice for Voice-Frequency Electrical-Noise Tests of Distribution Transformers. (COMSOC) [SH12328]

27.2.13 ANSI/IEEE Standard 473-1985

IEEE Recommended Practice for an Electromagnetic Site Survey (10 kHz to 10 GHz). (EMCS) [SH09134]

27.2.14 ANSI/IEEE Standard 475-1983

IEEE Measurement Procedure for Field Disturbance Sensors (RF Intrusion Alarm). (EMCS) [SH08433]

27.2.15 ANSI/IEEE Standard 518-1982 (Reaff 1990)

IEEE Guide for the Installation of Electrical Equipment to Minimize Noise Inputs to Controllers from External Sources. (IAS) [SH08813]

27.2.16 ANSI/IEEE Standard 539-1979

IEEE Standard Definitions and Terms Relating to Overhead Power Lines Corona and Radio Noise. (PES) [SH06882]

27.2.17 ANSI/IEEE Standard 539a-1984

Supplement to IEEE Standard 539-1979. (PES) [SH09530]

27.2.18 ANSI/IEEE Standard 644-1987

IEEE Standard Procedures for Measurement of Power Frequency Electric and Magnetic Fields from AC Power Lines. (PES) [SH10892]

27.2.19 ANSI/IEEE Standard 776-1987

IEEE Guide for Inductive Coordination of Electric Supply and Communication Lines. (COMSOC) [SH11239]

27.2.20 IEEE Standard 1027-1984

Draft Trial-Use Standard Method for Measuring the Magnetic Field Intensity Around a Telephone Receiver. (COMSOC) [SH09497]

27.3 THE ELECTROMAGNETIC ENVIRONMENT OF AN AUTOMOBILE ELECTRONIC SYSTEM

Note: Parts of this section were taken from the article of the same name by J. P. Muccioli and S. S. Awad published in the *IEEE Transactions on Electromagnetic Compatibility,* Aug. 1987.

This work was performed to study the electromagnetic environmental conditions in a typical midsize automobile with a high-power frequency modulation (FM) transmitter installed inside the vehicle. Different antenna locations were used to radiate the electromagnetic waves that were studied. The data obtained from the experimental results is presented and discussed.

27.3.1 Test Methodology

The levels of the electric field strength inside the vehicle depend on a number of factors. One basic factor is the size of the automobile. In this case, a midsize automobile was used for experimentation. The electromagnetic source was selected to be a 100-W FM transmitter operating on five frequencies: 25.04, 35.04, 39.04, 51.20, and 144.50 MHz. The transmitting antenna was placed at four different locations on the outer surface of the vehicle as shown in Fig. 27.1. The transmitter was placed on the passenger seat and was connected to the radiating antenna through a coaxial cable. The electromagnetic environment was mapped inside the vehicle with both doors closed, engine running at idle, and the driver seated in the left front seat. The electric field strength measurements were taken at 15 different locations inside the vehicle, as shown in Fig. 27.2. At each location, the electric field strength was measured once in a direction parallel to the transmitting antenna and once orthogonal to it.

An important factor that can influence the magnitude of the electric field strength is that of ground plane. For this test, the vehicle was placed outside in the open, on dry ground, and away from any other building or vehicles which could affect the electromagnetic environment inside.

27.3.2 Test Instrumentation

1. Field strength meter—IFI, EFS-1, frequency range 10 kHz to 220 MHz
2. Motorola Transmitter 90/100-W power amplifier
   a. Frequency 25.04 MHz @ 100 W
   b. Frequency 35.04 MHz @ 100 W

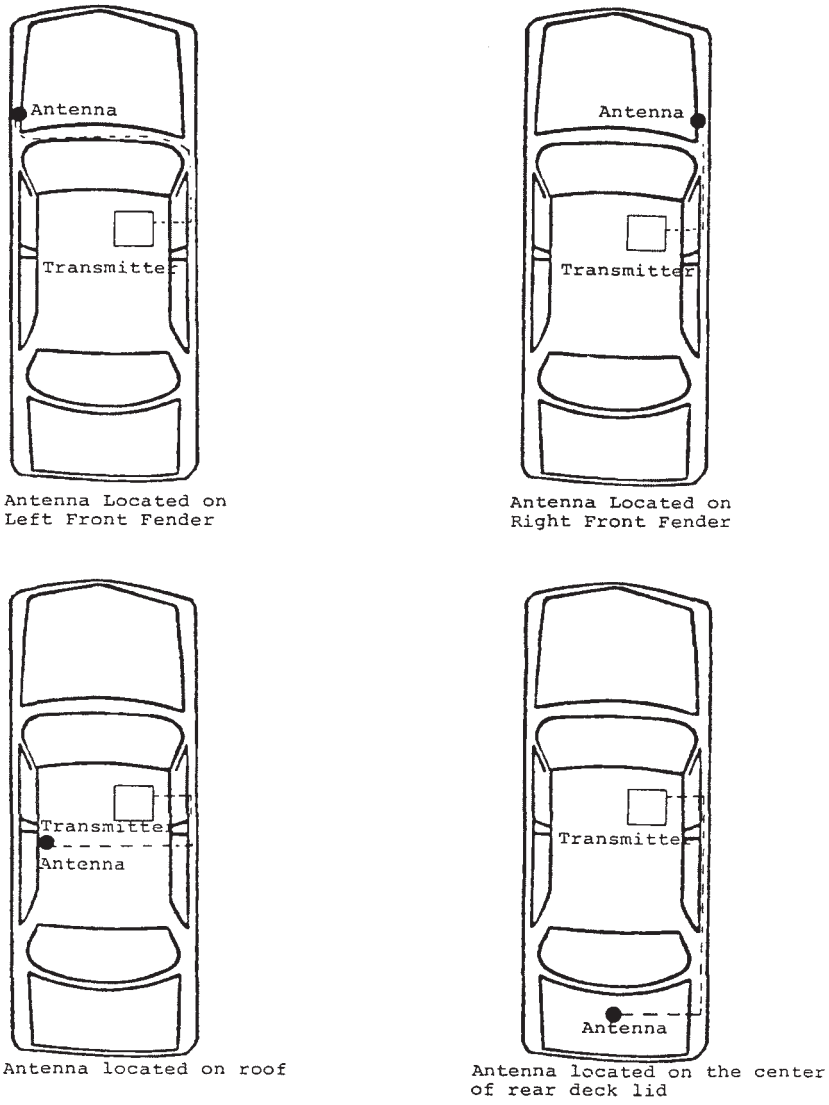


FIGURE 27.1 Antenna locations and coaxial cable routing.

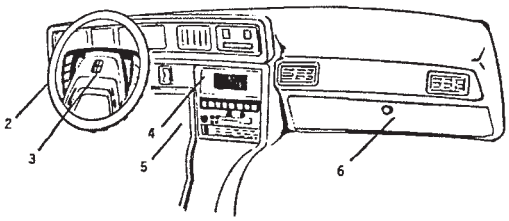
c. Frequency 39.04 MHz @ 100 W

d. Frequency 51.20 Mhz @ 100 W

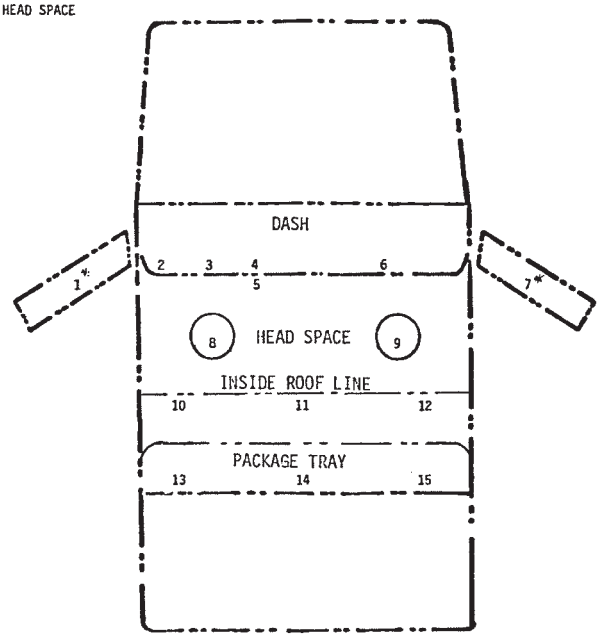
3. Drake UV-3 FM transceiver, 160 W RF power amplifier, frequency 144.50 MHz @ 100 W

27.3.3 Summary

The results of the electric field measurements are shown in Table 27.5. For each of the four antenna locations, the electric field strength components (parallel and orthogonal to the



1. LEFT DOOR TRIM PANEL AT DOOR HANDLE
2. LOWER LEFT SIDE OF DASH PANEL
3. STEERING WHEEL
4. CENTER OF DASH PANEL
5. LOWER CENTER OF DASH PANEL
6. GLOVE COMPARTMENT
7. RIGHT DOOR TRIM PANEL AT DOOR HANDLE
8. DRIVER HEAD SPACE
9. PASSENGER HEAD SPACE
10. LEFT INSIDE ROOF LINE BEHIND SUN ROOF
11. CENTER INSIDE ROOF LINE BEHIND SUN ROOF
12. RIGHT INSIDE ROOF LINE BEHIND SUN ROOF
13. LEFT SIDE OF PACKAGE TRAY
14. CENTER OF PACKAGE TRAY
15. RIGHT SIDE OF PACKAGE TRAY



* NOTE: DOOR MEASUREMENTS WERE MADE AT ARM REST ABOVE DOOR HANDLE

FIGURE 27.2 Fifteen metered locations inside the vehicle.

antenna) are listed for the 15 different meter locations at various transmitting frequencies. From Table 27.5, the electric field environment inside the vehicle could be divided into three different groups:

1. Locations of electric field strengths greater than 150 V/m
   - **a.** Left door trim panel at door handle
   - **b.** Left inside roof line behind sunroof
   - **c.** Right inside roof line behind sunroof
   - **d.** Steering wheel

TABLE 27.5 Field Strength Data at Various Meter Locations

Antenna location on vehicle: left front fender (driver side)

Meter location	Frequency of transmitter 25.04 MHz @ 100 W		Frequency of transmitter 35.04 MHz @ 100 W		Frequency of transmitter 39.04 MHz @ 100 W		Frequency of transmitter 51.2 MHz @ 100 W		Frequency of transmitter 144.5 MHz @ 100 W	
	Field strength parallel to antenna	Field strength orthogonal to antenna	Field strength parallel to antenna	Field strength orthogonal to antenna	Field strength parallel to antenna	Field strength orthogonal to antenna	Field strength parallel to antenna	Field strength orthogonal to antenna	Field strength parallel to antenna	Field strength orthogonal to antenna
1	30 V/M	130 V/M	8 V/M	29 V/M	5 V/M	95 V/M	10 V/M	100 V/M	0 V/M	0 V/M
2	20 V/M	35 V/M	18 V/M	30 V/M	15 VLM	25 V/M	45 V/M	70 V/M	27 V/M	21 V/M
3	22 V/M	220 V/M	13 V/M	58 V/M	19 V/M	160 V/M	24 V/M	175 V/M	13 V/M	15 V/M
4	28 V/M	29 V/M	30 V/M	60 V/M	17 V/M	29 V/M	31 V/M	30 V/M	10 V/M	10 V/M
5	27 V/M	24 V/M	28 V/M	11 V/M	18 V/M	13 V/M	25 V/M	10 V/M	11 V/M	10 V/M
6	28 V/M	20 V/M	48 V/M	60 V/M	17 V/M	14 V/M	20 V/M	35 V/M	21 V/M	28 V/M
7	55 V/M	260 V/M	20 V/M	130 V/M	30 V/M	100 V/M	26 V/M	100 V/M	11 V/M	40 V/M
8	29 V/M	13 V/M	8 V/M	12 V/M	30 V/M	20 V/M	35 V/M	50 V/M	10 V/M	19 V/M
9	17 V/M	29 V/M	0 V/M	5 V/M	30 V/M	35 V/M	30 V/M	12 V/M	10 V/M	10 V/M
10	40 V/M	17 V/M	28 V/M	5 V/M	120 V/M	35 V/M	85 V/M	22 V/M	12 V/M	0 V/M
11	40 V/M	15 V/M	35 V/M	5 V/M	110 V/M	30 V/M	100 V/M	27 V/M	9 V/M	0 V/M
12	35 V/M	14 V/M	40 V/M	2 V/M	90 V/M	30 V/M	81 V/M	25 V/M	15 V/M	1 V/M
13	0 V/M	0 V/M	0 V/M	0 V/M	4 V/M	5 V/M	17 V/M	24 V/M	27 V/M	3 V/M
14	0 V/M	0 V/M	0 V/M	0 V/M	5 V/M	2 V/M	20 V/M	8 V/M	30 V/M	3 V/M
15	0 V/M	0 V/M	0 V/M	0 V/M	5 V/M	2 V/M	21 V/M	13 V/M	20 V/M	3 V/M

Antenna location on vehicle: right front fender

Meter location	Frequency of transmitter 25.04 MHz @ 100 W		Frequency of transmitter 35.04 MHz @ 100 W		Frequency of transmitter 39.04 MHz @ 100 W		Frequency of transmitter 51.2 MHz @ 100 W		Frequency of transmitter 144.5 MHz @ 100 W	
	Field strength parallel to antenna	Field strength orthogonal to antenna	Field strength parallel to antenna	Field strength orthogonal to antenna	Field strength parallel to antenna	Field strength orthogonal to antenna	Field strength parallel to antenna	Field strength orthogonal to antenna	Field strength parallel to antenna	Field strength orthogonal to antenna
1	5 V/M	70 V/M	1 V/M	30 V/M	2 V/M	32 V/M	12 V/M	58 V/M	0 V/M	5 V/M
2	2 V/M	5 V/M	18 V/M	19 V/M	14 V/M	17 V/M	90 V/M	85 V/M	5 V/M	10 V/M
3	0 V/M	18 V/M	5 V/M	70 V/M	15 V/M	90 V/M	55 V/M	115 V/M	5 V/M	2 V/M
4	10 V/M	11 V/M	15 V/M	28 V/M	14 V/M	40 V/M	8 V/M	73 V/M	15 V/M	52 V/M
5	5 V/M	5 V/M	19 V/M	18 V/M	16 V/M	13 V/M	8 V/M	10 V/M	12 V/M	12 V/M
6	13 V/M	30 V/M	52 V/M	55 V/M	30 V/M	35 V/M	11 V/M	15 V/M	10 V/M	18 V/M
7	12 V/M	180 V/M	14 V/M	140 V/M	5 V/M	50 V/M	18 V/M	220 V/M	5 V/M	11 V/M
8	2 V/M	0 V/M	11 V/M	11 V/M	35 V/M	13 V/M	20 V/M	8 V/M	20 V/M	5 V/M
9	1 V/M	10 V/M	16 V/M	20 V/M	30 V/M	24 V/M	35 V/M	8 V/M	11 V/M	11 V/M
10	14 V/M	1 V/M	110 V/M	27 V/M	80 V/M	26 V/M	48 V/M	16 V/M	20 V/M	5 V/M
11	17 V/M	2 V/M	100 V/M	16 V/M	80 V/M	30 V/M	53 V/M	11 V/M	18 V/M	5 V/M
12	18 V/M	8 V/M	100 V/M	23 V/M	75 V/M	23 V/M	62 V/M	13 V/M	17 V/M	5 V/M
13	8 V/M	8 V/M	5 V/M	5 V/M	3 V/M	3 V/M	10 V/M	8 V/M	24 V/M	10 V/M
14	8 V/M	8 V/M	5 V/M	5 V/M	5 V/M	1 V/M	10 V/M	3 V/M	30 V/M	3 V/M
15	10 V/M	35 V/M	5 V/M	5 V/M	3 V/M	2 V/M	8 V/M	5 V/M	14 V/M	5 V/M

2. Locations of electric field strengths between 50 and 150 V/m
   - **a.** Center of dash panel
   - **b.** Center of package tray
   - **c.** Driver head space
   - **d.** Glove compartment
   - **e.** Lower center of dash panel

TABLE 27.5 Field Strength Data at Various Meter Locations (*Continued*)

Antenna location on vehicle: roof

Meter location	Frequency of transmitter 25.04 MHz @ 100 W		Frequency of transmitter 35.04 MHz @ 100 W		Frequency of transmitter 39.04 MHz @ 100 W		Frequency of transmitter 51.2 MHz @ 100 W		Frequency of transmitter 144.5 MHz @ 100 W	
	Field strength parallel to antenna	Field strength orthogonal to antenna	Field strength parallel to antenna	Field strength orthogonal to antenna	Field strength parallel to antenna	Field strength orthogonal to antenna	Field strength parallel to antenna	Field strength orthogonal to antenna	Field strength parallel to antenna	Field strength orthogonal to antenna
1	18 V/M	55 V/M	2 V/M	200 V/M	8 V/M	80 V/M	15 V/M	170 V/M	0 V/M	2 V/M
2	11 V/M	17 V/M	11 V/M	26 V/M	2 V/M	16 V/M	35 V/M	99 V/M	17 V/M	19 V/M
3	16 V/M	50 V/M	25 V/M	20 V/M	13 V/M	60 V/M	21 V/M	125 V/M	0 V/M	13 V/M
4	13 V/M	17 V/M	17 V/M	14 V/M	11 V/M	21 V/M	40 V/M	35 V/M	2 V/M	30 V/M
5	14 V/M	15 V/M	15 V/M	14 V/M	12 V/M	12 V/M	38 V/M	30 V/M	12 V/M	5 V/M
6	31 V/M	28 V/M	26 V/M	30 V/M	55 V/M	27 V/M	30 V/M	80 V/M	5 V/M	13 V/M
7	70 V/M	280 V/M	30 V/M	290 V/M	11 V/M	52 V/M	60 V/M	280 V/M	2 V/M	28 V/M
8	48 V/M	22 V/M	92 V/M	70 V/M	100 V/M	55 V/M	75 V/M	40 V/M	20 V/M	10 V/M
9	2 V/M	25 V/M	43 V/M	32 V/M	42 V/M	45 V/M	90 V/M	25 V/M	17 V/M	26 V/M
10	210 V/M	40 V/M	210 V/M	45 V/M	270 V/M	48 V/M	210 V/M	65 V/M	30 V/M	5 V/M
11	230 V/M	30 V/M	240 V/M	48 V/M	220 V/M	52 V/M	210 V/M	30 V/M	35 V/M	2 V/M
12	170 V/M	30 V/M	205 V/M	65 V/M	180 V/M	35 V/M	230 V/M	35 V/M	18 V/M	5 V/M
13	5 V/M	2 V/M	10 V/M	5 V/M	14 V/M	10 V/M	28 V/M	13 V/M	17 V/M	5 V/M
14	0 V/M	0 V/M	11 V/M	2 V/M	14 V/M	8 V/M	30 V/M	10 V/M	28 V/M	10 V/M
15	0 V/M	0 V/M	10 V/M	3 V/M	10 V/M	8 V/M	30 V/M	15 V/M	17 V/M	10 V/M

Antenna location on vehicle: center of rear deck lid

Meter location	Frequency of transmitter 25.04 MHz @ 100 W		Frequency of transmitter 35.04 MHz @ 100 W		Frequency of transmitter 39.04 MHz @ 100 W		Frequency of transmitter 51.2 MHz @ 100 W		Frequency of transmitter 144.5 MHz @ 100 W	
	Field strength parallel to antenna	Field strength orthogonal to antenna	Field strength parallel to antenna	Field strength orthogonal to antenna	Field strength parallel to antenna	Field strength orthogonal to antenna	Field strength parallel to antenna	Field strength orthogonal to antenna	Field strength parallel to antenna	Field strength orthogonal to antenna
1	2 V/M	31 V/M	0 V/M	45 V/M	15 V/M	100 V/M	10 V/M	180 V/M	0 V/M	2 V/M
2	2 V/M	5 V/M	24 V/M	40 V/M	30 V/M	75 V/M	45 V/M	55 V/M	0 V/M	13 V/M
3	5 V/M	45 V/M	22 V/M	110 V/M	14 V/M	150 V/M	20 V/M	280 V/M	2 V/M	18 V/M
4	2 V/M	5 V/M	43 V/M	40 V/M	10 V/M	24 V/M	30 V/M	15 V/M	5 V/M	30 V/M
5	2 V/M	0 V/M	30 V/M	30 V/M	5 V/M	16 V/M	50 V/M	30 V/M	2 V/M	2 V/M
6	20 V/M	30 V/M	5 V/M	1 V/M	100 V/M	78 V/M	10 V/M	12 V/M	1 V/M	1 V/M
7	21 V/M	200 V/M	55 V/M	300 V/M	150 V/M	>300 V/M	28 V/M	>300 V/M	5 V/M	35 V/M
8	22 V/M	11 V/M	0 V/M	11 V/M	50 V/M	18 V/M	58 V/M	27 V/M	2 V/M	11 V/M
9	14 V/M	68 V/M	22 V/M	2 V/M	92 V/M	52 V/M	68 V/M	52 V/M	2 V/M	10 V/M
10	100 V/M	21 V/M	5 V/M	13 V/M	150 V/M	20 V/M	150 V/M	45 V/M	40 V/M	13 V/M
11	110 V/M	18 V/M	5 V/M	18 V/M	180 V/M	27 V/M	130 V/M	30 V/M	38 V/M	8 V/M
12	140 V/M	24 V/M	10 V/M	16 V/M	175 V/M	26 V/M	160 V/M	30 V/M	28 V/M	10 V/M
13	12 V/M	5 V/M	27 V/M	2 V/M	23 V/M	5 V/M	35 V/M	11 V/M	45 V/M	9 V/M
14	23 V/M	8 V/M	40 V/M	3 V/M	40 V/M	5 V/M	45 V/M	12 V/M	60 V/M	20 V/M
15	10 V/M	5 V/M	24 V/M	0 V/M	25 V/M	5 V/M	25 V/M	18 V/M	30 V/M	28 V/M

f. Lower left side of dash panel

g. Passenger head space

3. Locations of electric field strengths less than 50 V/m
   a. Left side of package tray
   b. Right side of package tray

The author acknowledges the editing assistance of Sandra Muccioli.

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ABOUT THE AUTHOR

James P. Muccioli has extensive experience in EMC design, analysis, and testing. His background includes 13 years of specialized EMC systems experience at Chrysler Corporation and United Technologies. He served on the faculty of Lawrence Technological University, teaching an undergraduate course on noise reduction techniques and a continuing education seminar on electronic system noise reduction. He teaches EMC seminars through his own consulting firm JASTECH and has authored several symposium papers on EMC and is a NARTE Certified EMC Engineer. He is an active member of SAE-J1113 and J-551 EMC committees (1984–present) and is chairperson of the SAE Integrated Circuit EMC Task Force (1991–present). He is an IEEE-Electromagnetic Compatibility Society Board of Directors member.

CHAPTER 28
ELECTROMAGNETIC COMPATIBILITY

James P. Muccioli
EMC Consultant, JASTECH

28.1 NOISE PROPAGATION MODES

28.1.1 Introduction

Before an engineer can design for EMC, he must first understand the paths where electromagnetic interference can affect electronic modules and how electromagnetic emissions from his module will affect other electronic modules. Noise propagation can be defined as conducted mode propagation and/or radiated emissions propagation.

28.1.2 Conducted Mode Propagation

Conducted mode propagation occurs when electromagnetic interference travels on the wiring harness connecting the noise source to the device affected, as shown in Fig. 28.1.

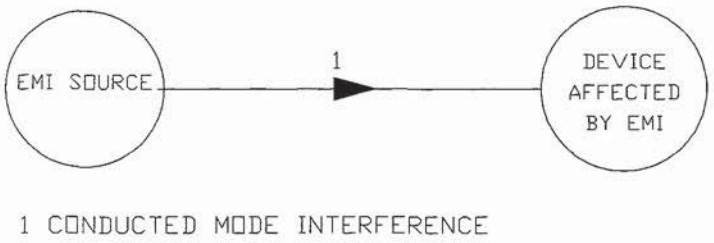


FIGURE 28.1 Conducted mode propagation.

28.1.3 Radiated Emissions Propagation

Radiated emissions propagation occurs when the electromagnetic interference travels through free space (air) from a noise source to the device affected, as shown in Fig. 28.2.

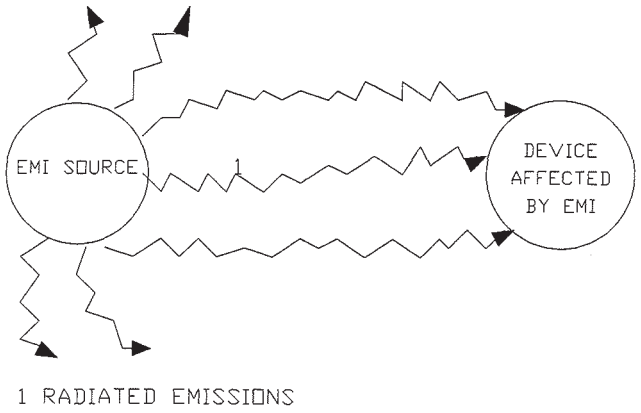


FIGURE 28.2 Radiated emissions propagation.

28.1.4 Conducted and Radiated Propagation

Conducted and radiated propagation occurs when the electromagnetic interference travels on and radiates from the wiring harness connecting the noise source to the device affected, as shown in Fig. 28.3.

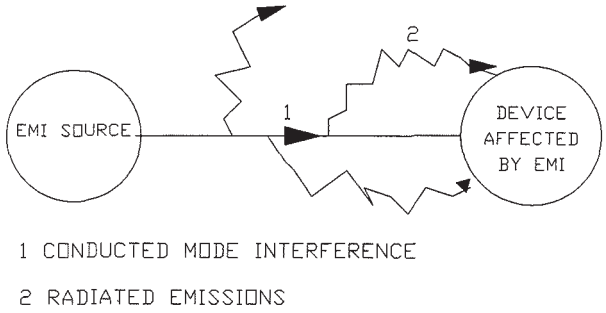


FIGURE 28.3 Conducted and radiated propagation.

28.1.5 Radiated and Conducted Propagation

Radiated and conducted propagation occurs when the electromagnetic interference travels through free space (air) from a noise source to the wiring harness of the device affected, as shown in Figure 28.4.

28.2 CABLING

28.2.1 Introduction

The use of wiring harnesses (transmission lines) in the presence of electromagnetic fields can cause unwanted noise energy to be induced onto signal-carrying conductors. Typical wiring

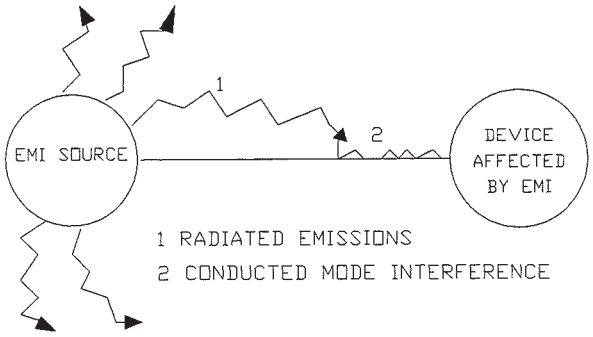


FIGURE 28.4 Radiated and conducted propagation.

harnesses in today's automobiles are made up of single, twisted pair, and coaxial type conductors. One of the biggest problems associated with using twisted pair and coaxial cables is an inappropriate method of termination. A test was performed to determine how termination affects them, and how they reject radiated interference.

28.2.2 Test Methodology

Using a stripline antenna, an E-field intensity of 50 V/m was maintained throughout the entire frequency range of the test. Figure 28.5 shows the test setup of the stripline antenna with relation to the cable under test and the ground plane. All cables used were 2 m in length and terminated with the same resistances. The cables were swept through a frequency range of 10 KHz to 100 MHz. Data points were selected at multiple decades of frequency.

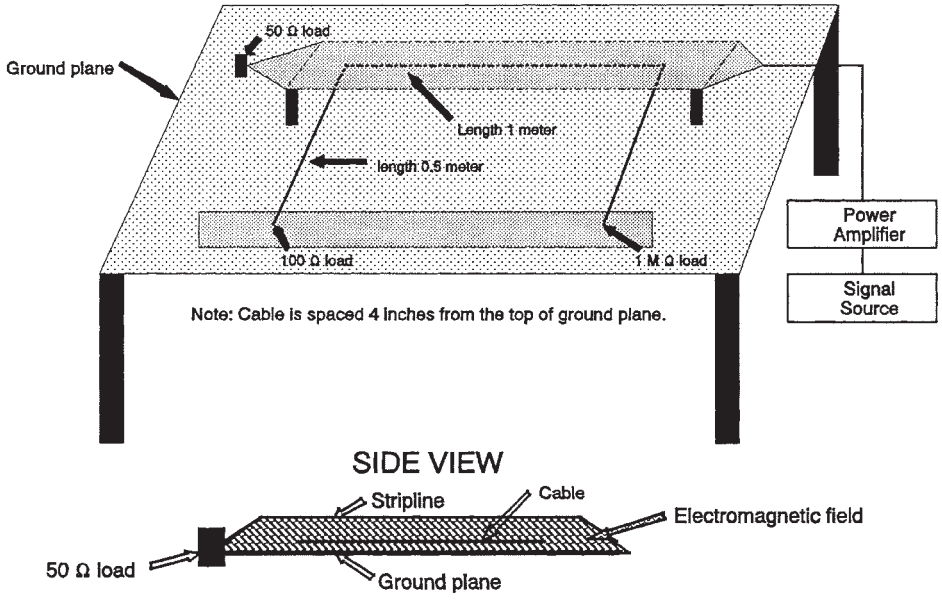


FIGURE 28.5 Stripline test setup.

28.2.3 Summary

Figure 28.6 shows the various cable configurations. Configurations A through F have both ends grounded, while configurations G through K have only one end grounded. The attenuation values for each cable configuration are shown in Table 28.1. Overall, cables with single-ended grounding offered more attenuation than cables with dual-ended grounding. This data should be used to get a feel for the different types of cable configurations. When the cable termination and load resistors are known, a test should be performed to verify the attenuation expected

TABLE 28.1 Attenuation in dB of Cable Configurations

Letter	10 kHz	50 kHz	100 kHz	1 MHz	10 MHz	100 MHz
A	0	0	0	0	0	0
B	0	0	0	0	0	–20
C	15	25	30	40	38	10
D	11	15	15	17	15	–10
E	8	8	7	13	10	20
F	8	12	15	27	28	20
G	40	44	46	56	38	51
H	20	15	15	15	10	–10
I	26	36	41	46	30	0
J	15	30	30	35	32	18
K	15	35	42	45	30	0

28.3 COMPONENTS

28.3.1 Capacitor

Capacitor Model. A high-frequency capacitor model is needed for analyzing the effects due to electromagnetic compatibility. Figure 28.7 shows one way to model a high-frequency capacitor.

Capacitor EMC Guidelines. Consider the frequency range, voltage rating, stability, temperature coefficient, and tolerance when choosing the dielectric type for the capacitance. The type of dielectric used in the capacitor will dictate the frequency range over which the capacitor will be most effective for filtering. Table 28.2 includes the relative losses (leakage) of dielectric types.

TABLE 28.2 Relative Losses of Dielectric Types

Dielectric type	Frequency range	Relative losses
Aluminum electrolytic	1 Hz–10 KHz	High
Tantalum electrolytic	1 Hz–10 KHz	High
Paper/mylar	100 Hz–5 MHz	Medium
High K-ceramic	1 KHz–100 MHz	Low
Plastic films	1 KHz–9 GHz	Low
Mica/glass/low-loss ceramic	5 KHz–10 GHz	Low

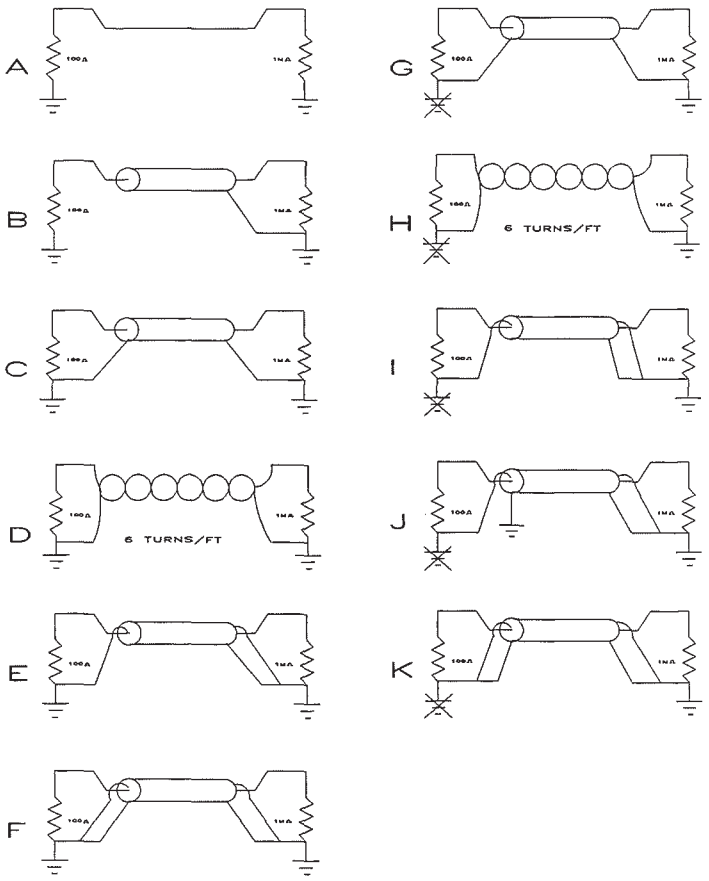
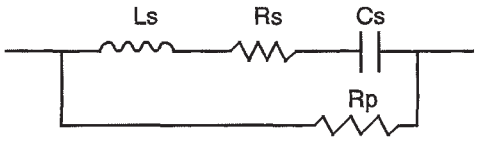


FIGURE 28.6 Cable configurations.



Cs = Series capacitance

Ls = Inductance due to lead length and capacitor structure

Rs = Effective series resistance and dissipation factor

Rp = Parallel leakage and volume resistivity of dielectric

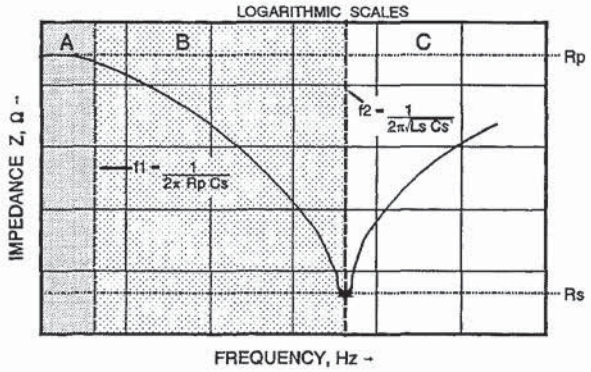
FIGURE 28.7 Equivalent circuit for a capacitor.

Capacitor Quality Q Factor. Quality factor Q of a capacitor is the ratio of the resonant frequency to the bandwidth between the frequencies on opposite sides of the resonance. The Q of a simple resonant circuit composed of a capacitance and inductances is given by the following equation:

$$Q = \frac{(Q_C \times Q_L)}{(Q_C + Q_L)}$$

where Q_C = the magnitude of the ratio of the capacitor susceptance to its effective shunt conductance at a specified frequency, and Q_L = the magnitude of the ratio of the inductor reactance to its effective series resistance at a specified frequency.

When Q is greater than 1, the capacitor impedance-versus-frequency model is as shown in Fig. 28.8. When Q is less than 1, the capacitor impedance-versus-frequency model is as shown in Fig. 28.9.



REGION

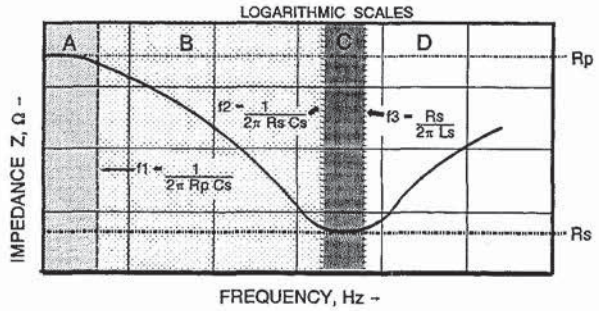
A Capacitor impedance is primarily determined by parallel leakage and volume resistivity of the dielectric (Rp).

B Capacitance (Cs) becomes the dominant with the impedance decreasing at -6 dB/octave.

★ Series resonance develops between Cs and Ls.

C Series inductance (Ls) becomes dominant.

FIGURE 28.8 Capacitor impedance versus frequency when $Q > 1$.



REGION

A Capacitor impedance is primarily determined by parallel leakage and volume resistivity of the dielectric (Rp).

B Capacitance (Cs) becomes the dominant with the impedance decreasing at -6 dB/octave.

C Series resistance (Rs) causes the relatively flat characteristic between f2 and f3.

D Series inductance (Ls) becomes dominant.

FIGURE 28.9 Capacitor impedance versus frequency when $Q < 1$.

The capacitor will self-resonate at some frequency dependent mainly upon the capacitive and inductive values of the capacitor itself, as shown in Figs. 28.8 and 28.9. Lead length is mainly responsible for the inductive element as depicted in the models. Excess length can reduce the resonant frequency significantly, hence reducing the operating frequency range.

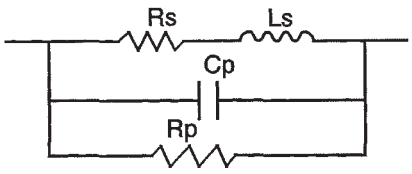
Using a network analyzer, data in Table 28.3 was gathered on ceramic capacitors. The lower the value of the capacitor, the greater the effect the lead length will have on the self-resonate frequency.

TABLE 28.3 Capacitors Measured at Self-Resonate Frequencies

Capacitance	Self-resonate frequency at ¼″ leads	Self-resonate frequency at ½″ leads
1000 pF	35 MHz	32 MHz
500 pF	70 MHz	65 MHz
100 pF	150 MHz	120 MHz
50 pF	220 MHz	200 MHz
10 pF	500 MHz	350 MHz

28.3.2 Inductor

Inductor Model. A high-frequency inductor model is needed for analyzing the effects due to electromagnetic compatibility. Figure 28.10 shows one way to model a high-frequency inductor.



Ls = Series inductance

Rs = Series resistance from wire used in winding

Cp = Distributed capacitance between the windings

Rp = Core and winding resistance losses (including skin effect) at the resonant frequency

FIGURE 28.10 Equivalent circuit for an inductor.

Inductor EMC Guidelines. EMC considerations for inductors include magnetic losses, mechanical stability, temperature coefficients, flux leakage, and dielectric losses. The shape of an inductor will determine some of its properties. An open core inductor, such as a cylinder, will have a large external magnetic field. A closed core inductor will confine most of the magnetic field. The toroid-shaped inductor has the maximum inductance per unit volume and low flux leakage. This is due to the fact that the toroid provides a closed circular path for magnetic flux, hence the external flux levels are very low. Figure 28.11 shows air core versus magnetic core inductors.

Inductor Quality Q Factor. Quality factor Q of an inductor is the ratio of the resonant frequency to the bandwidth between the frequencies on opposite sides of the resonance. The Q of a simple resonant circuit composed of a capacitance and inductances is given by the following equation:

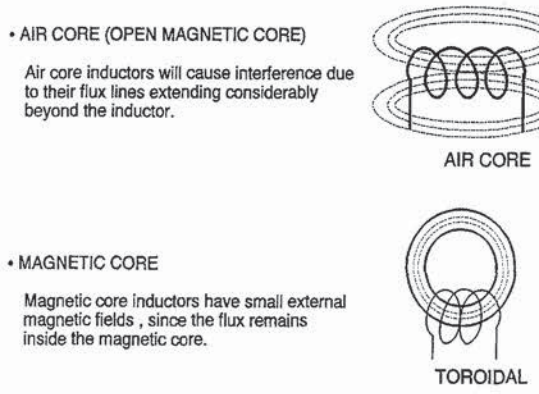
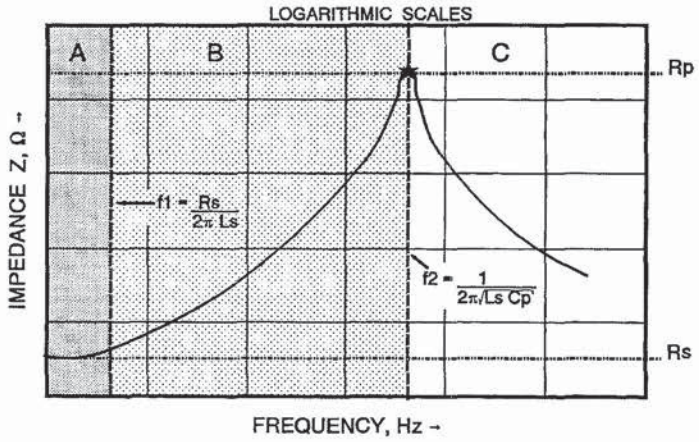


FIGURE 28.11 Air core versus magnetic core inductors.

$$Q = \frac{(Q_L \times Q_C)}{(Q_L + Q_C)}$$

where Q_L = the magnitude of the ratio of the inductor reactance to its effective series resistance at a specified frequency
Q_C = the magnitude of the ratio of the capacitor susceptance to its effective shunt conductance at a specified frequency

Figure 28.12 shows the inductor impedance versus frequency. An inductor has capacitance between each turn of the windings and leads. At some frequency, the inductor will become self-resonant, as shown in Fig. 28.12, due to its winding capacitance.



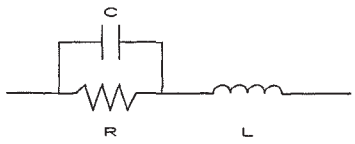
REGION

A	Inductor impedance is primarily determined by the winding dc resistance (Rs).
B	Inductance (Ls) becomes the dominant with the impedance increasing at +6 dB/octave.
★	Parallel resonance develops between Ls and Cp.
C	Parallel capacitance (Cp) becomes dominant.

FIGURE 28.12 Inductor impedance versus frequency.

28.3.3 Resistor

Resistor Model. A high-frequency resistor model is needed for analyzing the effects due to electromagnetic compatibility. In Fig. 28.13, one way to model a high-frequency resistor is shown.



C = SHUNT CAPACITANCE WHICH IS TYPICALLY 0.1 – 0.5pF

L = LEAD INDUCTANCE, EXCEPT FOR WIREWOUND RESISTORS

FIGURE 28.13 Equivalent circuit for a resistor.

Resistor EMC Guidelines. Consider the construction of the resistor before determining the transient handling capability and frequency characteristics. The resistor construction types are defined as carbon composition, chip (surface mount and leaded), film (thin and thick), and wirewound.

Transient Dissipation. Carbon composition resistors are capable of handling large transients without degradation to the resistor value. Chip-type resistors are capable of handling moderate (less than 40 V) transients, making them suitable for most printed circuit board applications. Film-type resistors should be *avoided* for lines which encounter transients of significant power, since the film degrades after many transients and the resistor value will become lower. Wirewound resistors can dissipate repetitive, high-power, and high-peak transients without failure. The larger the diameter of the wire windings, the more effectively the transient can be dissipated

Resistor Noise. In general, composition-type resistors produce the most electrical noise and wirewound resistors produce the least. Electrical noise in resistors manifests due to the thermal properties present in their construction. If a high-power and a low-power composition-type resistor are put in identical circuit conditions, the higher power resistor will produce less electrical noise. Because the noise produced by film-type resistors is less than that of composition types, they are used in small-signal or high-gain applications.

28.4 PRINTED CIRCUIT BOARD EMC CHECKLIST

1. Reduce radiated emissions and susceptibility by selecting the slowest possible switching speed (bandwidth) for the electronic devices.
2. Partition the PC-board.
   - **a.** Bypass ground plane at I/O connector.
   - **b.** Group regulators/power supplies near I/O connector.
   - **c.** Place crystals/RC clock circuit directly next to ICs.
   - **d.** Group same family of electronic devices together (interface, analog, low/medium/high-speed logic circuitry).

3. Single point the different types of ground circuits to I/O ground.
4. Bypass all lines at I/O connector.
   a. Reduce RF entering the PC-board by filtering at entrance.
   b. Reduce RF leaving the PC-board by filtering at exit.
5. Lay out the power distribution system.
   a. Low impedance power distribution system limits EMI.
   b. Power feed and return lines *must* be as close as possible to minimize impedance and loop sizes.
6. Decouple active components and power supply lines.
   a. Minimize instantaneous current draw on the power bus by placing a capacitor from the IC power to the IC ground.
   b. Calculate the size of capacitor required.
   c. Bulk decoupling capacitor (electrolytic typical 10–100 μF) is required at power entrance point.
7. Ground all unused IC input pins where possible.
   a. Reduce IC noise by lowering the ground impedance and eliminate unused IC pins from acting like antennas.
8. Design reverse voltage protection where needed.
   a. Diodes can be used to protect against reverse voltage damage.
9. Design clock line routing.
   a. Minimize clock line loop size.
   b. Clock line return path must be next to clock line.
10. Design PC-board jumper cables to minimize loop area by having return paths for all types of signal and power lines.
11. Autoroute the PC-board one partition group at a time with signal lines last.
12. Design metal housings to act as shields.

28.5 INTEGRATED CIRCUIT DECOUPLING—A KEY AUTOMOTIVE EMI CONCERN

Note: Parts of this section were taken from the paper of the same name presented by James P. Muccioli at the EMC/ESD International Conference in April 1992.

28.5.1 Abstract

Since the development of the first solid state engine control for automobiles, microcircuit technology has evolved with greater complexity, faster clock speeds, and smaller package size. Electromagnetic compatibility (EMC) has become a high priority in the design of electronic automotive modules. At the same time, the die size of CMOS technology has decreased from 9-micron process size (50-ns rise/fall time) to 0.8-micron process size (1.5-ns rise/fall time) in high-speed CMOS integrated circuits. To minimize the effect of EMC due to the faster rise/fall time, the design engineer must analyze the integrated circuit (IC) package and associated decoupling capacitor. This section will concentrate on how to analyze the decoupling capacitor requirements.

28.5.2 Introduction

Automotive electromagnetic emissions requirements and extreme cost constraints require the design engineer to be very innovative in addressing his EMI concerns. All components on the printed circuit board must be analyzed for effects and emissions contributed to the total radiated emissions from the electronic module. One source of noise on the printed circuit board is the integrated circuit. Choosing the right decoupling capacitor will limit the amount of electromagnetic emissions radiated from the integrated circuits on the printed circuit board. The decoupling capacitor, if not properly chosen for each integrated circuit, will contaminate the input/output lines in the form of ringing, overshooting, and/or undershooting.

28.5.3 Decoupling Capacitor Value

The decoupling capacitor supplies the instantaneous power required to the integrated circuit when switching from one of its transition states to another. When calculating the value for the decoupling capacitor, the following items must be considered:

1. Transient current of integrated circuit
2. Switching time of transition state
3. Allowable transient voltage drop in the supply voltage
4. Decoupling capacitor inductance due to lead length and capacitor structure
5. Printed circuit board trace inductance

Before the decoupling capacitor value can be determined, the design engineer must measure the rise/fall times of the various types of integrated circuits used on the printed circuit board. If the printed circuit board is using dual-source integrated circuits for production, the second source integrated circuits must also be measured and taken into account. After gathering this data, the switching frequency generated by the integrated circuit rise/fall time can be calculated by the formula:

$$f = \left[\frac{1}{\pi} \times t_r\right] \text{Hz} \tag{28.1}$$

where t_r = rise time/fall time in seconds

The value of the decoupling capacitor must satisfy two requirements:

1. The value of the decoupling capacitor must equal or exceed the minimum decoupling capacitor value required to supply enough power to meet the allowable transient voltage drop on the supply voltage.
2. The decoupling capacitor at this value must avoid self-resonance when instantaneous power is required for the integrated circuit.

The minimum value of the decoupling capacitor referred to in the first requirement (preceding) can be calculated by the formula:

$$C = \frac{(dI \times dt)}{dV} \tag{28.2}$$

where dI = current of transient (amps)
dt = switching time of transient (seconds)
dV = the transient voltage drop in the supply voltage (volts)

The self-resonant circuit referred to in the second requirement (see Fig. 28.14) is the combination of the capacitance and inductance between the decoupling capacitor and integrated circuit, resonating at the switching frequency generated by the integrated circuit. The inductance in the self-resonant circuit is the combination of inductances of the capacitor (L_C), the printed circuit board trace (L_{PCB}), and the integrated circuit lead frame (L_{IC}). The capacitance used for calculating the self-resonant circuit is the value of the capacitor C only (the capacitance value for the printed circuit board trace and the integrated circuit lead frame can be neglected because their values are negligible when compared to the decoupling capacitor value). The frequency of the self-resonant circuit can be calculated by the following formula:

$$f_c = \frac{1}{2\pi\sqrt{(L_{PCB} + L_{IC} + L_C)(C)}} \text{Hz} \tag{28.3}$$

where L_{PCB} = inductance of printed circuit board trace (henrys)
L_{IC} = inductance of integrated circuit lead frame (henrys)
L_C = inductance of capacitor (henrys)
C = capacitance value (farads)

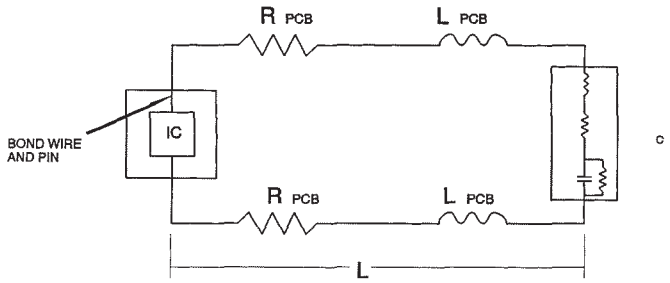


FIGURE 28.14 Self-resonant circuit.

If the second requirement is not met (the circuit becomes self-resonant), there will not be enough power to maintain the desired transient voltage drop.

When the design engineer analyzes the data from the three formulas and tries to meet the two requirements for a decoupling capacitor, the data will not always yield a solution.

The design engineer must also look at the decoupling capacitor placement (Fig. 28.15) and the various integrated circuit packages to determine if there are any differences in power and ground lead frame inductances.

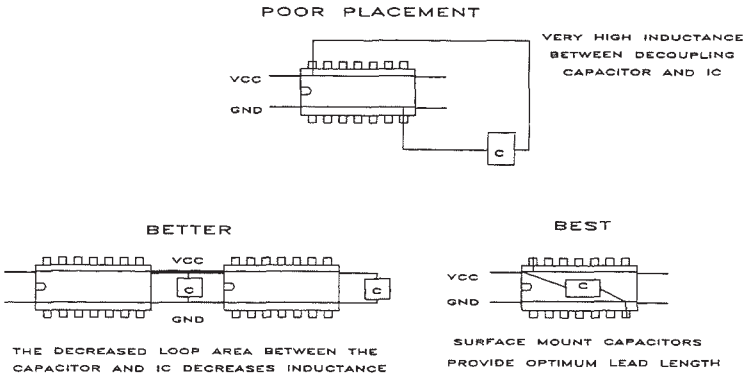


FIGURE 28.15 Decoupling capacitor placement.

The longest copper lead frame trace inductance values of various integrated circuits are not easily available. With the help of Mike Catherwood from Motorola, the following chart was created:

Package type	L_{max} (nH)
14 lead SOIC	1.81
16 lead SOIC	1.69
14 lead PDIP	3.93
16 lead PDIP	4.33
28 lead PDIP	8.72
20 lead PLCC	1.79
24 lead PLCC	2.45
44 lead PLCC	3.94
52 lead PLCC	4.06
68 lead PLCC	6.58
32 lead R-PLCC	1.89

This information is necessary for picking the lowest lead frame inductance for a specific IC package.

Sample Problem. Find the decoupling capacitor value for a 74HCO4 14 lead PDIP hex inverter when assuming the following:

1. Supply voltage drop = 250 mV
2. Current of transient = 50 mA
3. Switching time of transient = rise/fall time of IC = 10 ns

Note: The smaller value of t_{TLH} or t_{THL}, taken from the IC specification sheet, can be used for t_r

4. Printed circuit board trace = 5 nH/cm
5. Printed circuit board trace length = 2 cm
6. Capacitor inductance = 1 nH

Solution. The switching frequency generated by the IC rise/fall time can be calculated using Eq. (28.1):

$$\begin{aligned} f &= [1/\pi \times t_r]\ \text{Hz} \\ &= 1/[\pi \times (1.0 \times 10^{-8})]\ \text{Hz} \\ &= 31\ 830\ 989\ \text{Hz} \\ &= 31.8\ \text{MHz} \end{aligned}$$

The minimum value of the decoupling capacitor referred to in the first requirement can be calculated using Eq. (28.2):

$$\begin{aligned} C &= \frac{(dI \times dt)}{dV} \\ &= [(5.0 \times 10^{-2}\text{A}) \times (1.0 \times 10^{-8}\text{s})]/2.5 \times 10^{-1}\text{V} \\ &= 2.0 \times 10^{-9}\text{F} \\ &= 2000\ \text{pF} \end{aligned}$$

The frequency of the self-resonant circuit referred to in the second requirement can be calculated using Eq. (28.3):

$$f_c = \frac{1}{2\pi\,[(L_{PCB} + L_{IC} + L_C)(C)]^{1/2}}$$

$$= \frac{1}{2\pi\,[(2.0\text{ cm})(5.0\times10^{-9}\text{H/cm}) + (2)(3.93\times10^{-9}\text{H}) + (1.0\times10^{-9}\text{H})(2.0\times10^{-9}\text{F})]^{1/2}}$$

$$= 25{,}913{,}990\text{ Hz}$$

$$= 25.9\text{ MHz}$$

The second requirement is not met because the self-resonance of the capacitor combination (25.9 MHz) is lower in frequency than the integrated circuit switching frequency (31.8 MHz). If we change to a 14 lead SOIC package, the integrated circuit lead inductance is reduced to 1.81 nH per lead. Also, since the package is smaller, the printed circuit board trace length is reduced to 1 cm. The frequency of the self-resonant circuit is recalculated as shown:

$$f_c = \frac{1}{2\pi\sqrt{L_{PCB} + L_{IC} + L_C\,(C)}}$$

$$= \frac{1}{2\pi\sqrt{((1.0\text{ cm})(5.0\times10^{-9}\text{ H/cm}) + (2)(1.81\times10^{-9}\text{ H}) + (1.0\times10^{-9}\text{ H}))(2.0\times10^{-9}\text{ F})}}$$

$$= 36{,}284{,}204\text{ Hz}$$

$$= 36.3\text{ MHz}$$

Therefore, by changing the IC package from PDIP to SOIC, we can meet both requirements.

28.5.4 Summary and Discussion

Decoupling capacitor values calculated using the formulas in this paper will not be optimal for every application due to lead frame and printed circuit board trace inductances. Integrated circuit manufacturers need to continue their search for ways to minimize the inductances in the power and ground leads. They should investigate supplying integrated circuits with decoupling capacitors internal to lead frame packages. Until the integrated circuit manufacturers can help the design engineer, the following items should be considered before a decoupling capacitor is chosen:

1. The larger the decoupling capacitor value, the lower the self-resonant frequency.
2. Too small a decoupling capacitor will not have sufficient charge storage for transient current needed by the integrated circuit.
3. Different integrated circuit package configurations will change the integrated circuit lead frame inductance.

28.6 IC PROCESS SIZE AFFECTS EMC

Note: Parts of this section were taken from the article of the same name by James P. Muccioli published in the June 1993 issue of *EMC Test & Design* magazine.

28.6.1 Abstract

This section focuses on how to measure the near-field radiated emissions generated by an integrated circuit. Testing was performed in a controlled manner that yields repeatable results using a miniature skin current probe. Integrated circuits are characterized by process size and its effect on radiated emissions.

28.6.2 Test Configuration

The devices under test (DUT) are all the same eight-bit microprocessor type with internal test ROM code. The only variable is the process size, which changes from 1.95 micron to 1.50 micron.

The DUT is in a standardized manufacturer IC test setup (Fig. 28.16) which is part of a ground plane to assure test repeatability. The DUT is powered by a low-impedance battery (alkaline) to assure that there is no possibility for conducted noise to interfere with or confuse the test results. The software for the programmable integrated circuit flows in a continuous loop and is part of the internal ROM.

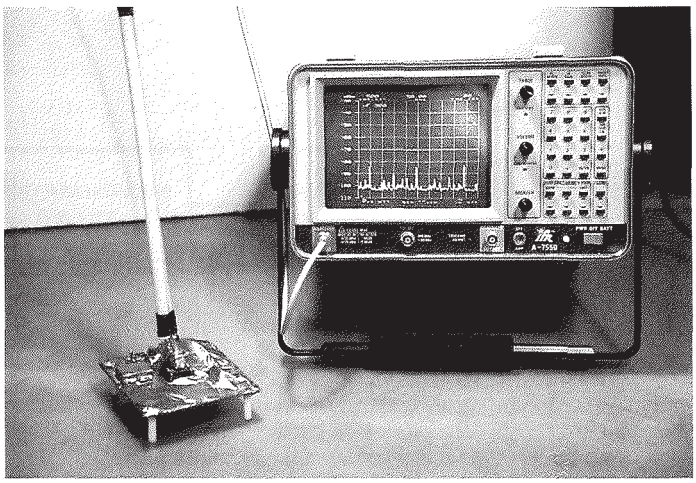


FIGURE 28.16 Picture of IC test setup with ground plane and skin current probe.

28.6.3 Test Methodology

The purpose for using a miniature skin current probe is to make quantitative measurements of currents (magnetic fields) generated by integrated circuits. The current probe can be used in a nonshielded room since only the magnetic fields related to the electromagnetic radiation potential of the integrated circuit affect the probe and it is relatively insensitive to stray electric fields.

The surface of the integrated circuit is mapped by orienting the probe for maximum sensitivity and then repeating the measurement after moving the probe to the next location. The skin current probe (Fischer Custom Communications, Inc. F-97) has a transfer impedance of 1 ohm ±20% from 70 MHz to greater than 1000 MHz as shown in Fig. 28.17.

The miniature skin current probe is in series with a 20-dB preamplifier (Mini-Circuits ZFL-1000LN) and is connected to a spectrum analyzer (IFR Systems, Inc. A-7550) as shown in Fig. 28.18. The system gain of the measuring equipment should be known with an accuracy

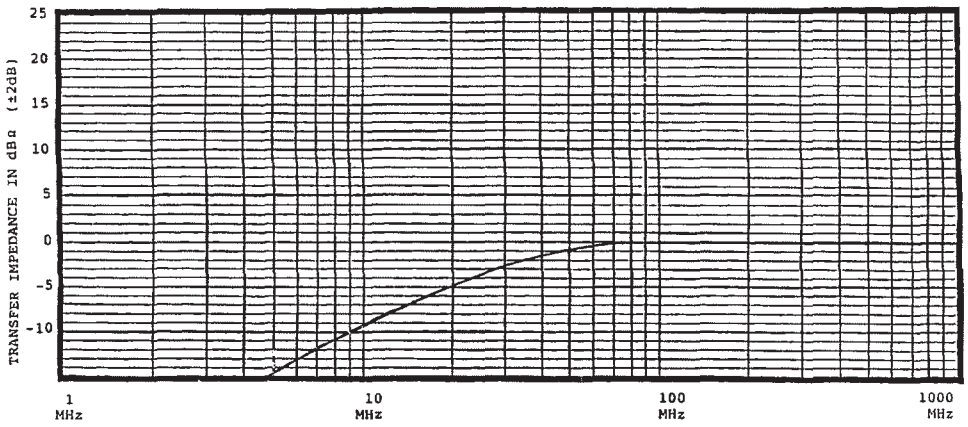


FIGURE 28.17 F-97 transfer impedance versus frequency. *(Courtesy of Fischer Custom Communications)*

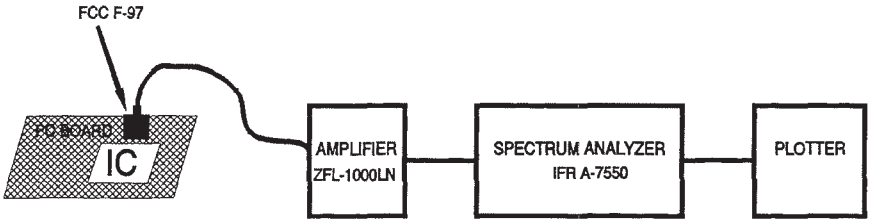


FIGURE 28.18 System test setup.

of ±0.5 dB. If the signals being measured by the skin current probe are within 6 dB of the system noise floor, then a smaller resolution bandwidth should be used on the spectrum analyzer.

The first measurement taken in each frequency band of the spectrum analyzer should be the ambient system level to assure that any ambient signals present are at least 6 dB below the signals of the integrated circuit. This is accomplished by taking the ambient measurement with the skin current probe placed on top of the integrated circuit in the measurement position with no power supply to the DUT. The DUT should be energized and a complete operational check of the integrated circuit test code performed to assure proper functioning of the device.

28.6.4 Test Results

Figures 28.19 and 28.20 show the system noise floor with the preamplifier and the F-97 probe. The frequency range of Fig. 28.19 is from 70 to 250 MHz with the center at 160 Mhz. The frequency range of Fig. 28.20 is from 250 to 500 MHz with the center at 375 MHz. The system noise floor from 70 to 500 MHz is below –120 dBm when the 20-dB gain is factored into the spectrum analyzer plot.

Figures 28.21 and 28.22 show the measured magnetic emissions of an eight-bit microprocessor with a 1.95-micron process size. The highest peak frequency from the microprocessor is at 72 MHz with a level corrected for preamp gain of –83.33 dBm.

Figures 28.23 and 28.24 show the measured magnetic emissions of an eight-bit microprocessor with a 1.50-micron process size. The highest peak frequency from the microprocessor is at 72 MHz with a corrected level of –86.00 dBm.

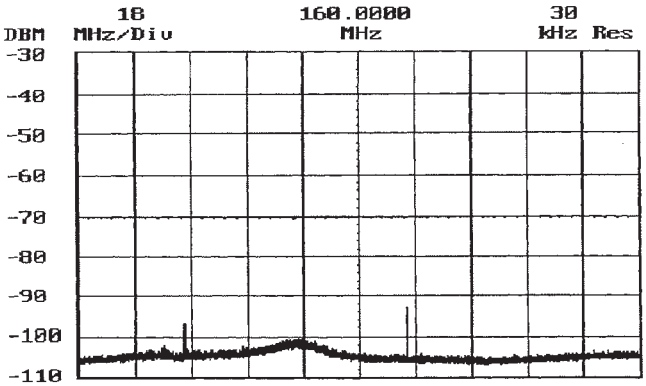


FIGURE 28.19 Ambient system level measurement from 70 to 250 MHz.

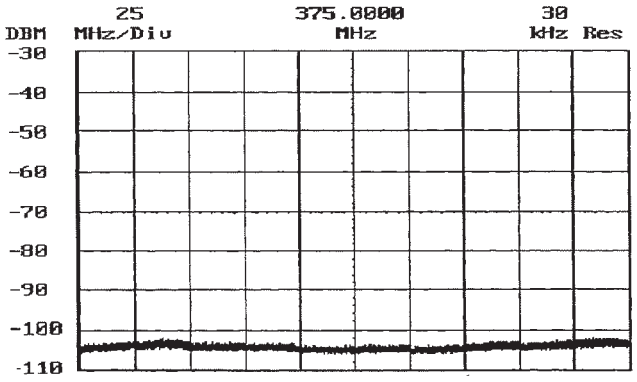


FIGURE 28.20 Ambient system level measurement from 250 to 500 MHz.

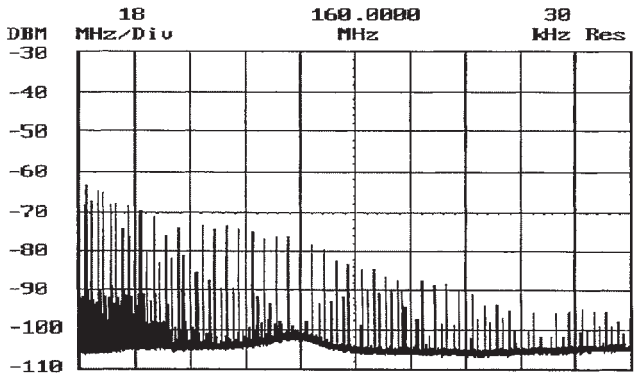


FIGURE 28.21 Magnetic emissions of 1.95-micron process from 70 to 250 MHz.

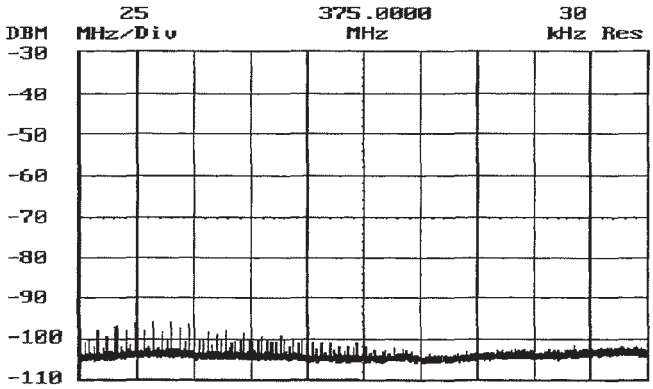


FIGURE 28.22 Magnetic emissions of 1.95-micron process from 250 to 500 MHz.

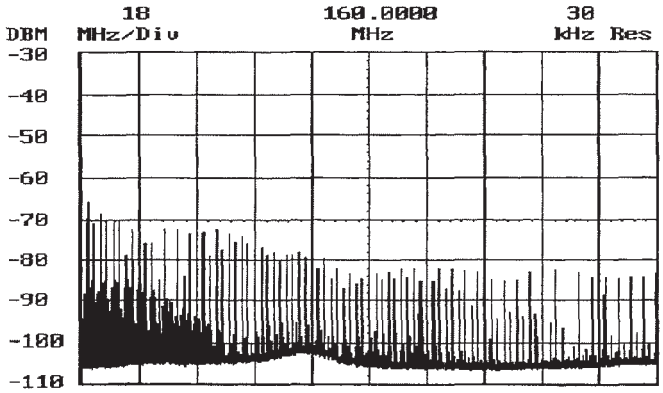


FIGURE 28.23 Magnetic emissions of 1.5-micron process from 70 to 250 MHz.

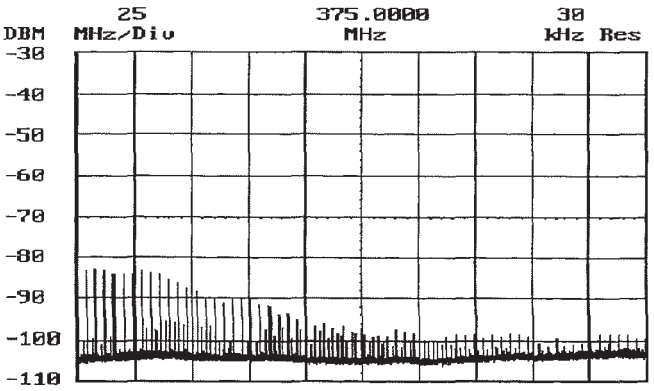


FIGURE 28.24 Magnetic emissions of 1.5-micron process from 250 to 500 MHz.

28.6.5 Summary and Discussion

When analyzing the data from Figs. 28.21, 28.22, 28.23, and 28.24, the following statements can be made:

1. The 1.95-micron process size magnetic emissions drop off faster than the 1.50-micron process size.
2. The 1.50-micron data has a more intense magnetic field between 70 and 115 MHz than the 1.95-micron data.
3. The amplitude of the 1.95-micron data is typically 10 to 15 dBm less than the 1.50-micron data after 200 MHz.

From the data analyzed, the author demonstrated that integrated circuit process size changes do have an effect on electromagnetic compatibility. The rise time of the integrated circuit is also affected by the process size change. The 1.95-micron process size has a rise time of 6.4 ns and the 1.50-micron process size has a rise time of 2.4 ns. Until the integrated circuit manufacturers can supply typical emission-level data with integrated circuit process size changes, the design engineer must make quantitative measurements of magnetic emissions from the integrated circuit.

The author acknowledges the editing assistance of Sandra Muccioli.

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ABOUT THE AUTHOR

For information about the author, please refer to page 27.18.

P · A · R · T · 7

EMERGING TECHNOLOGIES

CHAPTER 29
NAVIGATION AIDS AND INTELLIGENT VEHICLE-HIGHWAY SYSTEMS*

Robert L. French
R. L. French & Associates

Autonomous navigation and route guidance systems with static databases are of considerable utility on a stand-alone basis. However, future versions will be linked to traffic management centers (TMC) by mobile data communications for maximum effectiveness. Automobile navigation technologies coupled with data communications also provide a basis for vehicle tracking and fleet management. These in-vehicle systems are viewed as a major subset of intelligent vehicle-highway systems (IVHS), a rapidly expanding worldwide movement to improve the efficiency, safety, and environmental aspects of road traffic through the application of information, communications, positioning, and control technologies.

29.1 BACKGROUND

Sophisticated vehicular navigation system concepts have become widely known only during the last decade. However, the historical roots of automobile navigation go much deeper.[1] The first vehicular navigation system was the "south-pointing chariot," a mechanical direction-keeping system developed by the Chinese around 200 to 300 A.D., almost 1000 years before the magnetic compass was invented. Its operation was based on the differential odometer phenomenon that, as a vehicle changes heading, the outer wheels travel further than the inner wheels by a distance that is a mathematical function of the change in heading.

Mechanical route guides for automobiles were introduced in the United States around 1910 to aid the drivers of early automobiles before roads were uniformly marked. These early devices incorporated the information of route maps in various forms including sequential instructions printed on a turntable, punched in a rotating disk, and printed on a moving tape, all driven by an odometer shaft in synchronization with distance traveled along the route.

For example, the 1910 Chadwick Road Guide rotated a metal disk in synchronization with distance traveled. The disk had holes spaced to coincide with decision points along the route

* As this book is going to press, the name "Intelligent Vehicle-Highway Systems" is being changed to "Intelligent Transportation Systems (ITS) in the United States.

represented by the disk. An array of spring-loaded pins behind the slowly rotating disk was normally depressed, but when a punched hole traversed a pin, the pin released and raised a signal arm bearing a color-coded symbol indicating the action to be taken. In addition, a bell was sounded to draw the driver's attention to the signal.

The early mechanical route guidance systems faded out of the picture as roadside signs were standardized and became more plentiful by the 1920s. A resurgence of interest in route guidance occurred in the 1960s when ERGS (Electronic Route Guidance System) was researched by the U.S. Bureau of Public Roads.[2] Although ERGS was soon grounded from lack of Congressional support, it was followed in the 1970s by CACS (Comprehensive Automobile Control System) in Japan and by Autofahrer Leit-und Information System (ALI) in Germany.

Like ERGS, the CACS and ALI used real-time traffic information to compute best routes for downloading to on-board display equipment at strategically located proximity beacons. Thus, these early research and test projects, along with the evolution during the same era of advanced traffic management concepts for computerized control of area-wide traffic signals based on a centralized traffic database, set the stage for the much broader IVHS movements that started shaping up in Europe, Japan, and the United States in the mid-1980s.

Although comprehensive IVHS products and services, including data communication links between the traffic infrastructure and navigation-equipped vehicles, are not yet available, sophisticated autonomous navigation systems have been on the market in Japan since being introduced as a factory option by Toyota in 1987.[3] Approximately 500,000 had been sold by 1994, the year that OEM navigation systems were finally introduced in the United States and Europe.

29.2 AUTOMOBILE NAVIGATION TECHNOLOGIES

Positioning technologies are fundamental requirements of both vehicle navigation systems and vehicle tracking systems. Almost all vehicular navigation systems include dead reckoning with map matching as the main positioning technology, but most state-of-the-art systems also include a GPS (Global Positioning System) receiver now that the GPS satellite constellation is fully operational.

Map matching as well as route guidance must be supported by digital road maps. Another important supporting technology is mobile data communications for traffic and other traveler information. Although vehicle tracking systems may not require digital road maps aboard the vehicle (as is generally the case for navigation systems), they do require a mobile data communications link between the vehicle and dispatch office unless they use infrastructure-based integrated positioning and communications technologies. However, GPS and other radiopositioning technologies (e.g., Loran-C) are often used in conjunction with separate mobile communication systems for vehicle tracking.

29.2.1 Radiopositioning

Radiopositioning is the processing of special signals from one or more radio transmitters at known locations to determine the position of the receiving equipment. Although a number of radiopositioning technologies are potentially applicable, satellite-based GPS is by far the most popular.

GPS, which is operated by the U.S. Department of Defense, includes 24 satellites spaced in orbits such that a receiver can determine its position by simultaneously analyzing the travel time of signals from at least four satellites. GPS has the advantage of giving absolute position (albeit with an uncertainty of up to 100 m for civil receivers unless corrected by differential GPS). However, GPS alone is inadequate for automobile navigation because signal reception on roadways is sometimes blocked by buildings, foliage, etc. Nonetheless, GPS is very effective for automobile navigation when integrated with dead reckoning and map matching.

Proximity beacons provide another form of radiopositioning which is used in some vehicle navigation systems, particularly those that also use proximity beacons for communications purposes. Proximity beacons are devices installed at key intersections and other strategic roadside locations that communicate their location and/or other information to receivers in passing vehicles via very short-range radio, microwave, or infrared signals. The reception of a proximity beacon signal means that the receiving vehicle is within 50 m or so of the beacon, and provides an occasional basis for confirming vehicle position.

29.2.2 Dead Reckoning

Dead reckoning, the process of calculating location by integrating measured increments of distance and direction of travel relative to a known location, is used in virtually all vehicle navigation systems. Dead reckoning gives a vehicle's coordinates (X_n, Y_n) relative to earlier coordinates (X_o, Y_o):

$$X_n = X_o + \sum_1^n \Delta X_i = X_o + \sum_1^n \Delta l_i \sin \phi_i$$

$$Y_n = Y_o + \sum_1^n \Delta Y_i = Y_o + \sum_1^n \Delta l_i \cos \phi_i$$

where ϕ_i is the heading associated with l_i, the ith measured increment of travel as illustrated in Fig. 29.1. Dead reckoning for vehicle navigation thus requires sensors for measuring distance traveled and heading (or change in heading).

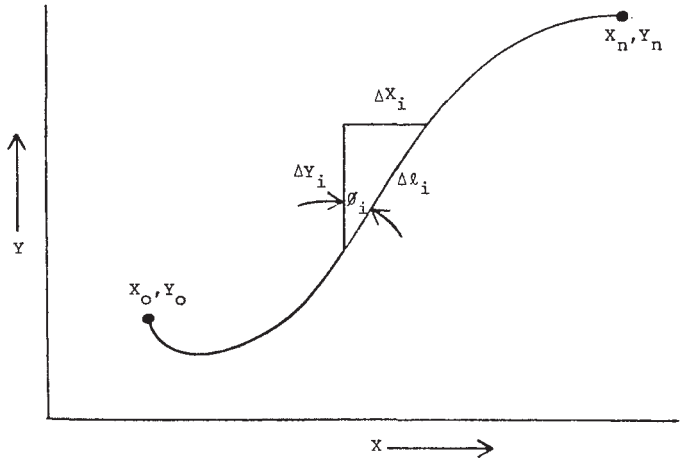

FIGURE 29.1 Dead-reckoning formulation.

Distance Sensors. Distance measurements for vehicle navigation systems are usually made with an electronic version of the odometer. Electronic odometers provide discrete signals from a rotating shaft or wheel, and a conversion factor is applied to obtain the incremental distance associated with each signal. Automobiles equipped with antilock braking systems (ABS) already have wheel sensors that may also serve as electronic odometers for navigation systems.

Odometers are subject to a number of error sources, some of which are systematic and may be corrected in the distance conversion process. The difference in the diameter of a new tire and a well-worn tire, for example, can contribute distance errors as high as 3 percent. The

error in distance measurements increases by approximately 0.1 to 0.7 percent when vehicle speed is increased by 40 km/h due to the effect of centrifugal force on the tires, and a 10 psi change in tire pressure can induce an error of 0.25 to 1.1 percent.

Heading Sensors. Vehicle heading may be measured directly with a magnetic compass, or indirectly by keeping track of heading relative to an initial heading by accumulating incremental changes in heading. A number of alternative means are available for measuring vehicle heading or heading changes. However, most have at least one drawback. As a result, it is a common practice to use two different types of sensors in combination to offset one another's weaknesses.

The magnetic compass's well-known accuracy problems due to anomalies in the earth's magnetic field are compounded when installed in a vehicle by induced fields which depend upon vehicle heading. Nonetheless, some form of magnetic compass is used in most vehicular navigation systems. Compact solid state flux-gate compasses with software processes for compensating errors resulting from both permanent and induced magnetism of the vehicle are popular in current systems.

In many applications, both a flux-gate compass and a differential odometer or a gyroscopic device are used along with a software filtering process that combines the outputs. Higher relative weight is placed on the differential odometer or gyro output for short-term changes in heading and on the compass output for longer-term trends in absolute heading.

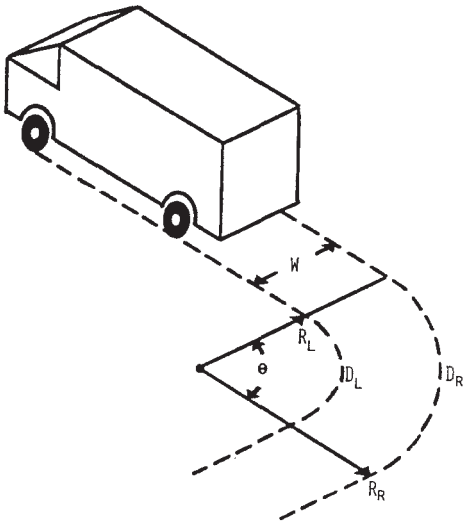

FIGURE 29.2 Differential odometer principle.

A differential odometer consists of a pair of odometers, one each for the wheels on opposite ends of an axle. When a vehicle changes heading by an amount Θ as illustrated in Fig. 29.2, the outer wheel travels farther than the inner wheel by ΔD, which may be expressed in terms of heading change and vehicle width:

$$\Delta D = D_R - D_L = \Theta(R_R - R_L) = \Theta W$$

Thus $\Theta = \Delta D/W$.

Several other types of heading-change sensors use some form of the gyroscopic principle. These range from traditional spinning devices and gas-jet sensors to vibrating bars and fiber optic gyros. Although more expensive than differential odometer sensors, they are much simpler to install. The fiber optic gyro started appearing in production automobile navigation systems in 1991. Finally, the more advanced forms of GPS receivers also support derivation of vehicle heading.

29.2.3 Digital Road Maps

Although a few route guidance systems use centrally located digital road map databases, the vast majority require an on-board database. The two basic approaches to digitizing maps are matrix encoding and vector encoding. A matrix-encoded map is essentially a digitized image in which each image element or pixel, as determined by an X-Y grid with arbitrary spacing, is defined by digital data-giving characteristics such as shade or color. In addition to requiring more data storage than vector encoding, matrix encoded maps are ill-suited for analytical treatment such as map matching or route finding.

The vector encoding approach applies mathematical modeling concepts to represent geometrical features such as roadways and boundaries in abstract form with a minimum of data.