Petitioner's Supplemental Reply in Support of Petition IPR2017-01430

DOCKET NO.: 2211726-00145
Filed on behalf of Unified Patents Inc.
By: David L. Cavanaugh, Reg. No. 36,476
Daniel V. Williams, Reg. No. 45,221
Matthew J. Leary, Reg. No. 58,593
Wilmer Cutler Pickering Hale and Dorr LLP 1875 Pennsylvania Ave., NW
Washington, DC 20006
Tel: (202) 663-6000
Email: david.cavanaugh@wilmerhale.com

Roshan Mansinghani, Reg. No. 62,429 Jonathan Stroud, Reg. No. 72,518 Unified Patents Inc. 1875 Connecticut Ave. NW, Floor 10 Washington, DC, 20009 Tel: (202) 805-8931 Email: roshan@unifiedpatents.com Email: jonathan@unifiedpatents.com

DOCKE

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNIFIED PATENTS INC. Petitioner

v.

PLECTRUM LLC Patent Owner

IPR2017-01430 Patent 5,978,951

PETITIONER'S SUPPLEMENTAL REPLY

TABLE OF CONTENTS

Page

I.	SUMMARY1	
II.	ROW-BASED SRAMS IN VIEW OF CHERITON ARE OBVIOUS	
	А.	Row-based SRAM memories were well-known, and are the only type of SRAMs described in the record
	В.	It would have been obvious for <i>Cheriton's</i> SRAMs to have rows3
III.	EACH ELEMENT OF THE NEW CLAIMS IS DISCLOSED AND/OR RENDERED OBVIOUS IN VIEW OF <i>CHERITON</i>	
	А.	Element $2(b)$ – "a cache comprised of plural rows, each having plural respective entries" and element $21(c)$ – "a cache having plural rows, each of said rows having plural entries"
	В.	Element $2(f)$ – "using said received, encoded address information to identify one of said cache rows", $21(h)$ – "usingsaid cache address to identify a cache entry"
	C.	Element $1(g)$ – "comparing said coded address to a value associated with a row"
	D.	Element 2(g), [(i)] – "retrieving first [second] address information from a [said] first entry of said identified row" and element 1(h) – "in the event of a matchwith said row, comparing said received destination address with a cached destination address associated with a first entry in said row"
TT 7	E.	Dependent claims 3-6, 12-14 and 22-24 are rendered obvious
IV.	CONCLUSION	

I. SUMMARY

Following the *SAS* decision, the Board instituted claims 1-6, 12-14, and 21-24 (the "New Claims"). Paper 16 at 2.

Addressing Claim 1, the Board preliminarily asserted that *Cheriton* lacked: 1) a "comparison of values associated with a row in a cache," and 2) the subsequent comparison of a value within that row. Paper 11 at 3. The first step uses, e.g., a hash value as an index/address to "identify" a cache row that potentially has routing data for a packet. *E.g.*, '951 patent (EX1001), Fig. 7B. Notably, Claims 2 and 21 simply require that a row is "identif[ied]" without requiring comparing values. The second step retrieves an entry from that identified row and compares it to the incoming packet's destination address to see if the row contains the hoped-for routing data. *Id.*, Claim 2, ll. 56-59.

These limitations comprise actions (identification and comparison) using particular data (values and destination addresses) stored in a specific structure (rows). The petition demonstrated that *Cheriton* explicitly taught the *actions* on the *particular data*, such as using a hash index to "identify" address data in an SRAM for element 2(f). Petition at 39-40. Hence, the Board's preliminary decision amounted to finding that *Cheriton* does not explicitly disclose that the acted-upon data was in a *row-based* structure. Paper 11 at 3.

But the petition and the as-filed record demonstrate that it would have been

obvious to use row-based SRAMs in *Cheriton* (addressed in Section II below). *E.g.*, Petition at 30-31. As a result, it would have been obvious for *Cheriton's* disclosed *actions* on its disclosed *data* to have been used in row-based SRAMs (the *structure* the record demonstrates was obvious) (addressed in Section III below). Seshan (EX1007) ¶¶ 62, 86-100, 105-106. This is why *Cheriton* renders the New Claims obvious.

For example, the Board does not appear to contest that *Cheriton* taught the action of retrieving and comparing destination addresses from multiple-entry elements in SRAM as per limitations 2(g) and 2(i). *See* Board Decision, Paper 8 at 14-15. If that SRAM was *row-based* (which the petition and the as-filed record demonstrate was obvious), the Petition showed that *Cheriton* rendered obvious retrieving that address from a *row*. Petition at 40-41.

II. ROW-BASED SRAMS IN VIEW OF *CHERITON* ARE OBVIOUS

A. Row-based SRAM memories were well-known, and are the only type of SRAMs described in the record.

There is no dispute that row-based SRAMs were well-known in the prior art. See Petition at 22-23; POPR at 6-8. To demonstrate the state of the art, the Petitioner provided both expert testimony and a corroborative reference, *Fujishima. See Fujishima* (EX1019); Seshan (EX1007) ¶¶ 62-64. As noted in the Petition, *Fujishima* teaches that "SRAM memory cell array 12 is provided with a cache row



decoder 43.... [which] is responsive to a cache row address signal ... for selecting one row in the SRAM memory cell array." *Id.* at 12:49-54; *accord id. at* 5:38-44 ("The second [SRAM] memory cell array is divided into a plurality of regions each comprising the same number of a plurality of rows").

Row-based SRAMs are the only type of SRAM in the record. Such SRAMs were so common that Dr. Seshan explained that the POSA would understand *Cheriton's* SRAM's to be row based even if not explicitly stated. Seshan (EX1007) ¶ 62. Properly understood, even the *Ross* reference cited by Patent owner used row-based SRAMs. Specifically, *Ross* cited prior art algorithms to efficiently find data in "array" (row-based) environments. *See Ross* (EX2001) at 1:38-67 (listing pre-1990 "array binary searches" indexing); Summary of Invention; Fig. 9; 7:34.

B. It would have been obvious for *Cheriton's* SRAMs to have rows.

Responding to the arguments made in the POPR (p. 7), there were multiple reasons why it would have been obvious to use rows in *Cheriton's* SRAMs. First, row-based SRAMS were not just known, but common—indeed, they are the only type of SRAMs in evidence. *See, e.g., Cubist Pharms., Inc. v. Hospira, Inc.*, 805 F.3d 1112, 1129 (Fed. Cir. 2015) (affirming obviousness because claimed purification method was "known to be one of the most common" options); *Monsanto Tech. LLC v. E.I. DuPont de Nemours & Co.*, 878 F.3d 1336, 1346 (Fed. Cir. 2018) (a "patent can be obvious in light of a single prior art reference if it would have been

DOCKET A L A R M



Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.