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Fujishima et al.

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[54]	SEMICONDUCTOR M	MEMORY	DEVICE	FOR
	SIMPLE CACHE SYSTEM			

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[21] Appl. No.: 564,657

[22] Filed:

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Related U.S. Application Data

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[30]	Foreign Application Priority Data
No	ov. 6, 1987 [JP] Japan
Dec	c. 17, 1987 [JP] Japan
[51]	Int. CL;
	G06F 13/00; G11C 7/00
[52]	U.S. Cl 395/425; 365/230.03;
	365/63; 365/49; 364/DIG. 1; 364/243.41
[58]	Field of Search 365/49, 230.03, 63;

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364/200 MS File, 900 MS File, 243.4, 243.41,

964, 964.2; 395/425

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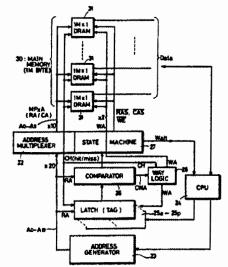
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Primary Examiner—Alyssa H. Bowler
Attorney, Agent, or Firm—Lowe, Price, LeBlanc &
Becker

[57] ABSTRACT

A semiconductor memory device comprises a DRAM memory cell array comprising a plurality of dynamic type memory cells arranged in a plurality of rows and columns, and an SRAM memory cell array comprising static type memory cells arranged in a plurality of rows and columns. The DRAM memory cell array is divided into a plurality of blocks each comprising a plurality of columns. The SRAM memory cell array is divided into a plurality of blocks each comprising a plurality of columns, corresponding to the plurality of blocks in the DRAM memory cell array. The SRAM memory cell array is used as a cache memory. At the time of cache hit, data is accessed to the SRAM memory cell array. At the time of cache miss, data is accessed to the DRAM memory cell array. On this occasion, data corresponding to one row in each of the blocks in the DRAM memory cell array is transferred to one row in the corresponding block in the SRAM memory cell

19 Claims, 12 Drawing Sheets





U.S. Patent

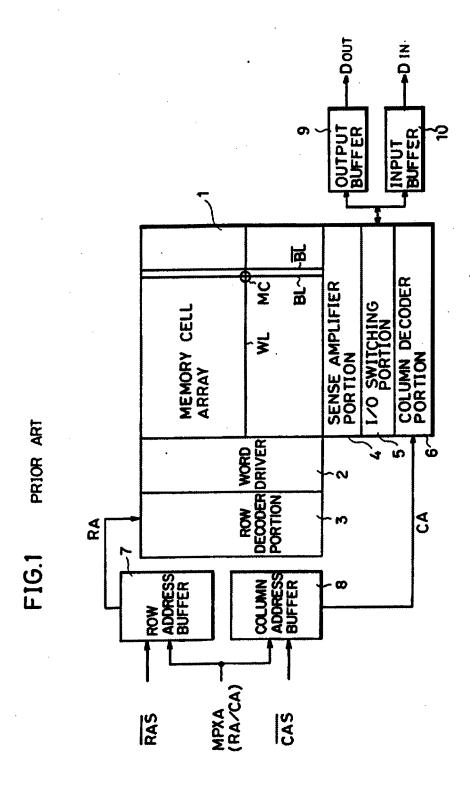


FIG.2A PRIOR ART

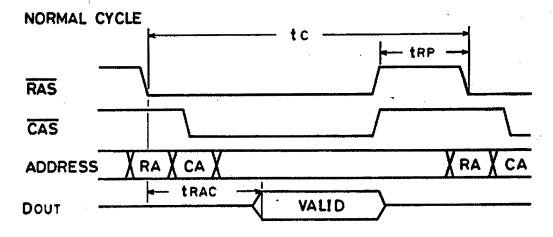


FIG. 2B PRIOR ART

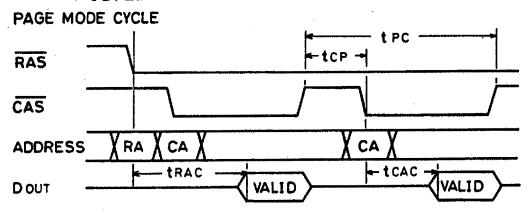


FIG.2C PRIOR ART STATIC COLUMN MODE CYCLE

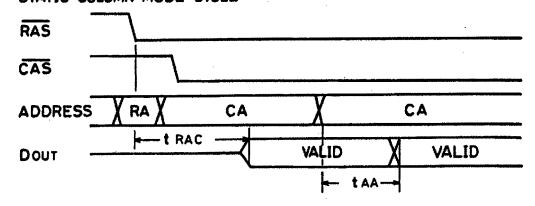
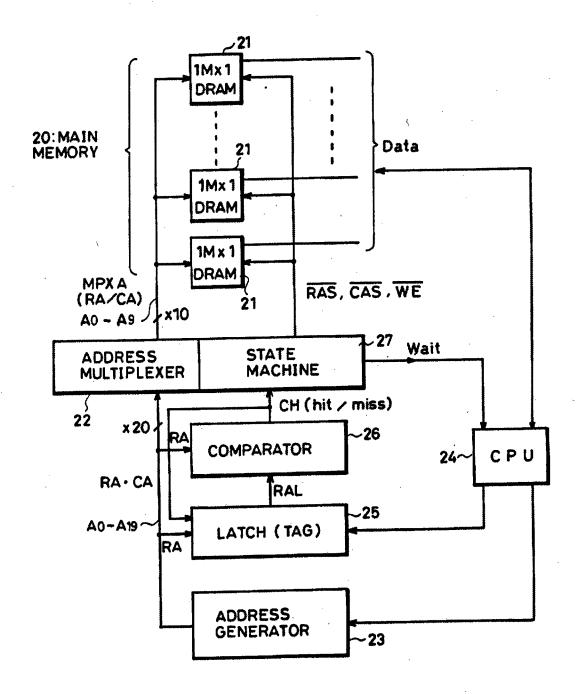




FIG.3 PRIOR ART



PRIOR ART

Sheet 4 of 12

↑ hit SYSTEM CLOCK Data CH RAS



DOCKET A L A R M

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