UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORP., CAVIUM, INC., and
WISTRON CORPORATION,
Petitioner,

v.

ALACRITECH, INC.,
Patent Owner.

Case IPR2017-01392[1]
U.S. Patent No. 7,337,241
Title: FAST-PATH APPARATUS FOR RECEIVING DATA CORRESPONDING TO A TCP CONNECTION

DECLARATION OF ROBERT HORST IN SUPPORT OF PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE TO PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,337,241

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[1] Cavium, Inc., which filed a Petition in Case IPR2017-01728, has been joined as a petitioner in this proceeding. Wistron Corporation, who filed a Petition in Case IPR2018-00328, has been joined as a petitioner in this proceeding.

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I, Robert Horst, hereby declare as follows:

I. INTRODUCTION

1. My name is Robert Horst. I have been retained on behalf of Petitioner Intel Corporation ("Intel") to provide this Declaration concerning technical subject matter relevant to the petition for *inter partes* review ("Petition") concerning U.S. Patent No. 7,337,241 (Ex. 1001, the "241 Patent"). I reserve the right to supplement this Declaration in response to additional evidence that may come to light.

2. I am over 18 years of age. I have personal knowledge of the facts stated in this Declaration and could testify competently to them if asked to do so.

3. I am being compensated for my time at the rate of $550 per hour. My compensation is not based on the resolution of this matter. My findings are based on my education, experience, and background in the fields discussed below.

4. I am an independent consultant with more than 30 years of expertise in the design and architecture of computer systems. My current curriculum vitae is submitted as Ex. 1236 and some highlights follow.

5. Currently, I am an independent consultant at HT Consulting where my work includes consulting on technology and intellectual property. I also have an appointment as an adjunct research professor at the University of Illinois in the Department of Electrical and Computer Engineering. I have testified as an expert

witness and consultant in patent and intellectual property litigation as well as *inter partes* reviews and re-examination proceedings.

6. I earned my M.S. (1978) in electrical engineering and Ph.D. (1991) in computer science from the University of Illinois at Urbana-Champaign after earning my B.S. (1975) in electrical engineering from Bradley University. During my master's program, I designed, constructed, and debugged a shared memory parallel microprocessor system. During my doctoral program, I designed and simulated a massively parallel, multi-threaded task flow computer.

7. After receiving my bachelor's degree and while pursuing my master's degree, I worked for Hewlett-Packard Co. While at Hewlett-Packard, I designed the micro-sequencer and cache of the HP3000 Series 64 processor. From 1980 to 1999, I worked at Tandem Computers, which was acquired by Compaq Computers in 1997. While at Tandem, I was a designer and architect of several generations of fault-tolerant computer systems and was the principal architect of the NonStop Cyclone superscalar processor. The system development work at Tandem also included development of the ServerNet System Area Network and applications of this network to fault tolerant systems and clusters of database servers.

8. Since leaving Compaq in 1999, I have worked with several technology companies, including 3Ware, Network Appliance, Tibion, and AlterG in the areas of network-attached storage and biomedical devices. From 2012 to

2015, I was Chief Technology Officer of Robotics at AlterG, Inc., where I worked on the design of anti-gravity treadmills and battery-powered orthotic devices to assist those with impaired mobility.

9. In 2001, I was elected an IEEE Fellow "for contributions to the architecture and design of fault tolerant systems and networks." I have authored over 30 publications, have worked with patent attorneys on numerous patent applications, and I am a named inventor on 82 issued U.S. patents.

10. My patents include those directed to networks (e.g., U.S. Pat. No. 6,157,967: Method of data communication flow control in a data processing system using busy/ready commands), storage (e.g., U.S. Pat. No. 6,549,977: Use of deferred write completion interrupts to increase the performance of disk operations), and multi-processor systems (e.g., U.S. Pat. No. 5,751,932: Fail-fast, fail-functional, fault-tolerant multiprocessor system). My publications include a conference paper that examined the performance and efficacy of protocol offload engines. Ex.1004.

11. My current Curriculum Vitae, which is filed as Ex. 1236, contains further details on my education, experience, publications, and other qualifications to render this opinion as expert.

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