

## [54] MICROCODE PROGRAM SEQUENCER

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[52] U.S. Cl. .... 340/172.5

[51] Int. Cl.<sup>2</sup> .... G06F 9/16

[58] Field of Search .... 340/172.5

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Primary Examiner—Gareth D. Shaw

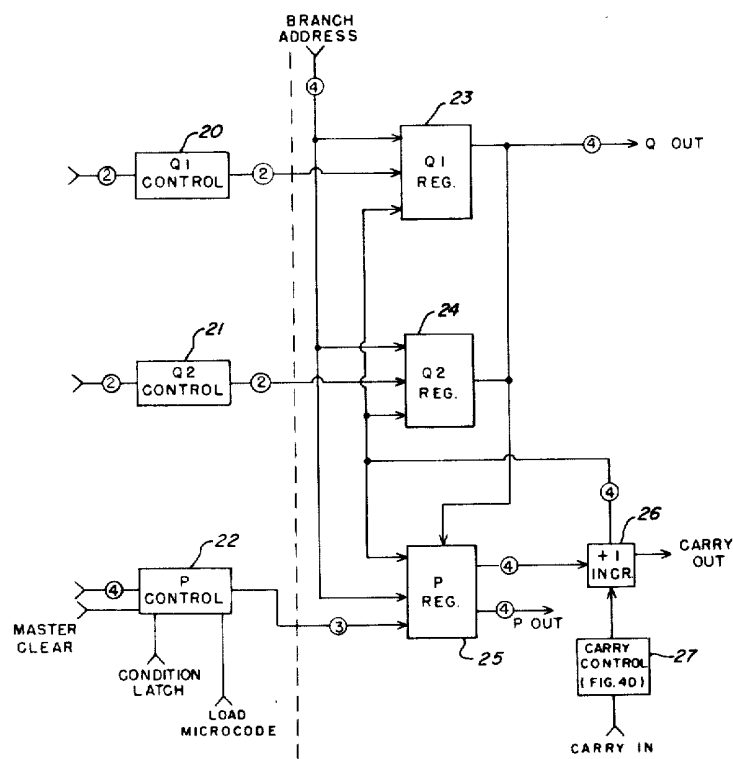
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## [57] ABSTRACT

A microcode program sequencer includes first and second registers (herein designated the Q and P registers), each connected to a computer memory to receive addresses therefrom. Control means is provided for each register such that the P register will provide output addresses to a microcode memory, whereas the Q register(s) provide output addresses to the P register. By properly operating the control means, incrementing of addresses from the P register can be accomplished, as well as address jumps and returns, using the Q register. Further, the contents of the Q register may also be incremented in synchronism with the P register, as desired. One feature of the invention resides in a conditional latch circuit which may be selectively operated as a latch or as an OR gate.

13 Claims, 9 Drawing Figures



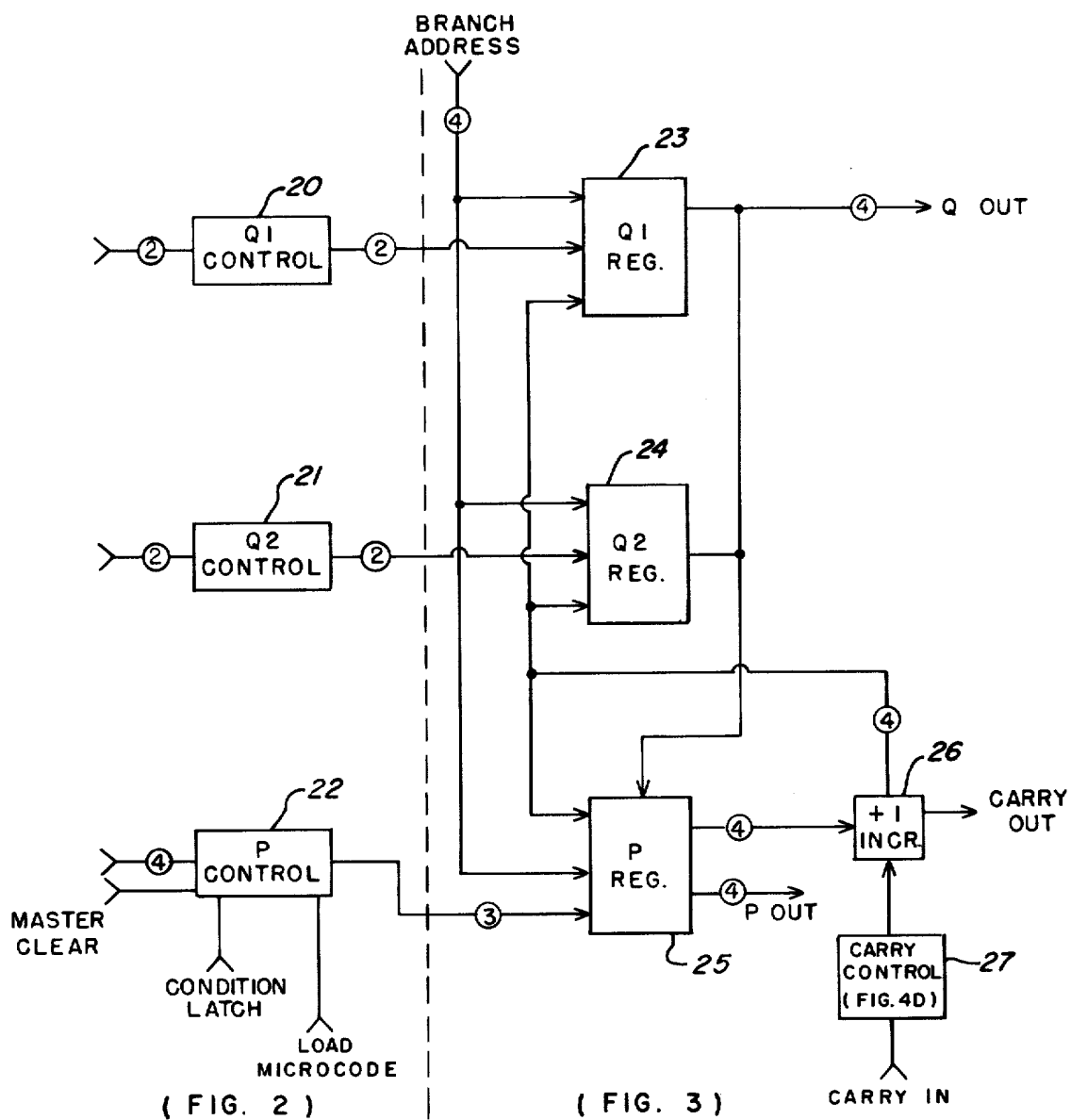


FIG. 1

FIG. 2

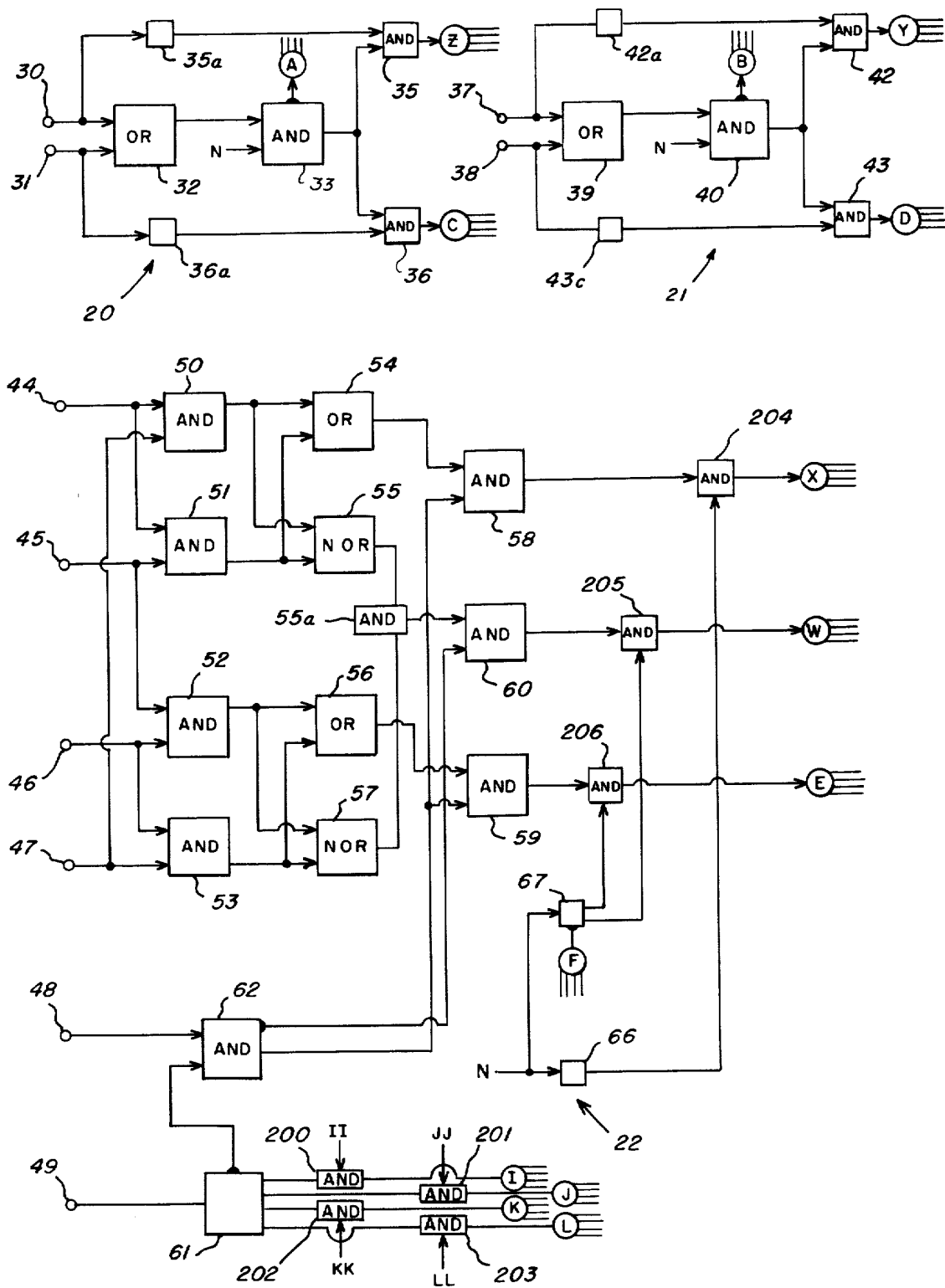
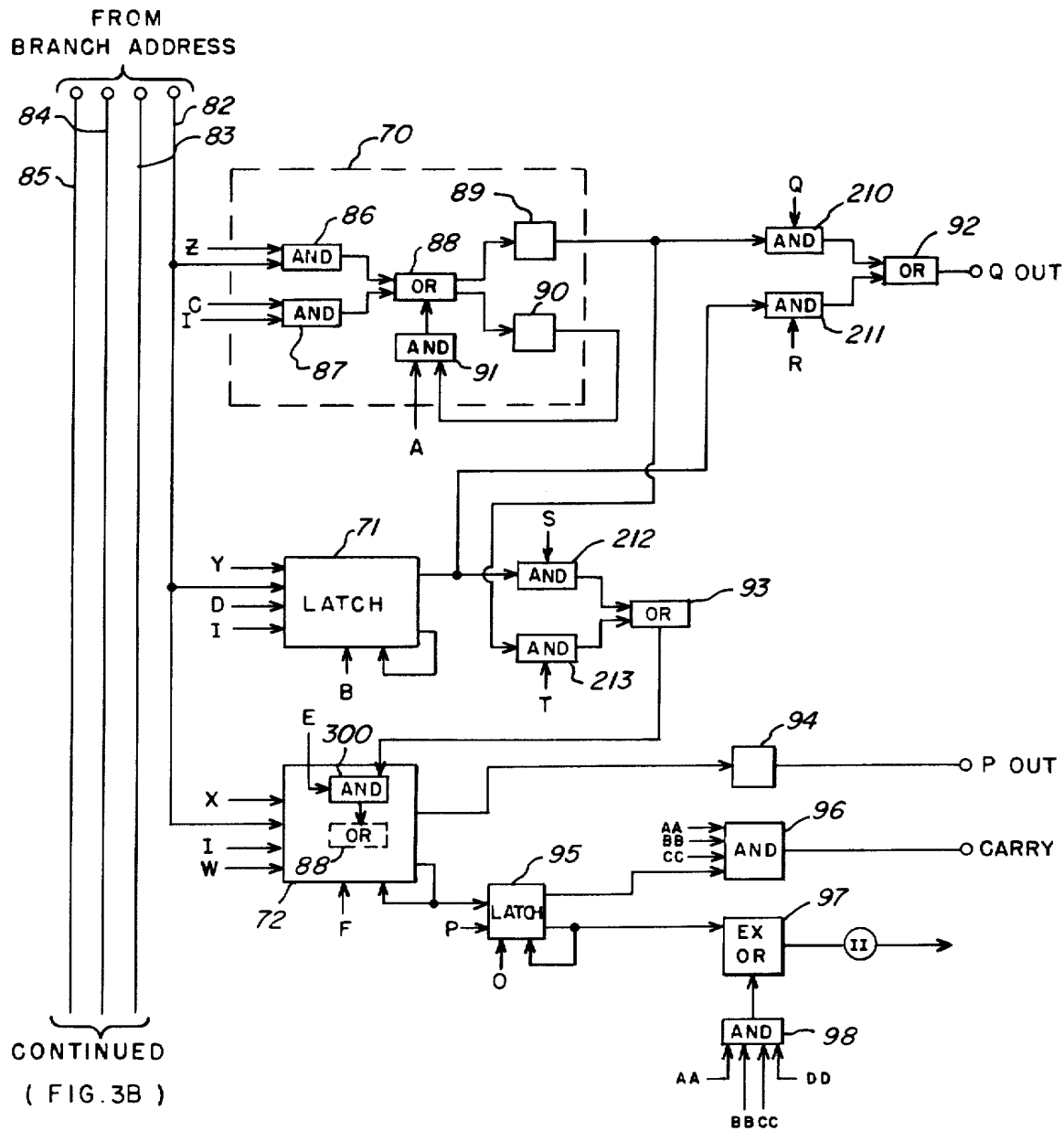
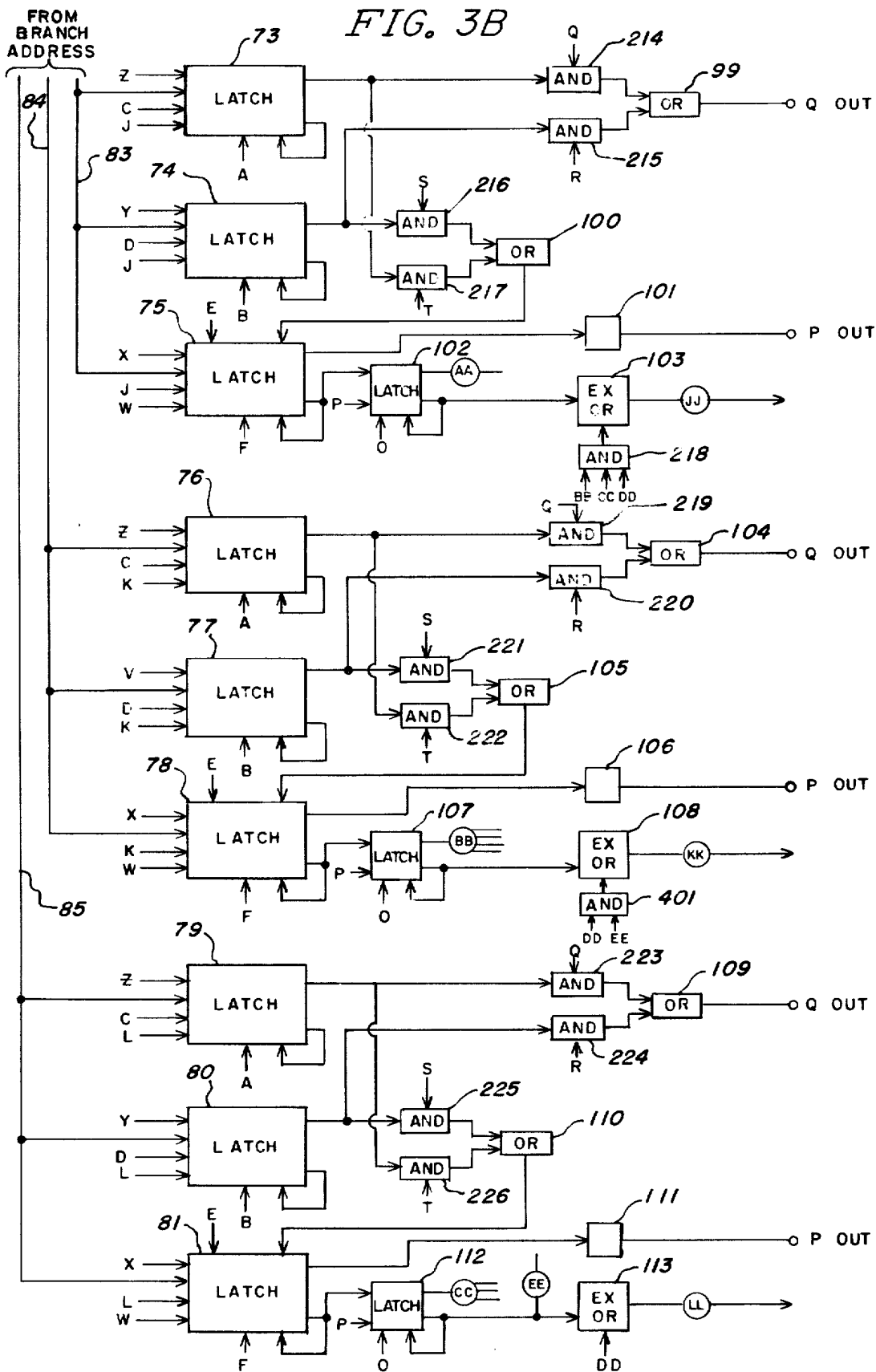


FIG. 3A







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