

[54] **PARALLEL-PIPELINED IMAGE PROCESSING SYSTEM**

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**Related U.S. Application Data**

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[60] Provisional application No. 60/006,097, Oct. 31, 1995.

[51] **Int. Cl.<sup>7</sup>** ..... **G06K 9/00**

[52] **U.S. Cl.** ..... **382/103; 382/325; 710/129; 710/132**

[58] **Field of Search** ..... **382/103, 107, 382/296, 307, 325; 395/800, 312, 309; 364/516; 348/149, 716; 701/1; 710/126, 129, 131, 132**

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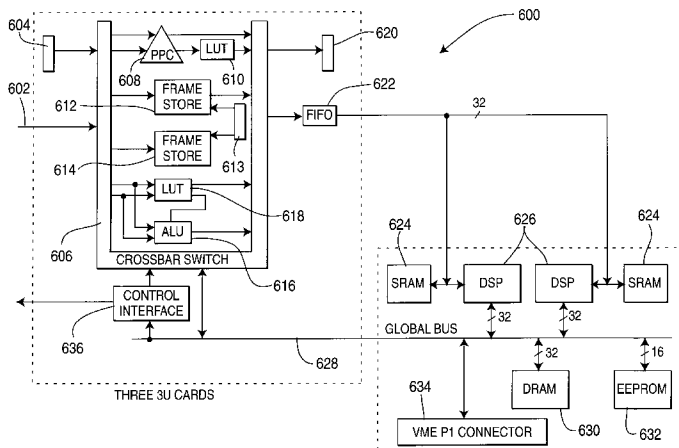
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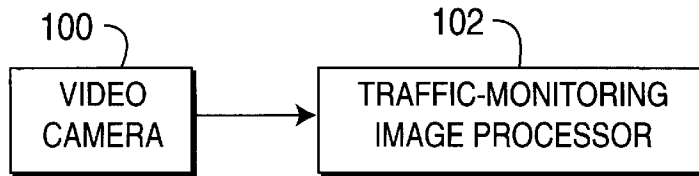
*Primary Examiner*—Jose L. Couso  
*Assistant Examiner*—Matthew C. Bella  
*Attorney, Agent, or Firm*—William J. Burke

[57] **ABSTRACT**

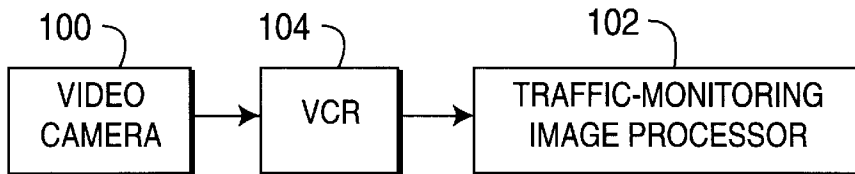
Apparatus for image processing a sequence of images containing a parallel-pipelined image processor comprised of image memories, a pyramid processing circuit, an arithmetic logic unit, a crossbar switch for video routing through the various components of the processor, signal processors to provide hardware programming through a global bus and also perform image processing operations. Images can be passed directly from the crossbar switch to internal static RAM of the signal processors through a first-in, first-out interface at full video rates.

**26 Claims, 5 Drawing Sheets**

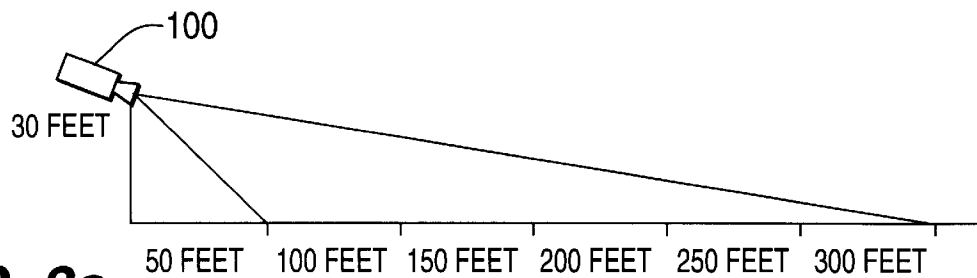




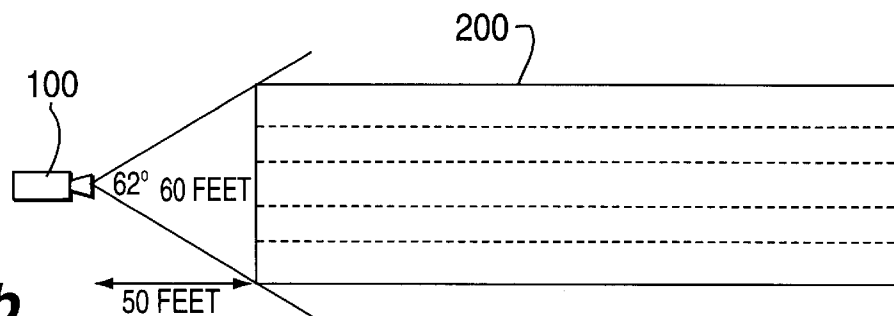
**FIG. 1a**



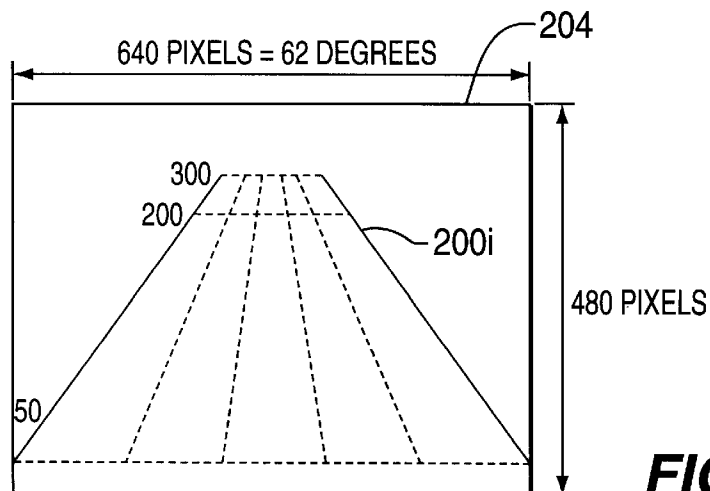
**FIG. 1B**



**FIG. 2a**



**FIG. 2b**



**FIG. 2c**

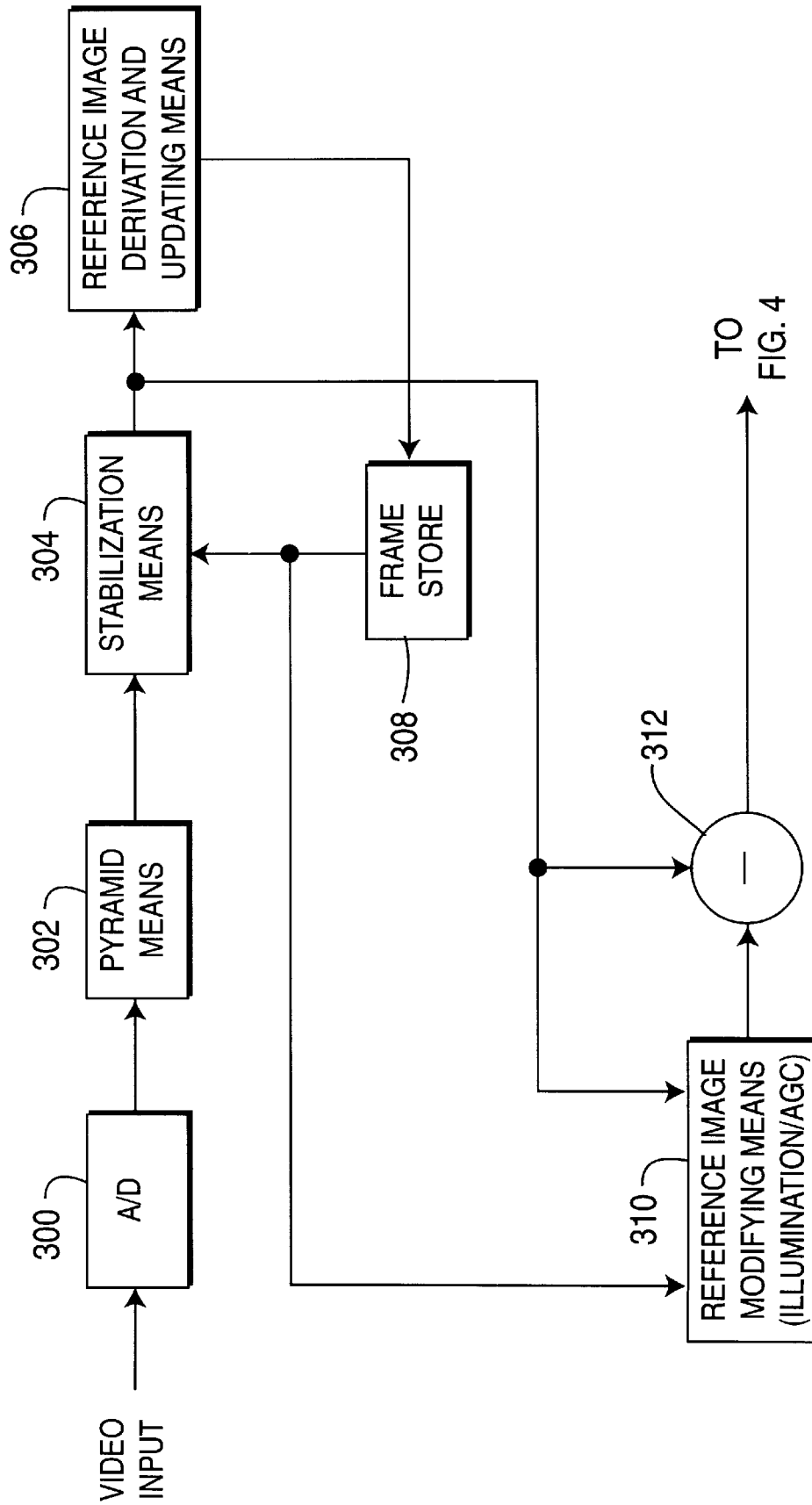


FIG. 3

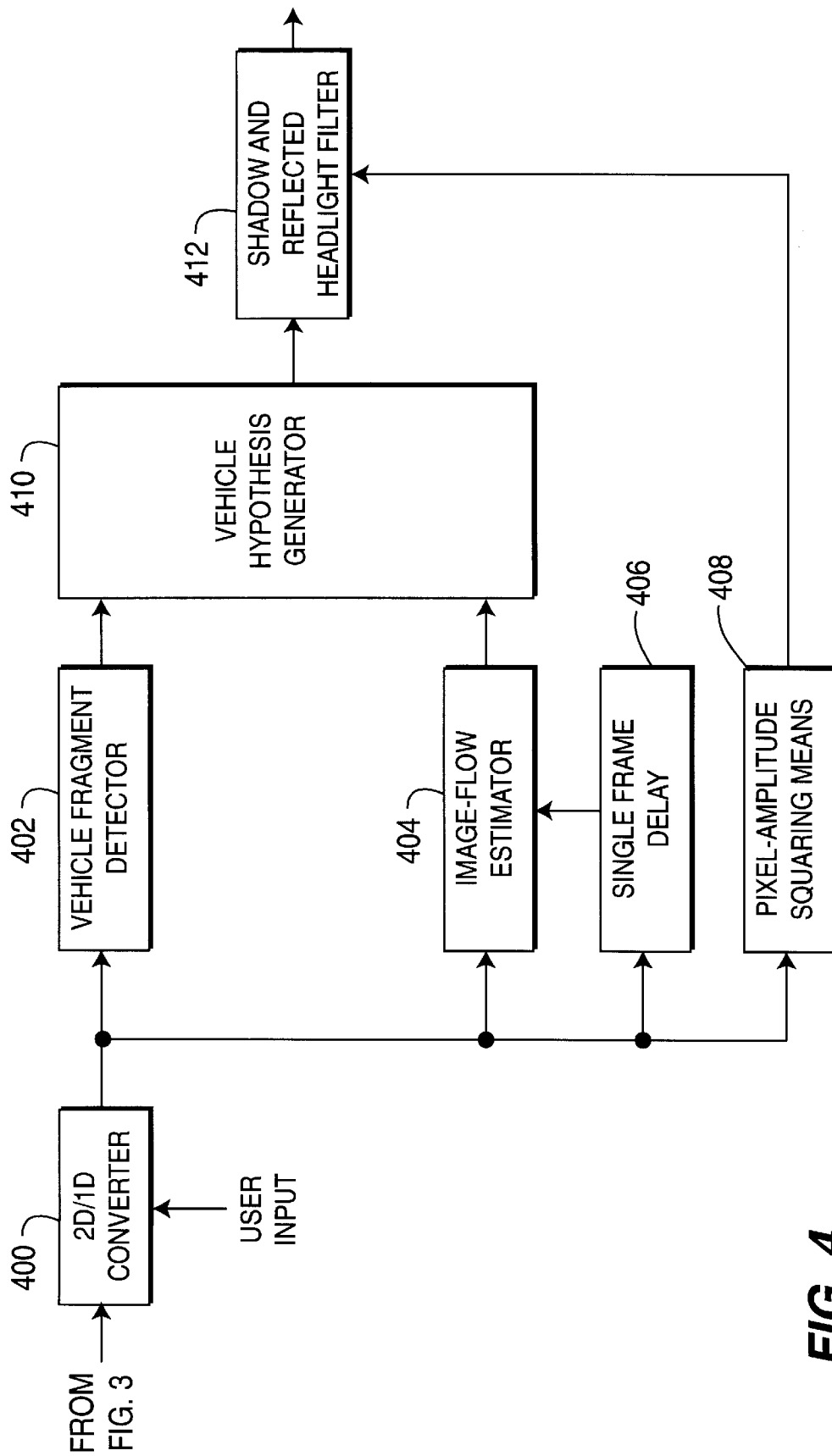
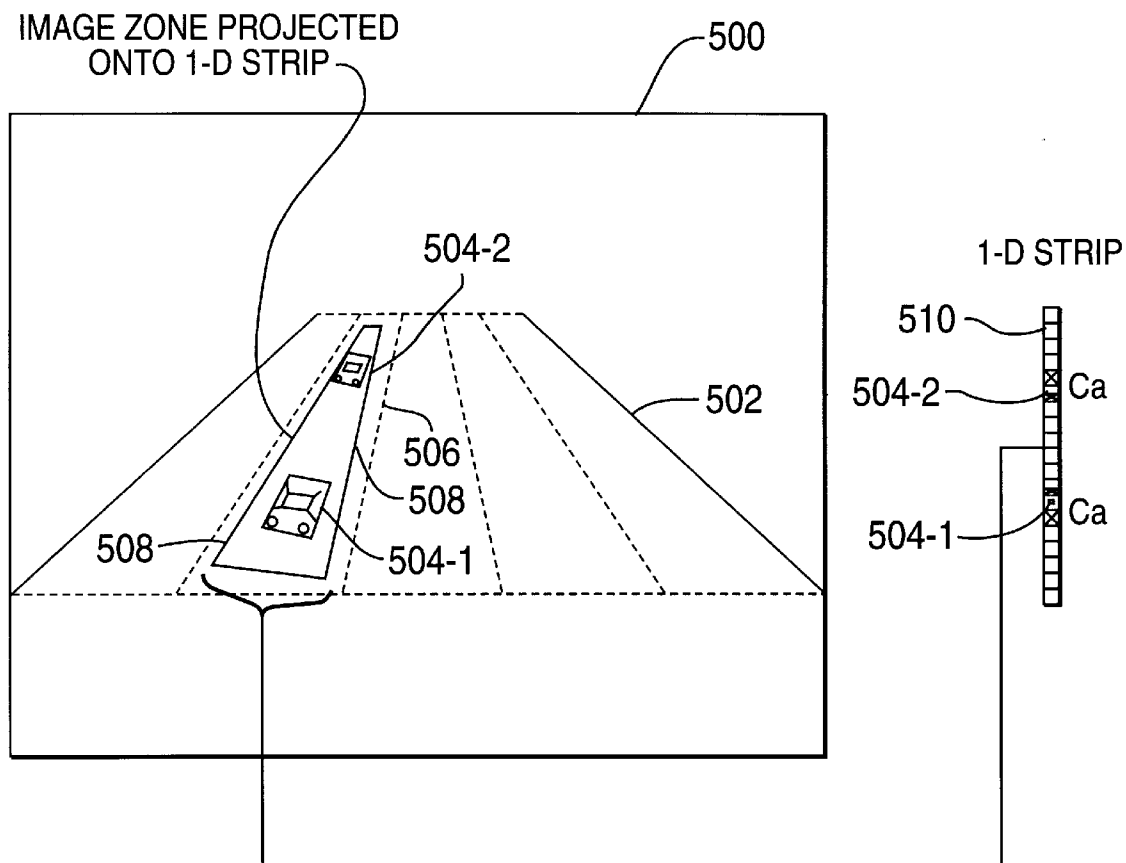
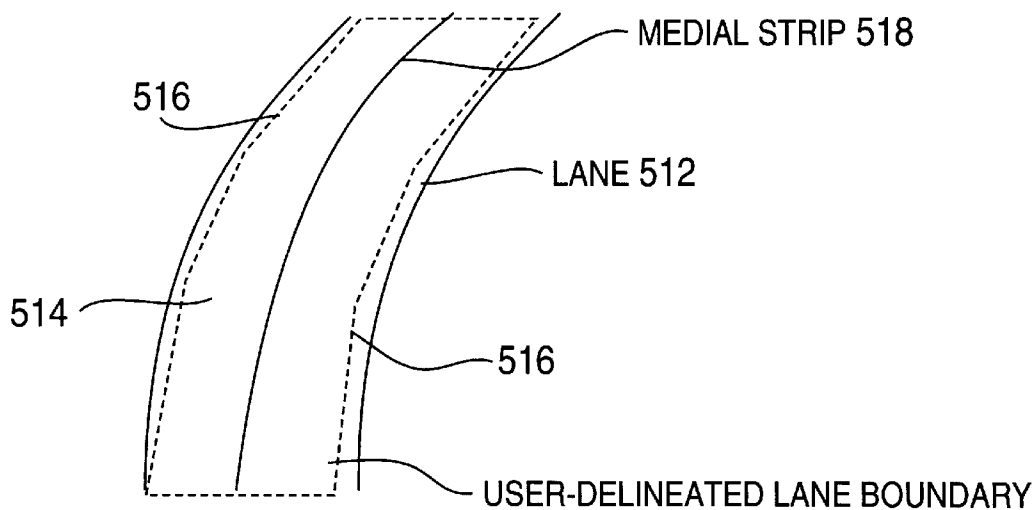


FIG. 4



**FIG. 5**



**FIG. 5a**

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