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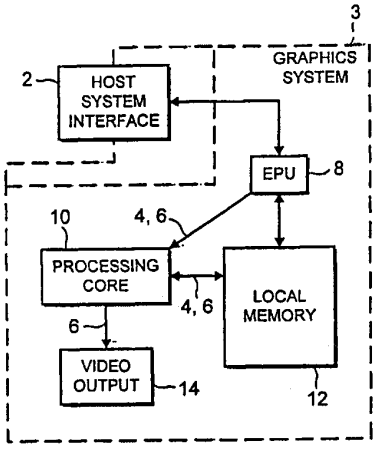
**(54) Title:** PARALLEL DATA PROCESSING APPARATUS

**(57) Abstract**

A data processing apparatus comprises a SIMD (single instruction multiple data) array (10) of processing elements. The processing elements are operably divided into a plurality of processing blocks, the processing blocks being operable to process respective groups of data items.

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# PARALLEL DATA PROCESSING APPARATUS

The present invention relates to parallel data processing apparatus, and in particular to SIMD (single instruction multiple data) processing apparatus.

## BACKGROUND OF THE INVENTION

Increasingly, data processing systems are required to process large amounts of data. In addition, users of such systems are demanding that the speed of data processing is increased. One particular example of the need for high speed processing of massive amounts of data is in the computer graphics field. In computer graphics, large amounts of data are produced that relate to, for example, geometry, texture, and colour of objects and shapes to be displayed on a screen. Users of computer graphics are increasingly demanding more lifelike and faster graphical displays which increases the amount of data to be processed and increases the speed at which the data must be processed.

A previously proposed processing architecture for processing large amounts of data in a computer system uses a Single Instruction Multiple Data (SIMD) array of processing elements. In such an array all of the processing elements receive the same instruction stream, but operate on different respective data items. Such an architecture can thereby process data in parallel, but without the need to produce parallel instruction streams. This can be an efficient and relatively simple way of obtaining good performance from a parallel processing machine.

However, the SIMD architecture can be inefficient when a system has to process a large number of relatively small data item groups. For example, for a SIMD array processing data relating to a graphical display screen, for a small graphical primitive such as a triangle, only relatively few processing elements of the array will be enabled to process data relating to the primitive. In that case, a large proportion of the processing elements may remain unused while data is being processed for a particular group.

It is therefore desirable to produce a system which can overcome or alleviate this problem.

## SUMMARY OF THE INVENTION

According to one aspect of the present invention, there is provided a data processing apparatus comprising a SIMD (single instruction multiple data) array of processing elements, wherein the processing elements are operably divided into a plurality of processing blocks, the processing blocks being operable to process respective groups of data items.

According to another aspect of the present invention, there is provided a data processing apparatus comprising an array of processing elements, which are operable to process respective data items in accordance with a common received instruction, wherein the processing elements are operably divided into a plurality of processing blocks having at least one processing element, the processing blocks being operable to process respective groups of data items.

Various further aspects of the present invention are

exemplified by the attached claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram illustrating a graphics data processing system;

Figure 2 is a more detailed block diagram illustrating the graphics data processing system of Figure 1;

Figure 3 is a block diagram of a processing core of the system of Figure 2;

Figure 4 is a block diagram of a thread manager of the system of Figure 3;

Figure 5 is a block diagram of a array controller of the system of Figure 3;

Figure 6 is a block diagram of an instruction issue state machine of the channel controller of Figure 3;

Figure 7 is a block diagram of a binning unit of the system of Figure 3;

Figure 8 is a block diagram of a processing block of the system of Figure 3;

Figure 9 is a flowchart illustrating data processing using the system of Figures 1 to 8;

Figure 10 is a more detailed block diagram of a thread processor of the thread manager of Figure 4;

Figure 11 is a block diagram of a processor unit of the processing block of Figure 8;

Figure 12 is a block diagram illustrating a processing element interface;

Figure 13 is a block diagram illustrating a block I/O interface;

Figure 14 is a block diagram of part of the processor unit of Figure 11; and

Figure 15 is a block diagram of another part of the processor unit of Figure 11.

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