US005981913A

United States Patent [19]

Kadomura et al.

[11] Patent Number: 5,981,913

[45] Date of Patent: Nov. 9, 1999

[54] **STATIC ELECTRICITY CHUCK AND WAFER STAGE**

[75] Inventors: **Shingo Kadomura**; **Tomohide Jozaki**; **Shinsuke Hirano**; **Kinya Miyashita**, all of Kanagawa; **Seiichirou Miyata**, Yamaguchi; **Yoshiaki Tatsumi**, Kanagawa, all of Japan

[73] Assignee: **Sony Corporation**, Tokyo, Japan

[21] Appl. No.: **08/821,334**

[22] Filed: **Mar. 20, 1997**

[30] **Foreign Application Priority Data**

Mar. 22, 1996 [JP] Japan 8-065625

[51] **Int. Cl.**[6] **H05B 3/68**; C23C 16/00; B23B 5/22

[52] **U.S. Cl.** **219/444.1**; 118/724; 279/128

[58] **Field of Search** 219/443, 457, 219/464, 544; 279/128, 134; 361/234; 269/8; 118/724–725

[56] **References Cited**

U.S. PATENT DOCUMENTS

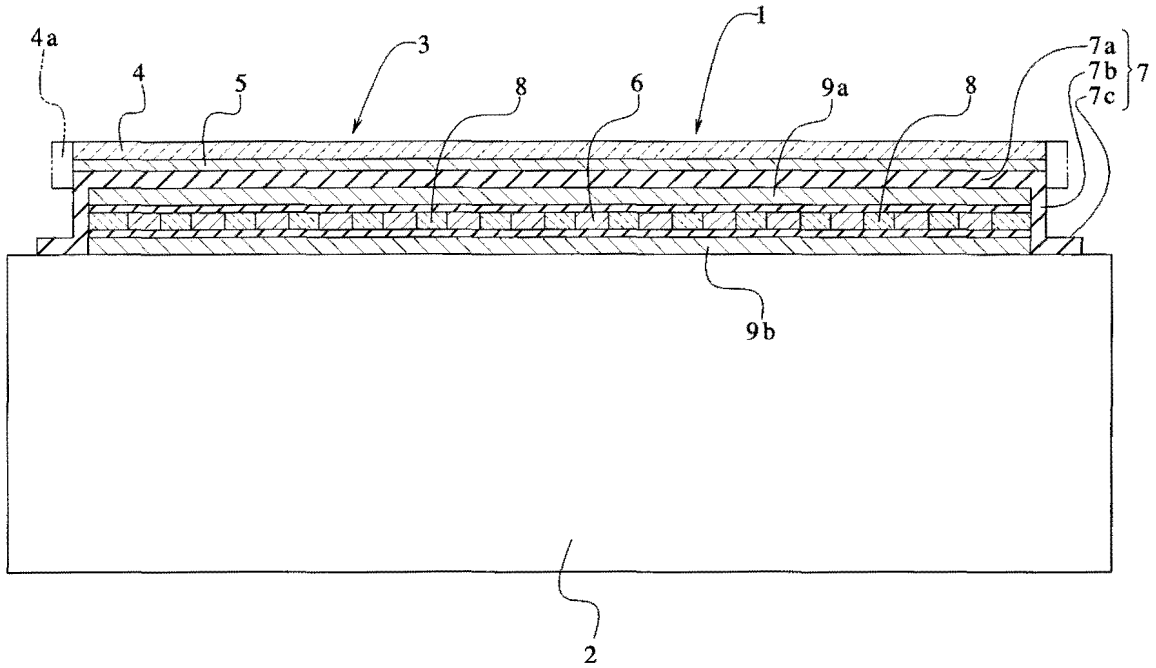
5,151,845	9/1992	Watanabe et al.	361/234
5,166,856	11/1992	Liporace et al.	361/233
5,191,506	3/1993	Logan et al.	361/234
5,280,156	1/1994	Niori et al.	361/234
5,374,807	12/1994	Yahav et al.	219/464
5,663,865	9/1997	Kawada et al.	361/234

Primary Examiner—Teresa Walberg
Assistant Examiner—Sam Paik
Attorney, Agent, or Firm—Hill & Simpson

[57] **ABSTRACT**

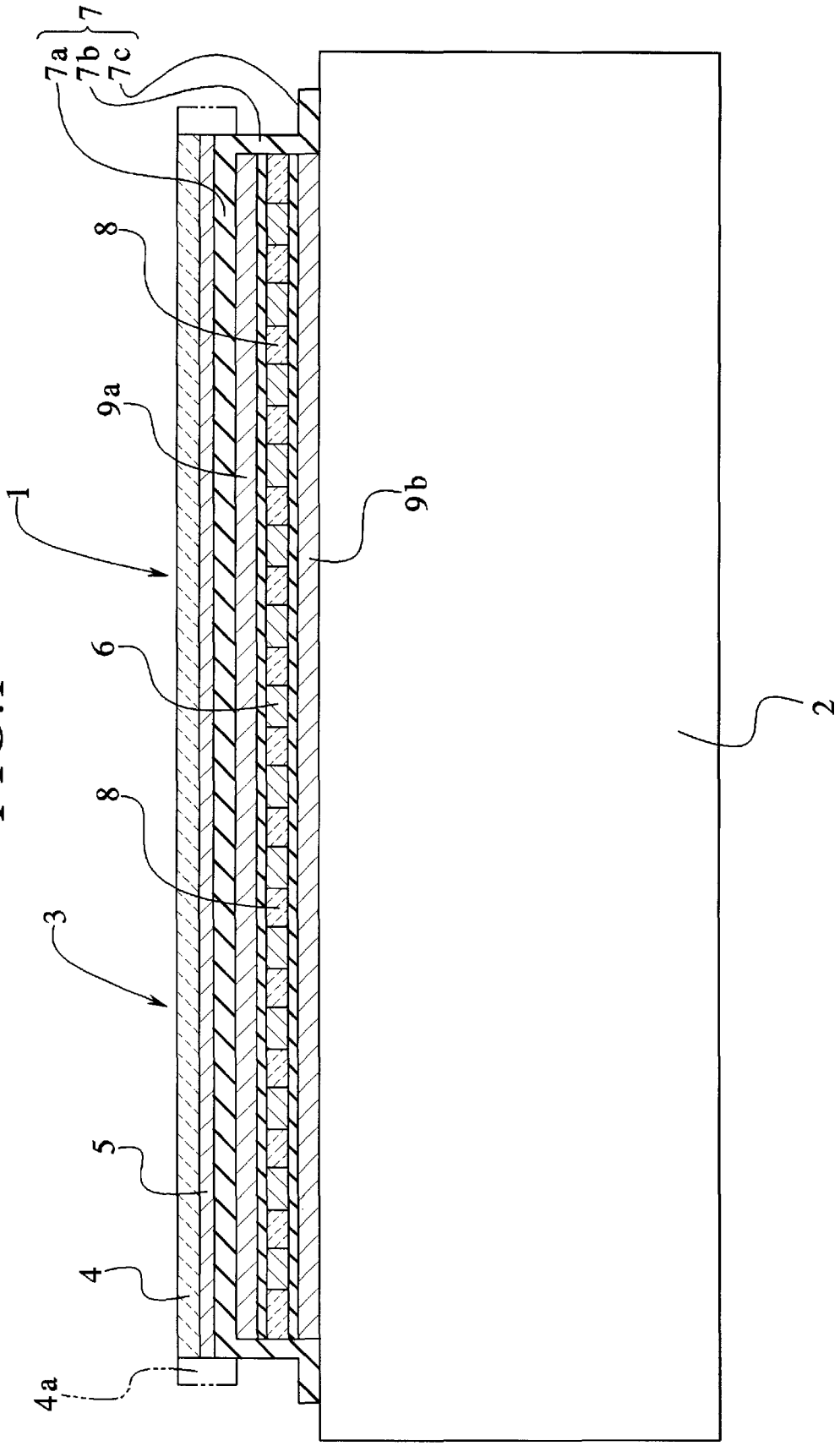
There are provided a static electricity chuck which can vary the temperature of a wafer in a short time without adversely effecting throughput, and a wafer stage having the static electricity chuck. The static electricity chuck includes a dielectric member 4 formed of insulating material, an electrode 5 of conductor which is disposed at the lower side of the dielectric member 4, and a heater 6 which is disposed at the lower side of the electrode 5 and heats the dielectric member 4. The wafer stage 1 includes the static electricity chuck which is provided on a metal jacket having cooling apparatus.

9 Claims, 3 Drawing Sheets



Tokyo Electron Limited
EXHIBIT 1002
IPR Petition for

FIG.1



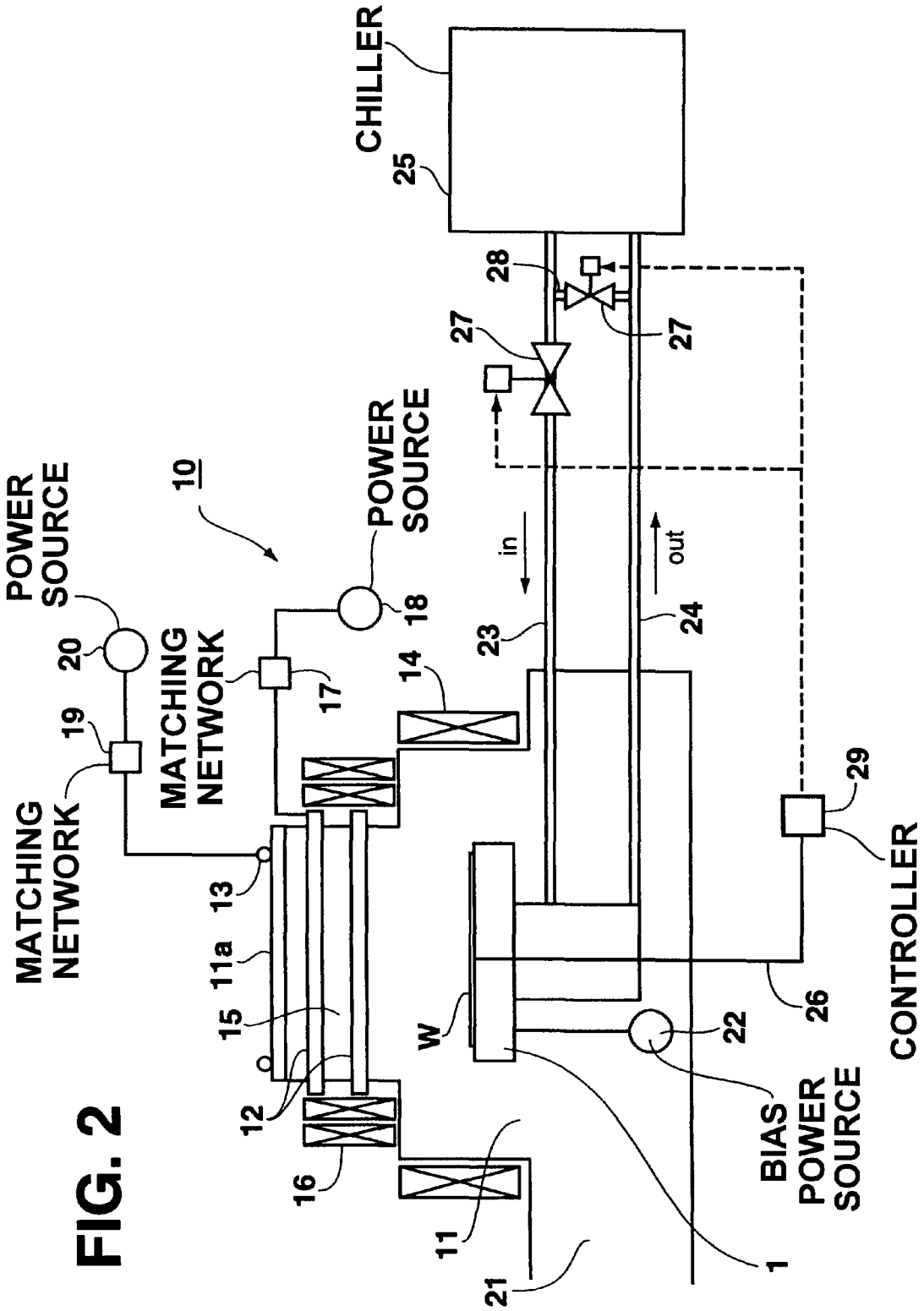


FIG. 2

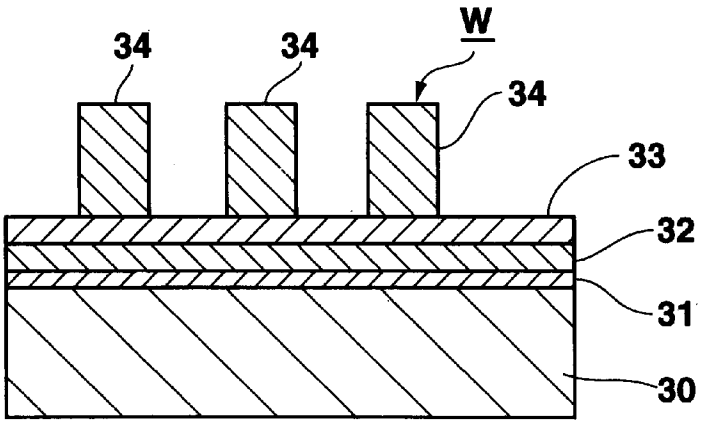


FIG. 3A

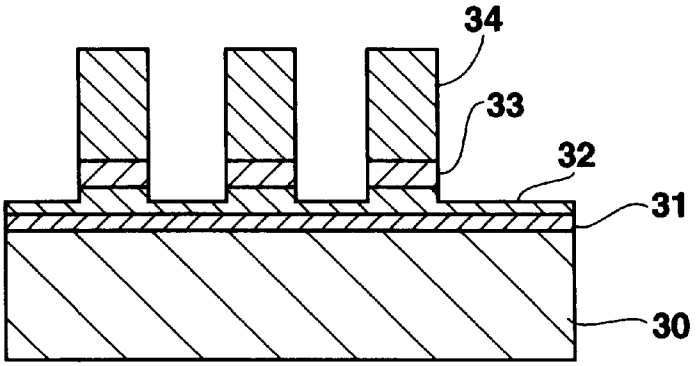


FIG. 3B

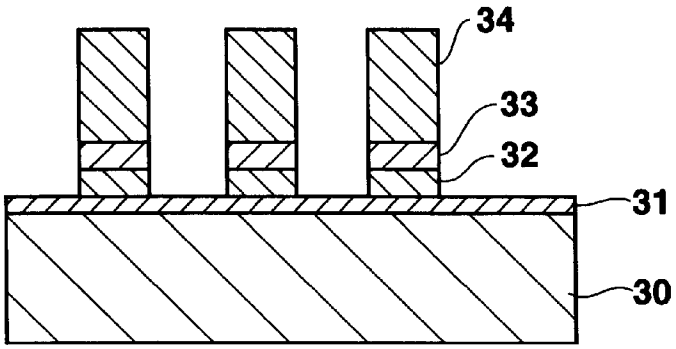


FIG. 3C

STATIC ELECTRICITY CHUCK AND WAFER STAGE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a static electricity chuck which is used to adsorptively hold a wafer in a manufacturing apparatus for a semiconductor device such as an etching device or the like, and a wafer stage having the static electricity chuck.

2. Description of Related Art

Recently, a technical requirement for the micromachining in a super LSI technique has been increasingly severer. For example, with respect to an etching treatment, it is indispensable to use a treatment method which can achieve both a high-precision micromachining which suppress a dimensional conversion difference as much as possible, and a high selection ratio to a back layer.

It is well known that when materials other than oxide film are subjected to a plasma etching treatment, a so-called side wall protection film is used to ensure an anisotropic shape. That is, when reaction products generated during the plasma etching treatment are re-dissociated in plasma, and these re-dissociated materials are deposited as various kinds of deposits such as organic polymer, etc. on the side walls of a pattern to thereby form a side wall protection film. The side wall protection film thus formed serves to protect the side walls from being etched.

As described above, the side wall protection film is formed by the deposits which are generated from the reaction products. Therefore, when a pattern formed by an etching treatment is convex, the thickness of the side wall protection wall is relatively larger as the width of the pattern is finer, and thus the whole pattern width is liable to be still smaller than a desired width. Accordingly, as described above, the fineness of each pattern is promoted, and if the pattern width is small (narrow), the dimensional precision of the pattern thus obtained is reduced when the anisotropy of the etching is achieved by using the side wall protection film.

In order to solve the above disadvantage, a technique of performing an etching treatment while exhausting at high speed has been recently attempted and considered to ensure the dimensional precision. In this high-speed exhausting process, a pump having a higher exhausting speed than a conventional etching treatment apparatus is secured, and the conductance of etching gas is improved to shorten the residence time of the etching gas during the etching treatment, whereby the re-dissociation of reaction products in plasma is suppressed during the etching treatment. According to the high-speed exhausting process as described above, the amount of deposits which are generated by the re-dissociation of the reaction products can be greatly reduced, so that the absolute value of the dimensional conversion difference and the dispersion thereof can be remarkably suppressed.

However, in the high-speed exhausting process as described above, the reaction products are quickly exhausted, resulting in reduction of a supply source for forming a side wall protection film. Therefore, a side wall protection film is not formed at a sufficient thickness, and the anisotropic shape is not sufficiently ensured. Accordingly, there occurs a new problem that the precision in shape of a pattern obtained when an overetching is carried out is lowered.

That is, when a substrate-applied bias is lowered to ensure the selection ratio to the back layer in the overetching process, occurrence of side etching or notching is unavoidable because the side wall protection film is thin and thus weak. On the other hand, when the applying bias is increased to ensure the shape precision, the selection ratio to the back layer is lowered.

In view of the foregoing, a low-temperature etching technique for cooling a wafer so that the temperature of the water is reduced to zero degree or less in the etching treatment is proposed as a technique which can solve the trade-off problem between the selection ratio and the shape precision as described above and achieve both the selection ratio and the anisotropic shape. This low-temperature etching technique is proposed by K. Tsujimoto, et al. in "Proceedings of Symposium on Dry Process" pp 42–49 on 24th and 25th of Oct. 1988 in Tokyo.

According to this technique, radical reaction is suppressed by reducing the temperature of samples to keep the anisotropy even under a low substrate-applied bias.

However, this low-temperature etching technique has the following disadvantages.

First, it is difficult to process those materials like W polyside for which reaction products have different vaporization pressures. If the temperature of samples are reduced to a low temperature suitable for etching of polysilicon to etch W polyside because reaction products such as WCl_x, WO_xCl_y, etc. which are generated by the etching treatment of WSi_x have low vaporization pressure, it would be impossible to perform the etching of WSi_x.

Secondly, ΔT (the difference between a set temperature of a sample stand and wafer temperature) increases during the etching treatment That is, for example, in a contact hole processing work, the setting of the low temperature is effective to ensure the selection ratio to the back layer of Si, however, the low-temperature setting induces the contact hole to be tapered in shape due to excessive deposition of polymer. Therefore, as described above, it is difficult to set the low-temperature condition, and incident energy must be increased to dissociate Si—O bonds in the contact hole processing work, resulting in increase of ΔT.

Accordingly, in the low-temperature etching treatment as described above, the etching must be performed at an incompletely low temperature.

In order to solve this disadvantage, it may be considered that the set temperature of a sample such as wafer or the like is varied between materials whose reaction products are different in vaporization pressure, or between an just etching treatment and an over etching treatment. However, if the set temperature is varied in the midst of the etching treatment, the throughput would be reduced, and it is inconvenient on cost.

Accordingly, there has been required a mechanism which can vary the temperature of a wafer in short time with no effect on the throughput, that is, which enables quick temperature reduction and increase.

OBJECT AND SUMMARY OF THE INVENTION

An object of the present invention is to provide a static electricity chuck which can vary the temperature of a wafer in short time without adversely effecting throughput, and a wafer stage for the static electricity chuck.

In order to attain the above object, according to a first aspect of the present invention, a static electricity chuck comprises a dielectric member formed of insulating

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.