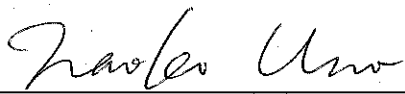


CERTIFICATION

I, Naoko UNO, c/o Sakai International Patent Office, 5F, Toranomom Mitsui Building 8-1, Kasumigaseki 3-chome, Chiyoda-ku, Tokyo, 100-0013, Japan, do hereby certify that I am fluent in the English and Japanese languages and a competent translator thereof, and that to the best of my knowledge and belief the following is a true and correct translation of the accompanying Non-English Language Japanese Patent Application Laid-Open Publication No. JP08-191059 A.

I certify under penalty of perjury under the laws of the United States that the foregoing is true and correct.

Executed this 20th day of January, 2017.

Signature: 

Naoko Uno

Tokyo Electron Limited
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(54) [Title of the Invention] PLASMA PROCESSING APPARATUS

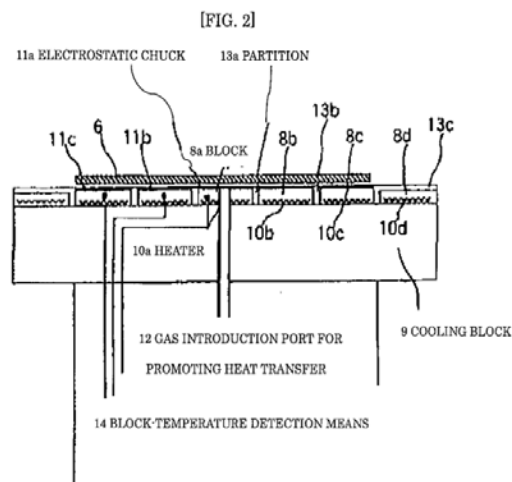
(57) [ABSTRACT]

[CONSTITUTION]

In a plasma processing apparatus provided with a plasma source and a stage 7 for holding a processed object in a processing chamber 1 to heat or cool the processed object, the stage 7 is divided into a plurality of blocks 8 and a heat quantity transmitted from the processed object to the stage 7 is controlled for each block 8, so that the temperature distribution of the processed object can be controlled freely, and the temperature of the processed object is uniform during plasma processing.

[PURPOSE]

It is possible to freely control the temperature distribution of the processed object, and in a semiconductor manufacturing process, a finer and higher-performance semiconductor can be manufactured. In addition, it is possible to reduce dust falling on the processed object and to improve the yield of semiconductor elements.



[Claim(s)]

[Claim 1] A plasma processing apparatus characterized in that the apparatus comprises: a plasma source; and a stage configured to hold a processed object in a processing chamber and to heat or cool the processed object, the stage being divided into a plurality of blocks, and a temperature of each of the blocks is set independently from each other so that a temperature distribution of the processed object can be set.

[Detailed Description of the Invention]

[0001]

[Industrial Applicability] The present invention relates to a plasma processing apparatus that allows temperature distribution control of a processed object.

[0002]

[Description of the Prior Art] In recent years, a semiconductor device has become still smaller, and higher scale integration has been achieved. In order to manufacture a semiconductor device with higher precision, it is necessary to set various conditions which affect processes. Among semiconductor processes used today, many of the film formation and etching processes are plasma processing, in which a processing gas is introduced into a vacuum chamber, and ionized by energy of a direct voltage, a μ wave, a high-frequency wave, and the like, so that a film is formed on a semiconductor wafer and etched.

[0003] The temperature of a semiconductor wafer (hereinafter referred to as wafer) during the plasma processing is one of the important parameters determining the precision achieved in the processing, and it is required to uniformize the wafer temperature distribution during the processing.

[0004] In the plasma processing apparatuses, for example, in an etching apparatus, a wafer is heated by plasma during processing, and hence, it is necessary to cool the wafer in order to keep the wafer temperature at a desired level. A first conventional technique for cooling a wafer uses an electrostatic force to hold the wafer on to a cooled stage as described in JP S56-53853 B and JP S57-44747 B. A second conventional technique for cooling a wafer holds the wafer onto the stage by mechanical means such as a clamp and introduces a gas between the wafer and the stage to promote cooling as described in JP H2-27778 B and JP H2-30128 A. A third conventional technique for cooling a wafer introduces a gas between the wafer and the stage while holding the wafer by an electrostatic force as described in JP S58-32410 A and JP S60-115226 A.

[0005] When these methods are employed, the wafer temperature is determined according to heat input from plasma and the heat transmission rate between the stage and the wafer. In the first conventional technique, there is a problem that a wafer cannot be sufficiently cooled due to an insufficient heat transmission rate. In the second and third conventional techniques, there is a problem that even though heat input from plasma is uniform in the surface of the wafer, a temperature distribution is generated in the wafer such that the temperature of the outer periphery thereof is higher because the gas pressure between the stage and the wafer is lower in the vicinity of the outer periphery of the wafer. In addition, in each case, when heat input from plasma is not uniform, a temperature distribution is generated according thereto.

[0006] In addition, one of important problems for a semiconductor manufacturing process as typified by a plasma processing process is foreign matter (dust) falling on a wafer. In plasma processing such as CVD and etching, dust particles which have been grown in plasma, or dust particles peeled off from a surface of a processing chamber fall on the wafer, which causes deterioration of the film quality and reduction of the process yield.

[0007] As described in one literature (Shiratani et al. Jpn. J. Appl. Phys. 30 (1991) 1887.), it is known that dust particles are negatively charged in plasma and suspended above the wafer or the electrode in an electric field formed by plasma. The behavior of the dust particles is affected by gravity, gas flow, electric field, magnetic field, and the like; however, the behavior also relates to a wafer temperature which causes thermophoresis.

[0008] As described in detail in one literature (G. M. Jellum et al. J. Appl. Phys. 67 (1990) 6490.), for example, it is reported that dust particles with the diameter of 0.5 μm move from a high temperature side to a low temperature side along an equipotential surface due to a thermophoresis effect caused by temperature gradient of several $^{\circ}\text{C}/\text{mm}$ in a parallel-plate argon RF discharge (0.5 Torr) with electrode interval of 25 mm.

[0009] Here, in a plasma etching apparatus, for example, since an object exposed to plasma is heated by incident ions, usually a wafer is actively cooled in order to obtain desired etching characteristics, and the periphery of the wafer or the electrode is lowest in temperature in the processing chamber. From the perspective of the thermophoresis effect, this satisfies a condition for easily collecting dust in the chamber. Therefore, it is expected that dust particles will be gathered near the wafer due to thermophoresis from a member around a processed object exposed to plasma, a chamber wall surface, and the like.

[0010]

[Problem to be solved by the invention] An object of the present invention is to uniformize the temperature distribution of a processed object, to obtain better plasma processing characteristics, and to reduce dust particles falling on the processed object.

[0011]

[Means for solving problem] The above problem is solved by configuring a stage which allows a free control of the temperature distribution of the processed object.

[0012]

[Function] According to the present invention, by configuring a stage which heats and cools a processed object so that the temperature distribution of the processed object can be freely controlled, it is possible to uniformize the temperature of the processed object and to obtain uniform plasma processing characteristics when the processed object is subjected to plasma processing.

[0013] Furthermore, by setting the temperature distribution in the processed object and an object(s) around it to a predetermined temperature distribution (for example, a temperature distribution where the temperature decreases from the processed object to its periphery) before blocking plasma, it is possible to guide dust particles in plasma in a direction away from the processed object and to reduce dust particles falling on the processed object upon plasma blocking.

[0014]

[Embodiment] Although the present invention is not limited to the field of semiconductor manufacturing, since it seems that the present invention is most useful for a semiconductor manufacturing apparatus and a semiconductor manufacturing process, an embodiment will be described in a case where a semiconductor wafer is used as a processed object and a microwave plasma etching apparatus is used as a plasma processing apparatus.

[0015] Fig. 1 is a cross-sectional view illustrating an embodiment of the present invention. The microwave plasma etching apparatus includes a processing chamber 1, a process gas introduction system 2, a microwave generation unit 3, a waveguide 4, a coil 5, a stage 7 for holding a wafer 6. The stage 7 also serves as an electrode for applying a high frequency to the wafer 6. Details of the stage 7 are illustrated in Fig. 2, and the stage 7 is divided into a plurality of blocks 8a, 8b, Since the wafer 6 is approximately circular, it is desirable that the blocks be divided as illustrated in Fig. 3. The number of blocks is determined according to the accuracy degree of controlling the temperature distribution of the wafer. It is desirable that the blocks be made of a metal material with high thermal conductivity such as aluminum. In addition, the blocks are partitioned by partitions 13 made of a material lower in thermal conductivity than the block, such as a ceramic material. All the blocks are cooled by one cooling block 9. It is preferable that the cooling block be also made of a metal material with high thermal conductivity such as aluminum. Furthermore, the blocks 8a, 8b, ... incorporate heaters 10a, 10b, ..., respectively, and the heaters are separately controlled. Therefore, it is possible to separately set the temperature for each block by controlling the output of the heater. Electrostatic chucks 11a, 11b, ... are formed on the surfaces of the blocks 8a, 8b, ..., respectively, and it is possible to electrostatically attract the wafer thereon. Furthermore, a gas of several Torr for promoting thermal conduction is introduced between the wafer and the stage. By using the stage having the above configuration, it is possible to freely set the temperature distribution of the wafer. That is, in order to increase the temperature at the center of the wafer, it is only necessary to increase the temperature of the block 10a by increasing the output from the heater 10a in Fig. 2. In contrast, in order to uniformize the wafer temperature in a case where the wafer temperature is not uniform even though the temperatures of the blocks are the same (in a case where heat input to the wafer from plasma is not uniform), it is only necessary to lower the set temperature of the block in contact with a portion high in temperature.

[0016] In addition, by adding a block-temperature detection means 14 for detecting the temperature of the block itself as illustrated in Fig. 2 or further preferably, by adding a wafer-temperature detection means 15 as illustrated in Fig. 4, and by controlling a heat transfer quantity between each block and the wafer using a detected temperature, it is possible to always control the temperature distribution of the wafer to a desired temperature distribution even if heat input to the wafer changes.

[0017] Being able to change the temperature distribution of the wafer contributes to reduction in dust falling on the wafer. Fig. 5 illustrates a flowchart of an etching process which is an embodiment according to the present invention. As described above, during the etching, dust generated due to etching or generated from the chamber wall surface or the like is charged and float near the wafer. It is desirable that the wafer temperature be uniform as much as possible because of a demand for uniformizing etching. At the time point when the etching processing is nearly finished, if the temperature distribution is made to change such that the temperature of the center portion of the wafer is high and the periphery thereof is low without blocking plasma, dust moves to a peripheral portion due to a thermophoresis effect caused by temperature gradient on the wafer. At this time, if a portion whose temperature is lowest is provided outside the wafer (block 8d in the embodiment illustrated in Fig. 2), the dust is gathered to the portion. Therefore, by blocking plasma after removing dust on the wafer, it is possible to reduce dust falling on the wafer when blocking plasma. In addition, in the case where enlargement of the temperature distribution of the wafer before blocking plasma has an adverse effect on the etching process, it is possible to minimize the effect on the etching process by changing the temperature distribution of the wafer after changing plasma into clean plasma which hardly affects the wafer, such as argon plasma as illustrated in the flowchart of Fig. 6.

[0018]

[Effect of the invention] The plasma processing apparatus according to the present invention can freely control the temperature distribution of a processed object, and in the semiconductor manufacturing process, can manufacture a smaller and higher-performance semiconductor by making the wafer temperature distribution during plasma processing uniform. In addition, the plasma processing method according to the present invention can reduce dust falling on the processed object and can improve the yield of semiconductor elements.

[Brief Description of the Drawings]

[Fig. 1] Fig. 1 is a cross-sectional view illustrating one embodiment according to the present invention.

[Fig. 2] Fig. 2 is a cross-sectional view illustrating the one embodiment according to the present invention.

[Fig. 3] Fig. 3 is a perspective view illustrating block division on a stage.

[Fig. 4] Fig. 4 is a cross-sectional view illustrating a second embodiment according to the present invention.

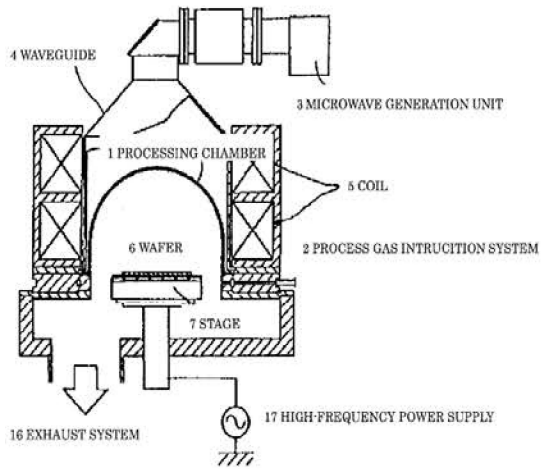
[Fig. 5] Fig. 5 is a flowchart illustrating the one embodiment according to the present invention.

[Fig. 6] Fig. 6 is a flowchart illustrating the second embodiment according to the present invention.

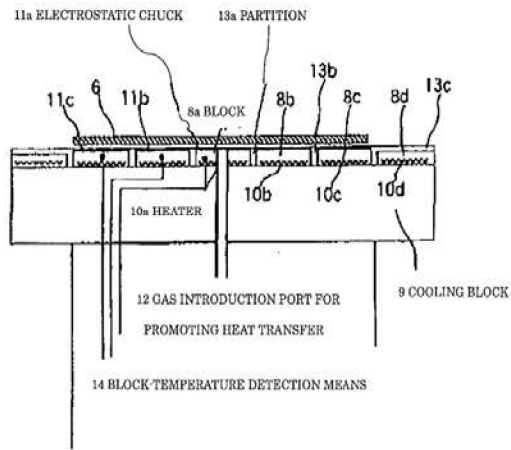
[Reference Signs List]

1 processing chamber, 2 process gas introduction system, 3 microwave generation unit, 4 waveguide, 5 coil, 6 wafer, 7 stage, 8 block, 9 cooling block, 10 heater, 11 electrostatic chuck, 12 gas introduction port for promoting heat transfer, 13 partition, 14 stage-temperature detection means, 15 wafer-temperature detection means, 16 exhaust system, 17 high-frequency power supply

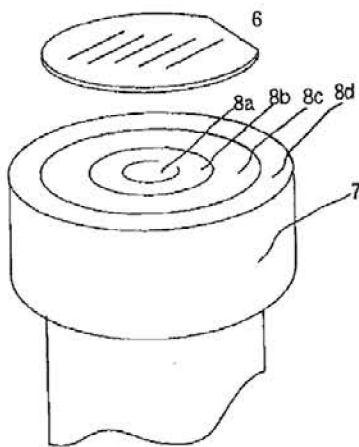
[FIG. 1]



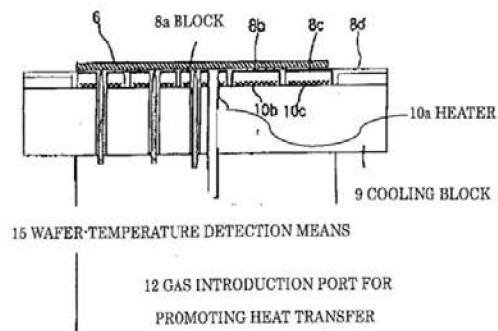
[FIG. 2]



[FIG. 3]



[FIG. 4]



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