

# Significance of JEDEC DIMM Module

Wednesday, September 25, 2002

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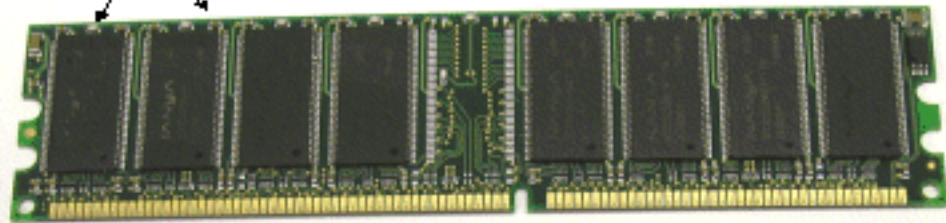
### Abstract

Non-JEDEC compliance memory modules have been flooding the market resulting in computer systems and confusion. System integrators and consumer are easily tempted by short-term cost saving without knowing its long-term consequence. This article illustrates the design process in JEDEC Raw cards. It highlights the details on proper memory module design. Whether it is clock net, stub length, termination resistor, or impedance control, thousands of hours of simulation and engineering. The resulting Gerbers are offered to you. It might make you think differently next time you pick up a memory module.

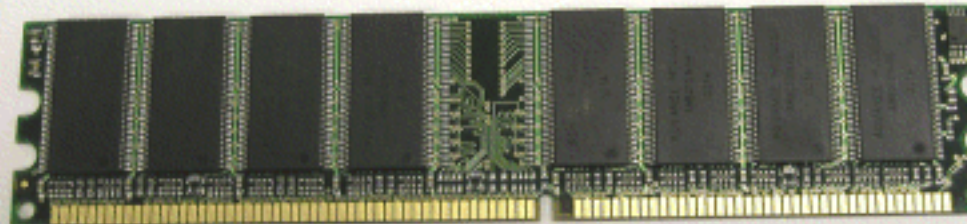
### General

We are seeing DIMM modules with only half of the number of bypass capacitors on modules with screened on resistors with value vary 30% across the same board. We are seeing modules made out of 4 layer printed circuit boards instead of 6 layer boards. We are seeing a module that has the correct circuitry but fail to work in the computer system. We are seeing memory module manufacturers cut all corners to reduce cost and to gain sales. We are frustrated at the many memory modules that do not work properly in our systems. That is when JEDEC, the semiconductor standard setting committee, gets into the picture. A standard on memory modules is needed to make sure every memory module works in every computer. With a unified standard, we can therefore, enjoy the benefit of state-of-the-art technology at the same time attending the lowest price.

Bypass Capacitors



Some DIMM Only Have Half Number of Capacitors



## Why is JEDEC Important?

JEDEC is an organization made up of 300 plus member companies from all over the world. It consists of memory vendor companies like Micron, Samsung, Infineon, Hynix and module manufacturers like Kingston, Smart Modular, and Wintec. Connector manufacturers like Molex, and Foxconn. Memory user companies like Sun Micro, Silicon Graphics, and other companies like Tektronix, Agilent and CST. Chipset companies like Nvidia, Via and

All these companies realize that the only way to have the best price for memory system is to promote one mainstream technology for the entire industry. Therefore, these companies get together 4 times a year all into one room with their differences set aside and concentrate on formulating a standard memory that the industry can accept. The standard design memory devices and modules that will work reliably in the computer system becomes the minimum requirement for the memory market. It is recognized by all manufacturers and is supported by the entire industry.

Member companies worked together on specification, simulation, prototyping, experimental parameters and system validations. A guideline is set down so that all JEDEC certified memories will be functionally inter-changeable with similar performances

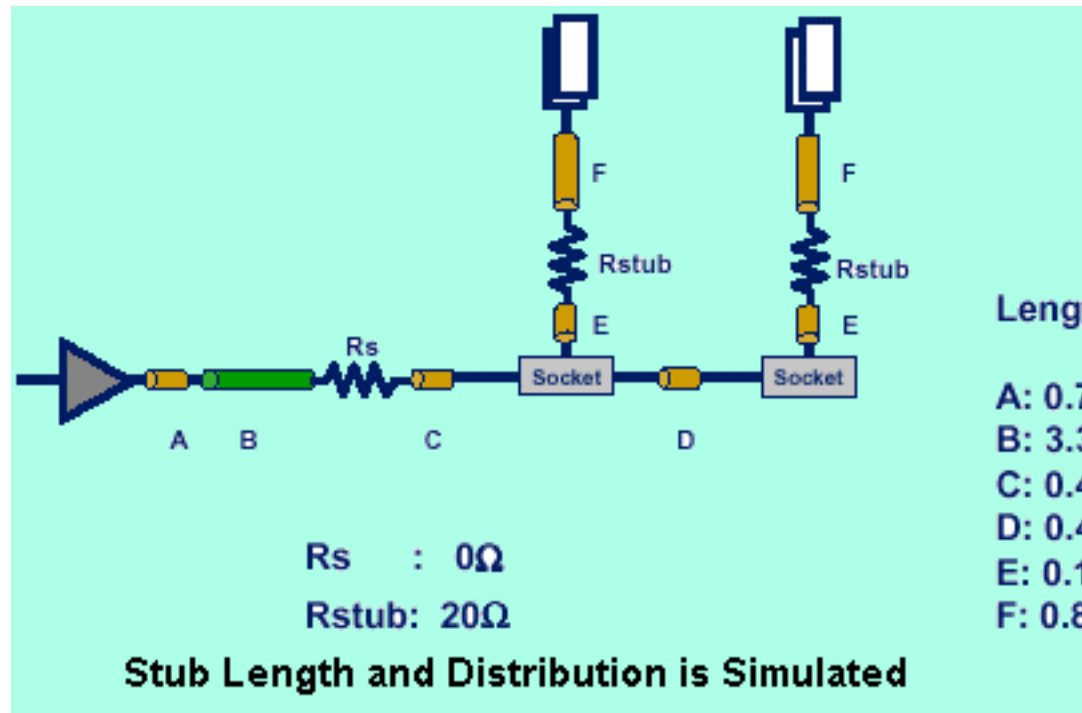
## Developing a JEDEC Memory Specification

JEDEC has been looking ahead for the needs of the semiconductor memory industry for many years. It started the work on DDR memory back in 1997. Through its efforts, DDR became the mainstream memory in the computer industry. JEDEC has just now completed the specification for DDR-II which should fill the market by 2005. The next task is DDR-III which is expected to materialize by 2007

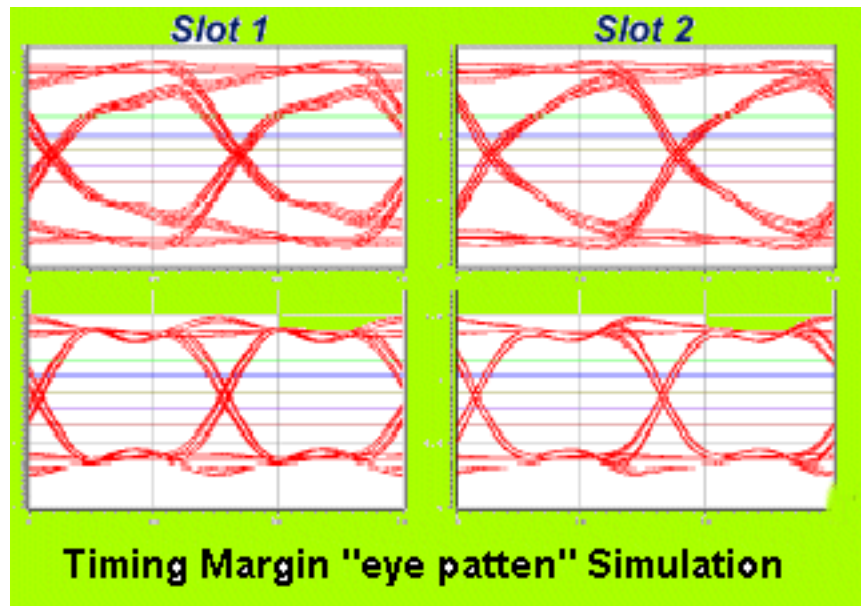
JEDEC's design procedure starts out with series of survey to users and semiconductor vendors. The user companies are asked what they would want while vendor companies are asked what they can practically produce economically not now but several years down the line. Both companies have to look at the memory bandwidth required to support their applications. Whether it is video streaming, 4G handset or fiber-to-home networking, systems designers have to forecast their memory requirements in speed, feature, and in density. The semiconductor vendors are asked to look at their process technology down the line. The challenge is before them for tighter line width technologies. Memory cores working at 2.5V power will have to go to 1.8V and 1.2V to gain the extra speed and bandwidth in a few years.

One of the major tasks for JEDEC is to assign pin-out for memory device and module. Whether it is for the memory chip or the memory module, pin-out assignment is critical. The layouts of the motherboard and the DIMM have to be done to find the optimum routing. Special attention is applied to minimize lead inductance and to accommodate a universal design for different die sizes in the future. Not to mention mechanical support and reliability

specifications.

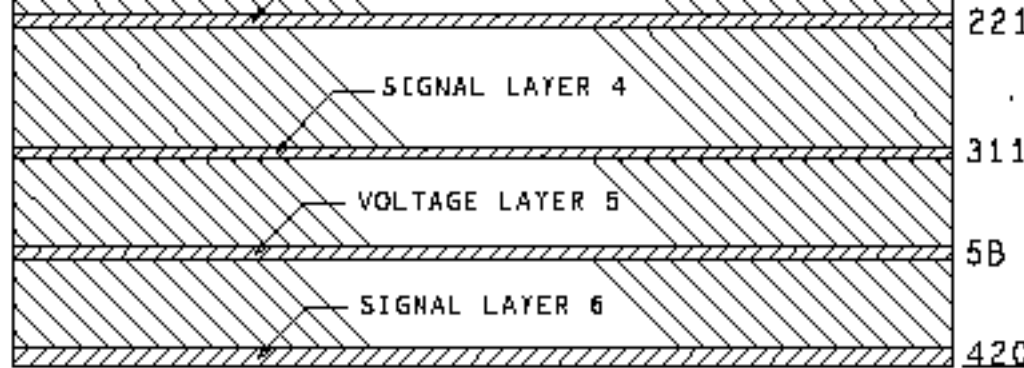


Before the engineer has a chance to build the system, he must also figure out how much margin his system has before hand. He takes the worst cases tolerance on hold jittering, and a lot of other factors into the calculation and comes up with an "eye simulation" that tells how much margin the system has when incorporated with the



After all these simulation and calculations, the engineer might decide on one particular value for the PC board to give best performance. He has, therefore, layout his P

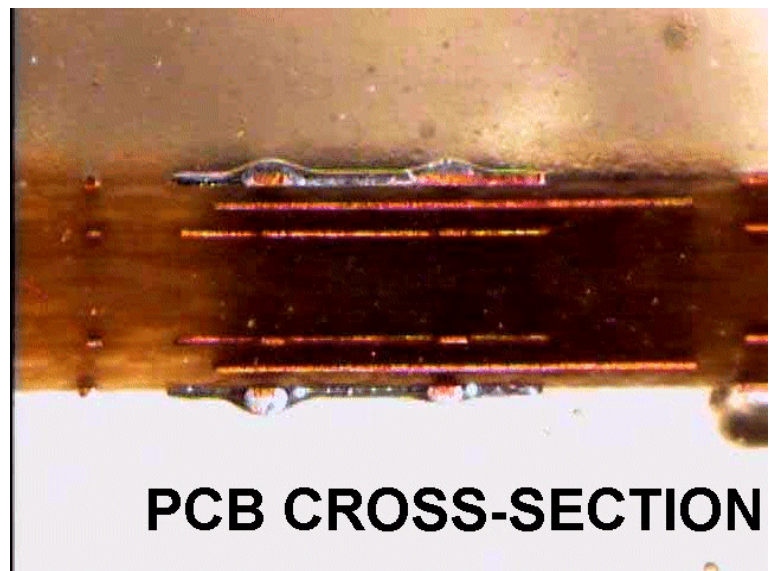
CORE 2



```
4 SUGGESTED STACKUP WITH THICKNESSES.  
LAYER [1] = SIGNAL (NAME=TOP,THICKNESS=1.0, DIELECTRIC  
INSULATOR (THICKNESS=4.2, DIELECTRIC=4.1)  
LAYER [2] = PLANE (NAME=GND,THICKNESS=1.2, DIELECTRIC  
INSULATOR (THICKNESS=5.2, DIELECTRIC=4.1)  
LAYER [3] = SIGNAL (NAME=S2,THICKNESS=1.2, DIELECTRIC  
INSULATOR (THICKNESS=20.0, DIELECTRIC=4.1)  
LAYER [4] = SIGNAL (NAME=S3,THICKNESS=1.2, DIELECTRIC  
INSULATOR (THICKNESS=5.2, DIELECTRIC=4.1)  
LAYER [5] = PLANE (NAME=VDD,THICKNESS=1.2, DIELECTRIC  
INSULATOR (THICKNESS=4.2, DIELECTRIC=4.1)  
LAYER [6] = SIGNAL (NAME=BOTDOM,THICKNESS=1.8, DIELECTRIC
```

### PCB Stack Specifications

Engineers also like to add measurement coupons (blank lines) on their PC board for the measurement of the actual impedance. In such case, a TDR (Termination Dependent Reflection) measurement is taken at the PC board manufacturing to determine the accuracy of the impedance. The impedance control can also be examined with a cross-section of the board measured under a microscope.



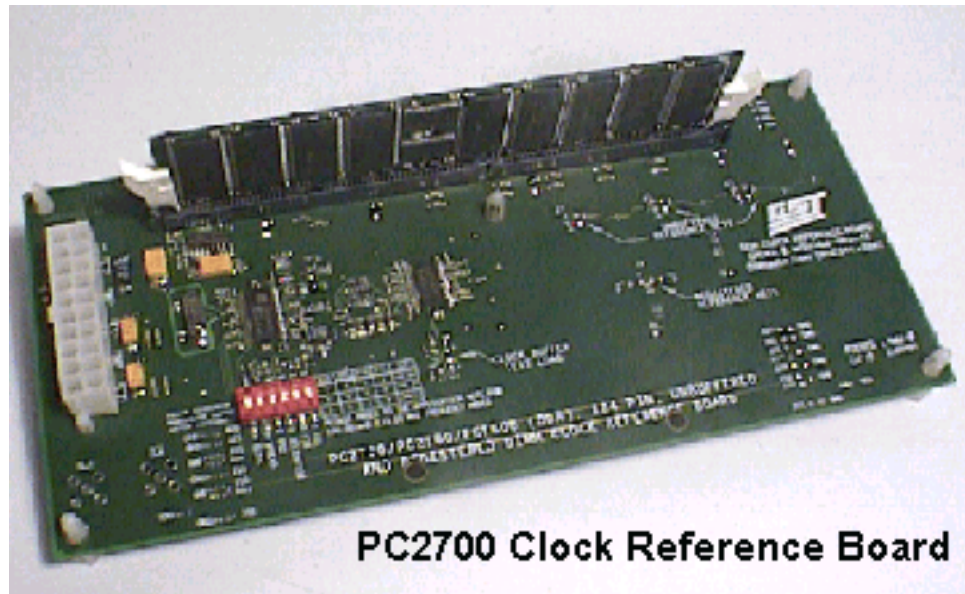
**PCB CROSS-SECTION**

## Memory Module System Validation

JEDEC members put these Raw Cards to test in different motherboards to verify in the system. The motherboard memory sockets are usually fully populated. Full tests are performed at 4 temperature/voltage extreme corners (low and high) to uncover a real actual operational environment. Clock arrival at the memory chip is also checked for timing delays with the help of a JEDEC Standard Clock Reference Board.

## JEDEC Standard Clock Reference Board

JEDEC members have determined that if common design modules are to work in a motherboard, the module clock skew is a very critical factor. Therefore, JEDEC has a Standard Clock Reference Board to be used for an industry wide uniform calibration. Many different Clock Reference Boards are made over time for the different generations of memory modules. There is the 133MHz CRB for 133Mhz SDRAM modules. There are also CRB for DDR DIMM as well as a new version for the PC2700 DIMM



The Clock Reference Board is a standard clock generator split into different clock paths. One path goes to a standard clock termination load while the other clock path goes to the memory chips. This provides the engineer with a mechanism to measure and to correct clock arrival

time to the chips on the module with an oscilloscope. Any unwanted skew can, therefore, be corrected by adding capacitors to the feedback of the clock PLL (phase lock loop)

These CRB's are manufactured in one batch of PCB and one batch of uniform components to minimize the variations. The result is the best way to unify the industry on clock timing, thus the assurance of modules will work in different systems.

## Proper Memory Module Manufacturing, Meeting JEDEC Standard

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