



US007414312B2

(12) **United States Patent**
Nguyen et al.

(10) **Patent No.:** **US 7,414,312 B2**
(45) **Date of Patent:** **Aug. 19, 2008**

(54) **MEMORY-MODULE BOARD LAYOUT FOR USE WITH MEMORY CHIPS OF DIFFERENT DATA WIDTHS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 569 days.

(21) Appl. No.: **10/908,718**

(22) Filed: **May 24, 2005**

(65) **Prior Publication Data**

US 2006/0267172 A1 Nov. 30, 2006

(51) **Int. Cl.**

H01L 23/34 (2006.01)
H05K 7/00 (2006.01)
G11C 5/06 (2006.01)

(52) **U.S. Cl.** **257/724; 257/786; 257/E23.141; 361/760; 361/784; 361/803; 365/63**

(58) **Field of Classification Search** None
See application file for complete search history.

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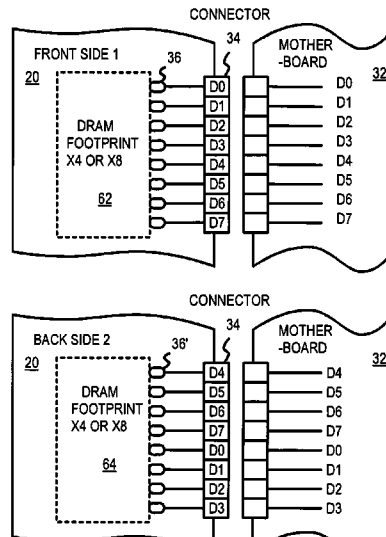
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(57) **ABSTRACT**

A memory module substrate printed-circuit board (PCB) has multi-type footprints and an edge connector for mating with a memory module socket on a motherboard. Two or more kinds of dynamic-random-access memory (DRAM) chips with different data I/O widths can be soldered to solder pads around the multi-type footprints. When $\times 4$ DRAM chips with 4 data I/O pins are soldered over the multi-type footprints, the memory module has a rank-select signal that drives chip-select inputs to all DRAM chips. When $\times 8$ DRAM chips with 8 data I/O pins are soldered over the multi-type footprints, the memory module has two rank-select signals. One rank-select drives chip-select inputs to front-side DRAM chips while the second rank-select drives chip-select inputs to back-side DRAM chips. Wiring traces on the PCB cross-over data nibbles between the solder pads and the connector to allow two $\times 4$ chips to drive a byte driven by only one $\times 8$ chip.

20 Claims, 7 Drawing Sheets



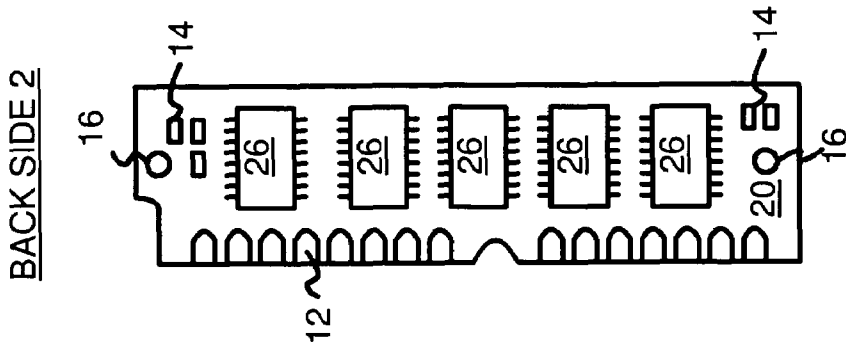


FIG. 1B

PRIOR ART

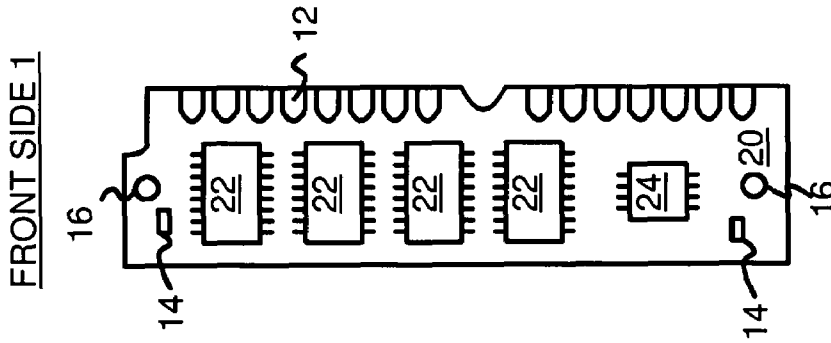


FIG. 1A

PRIOR ART

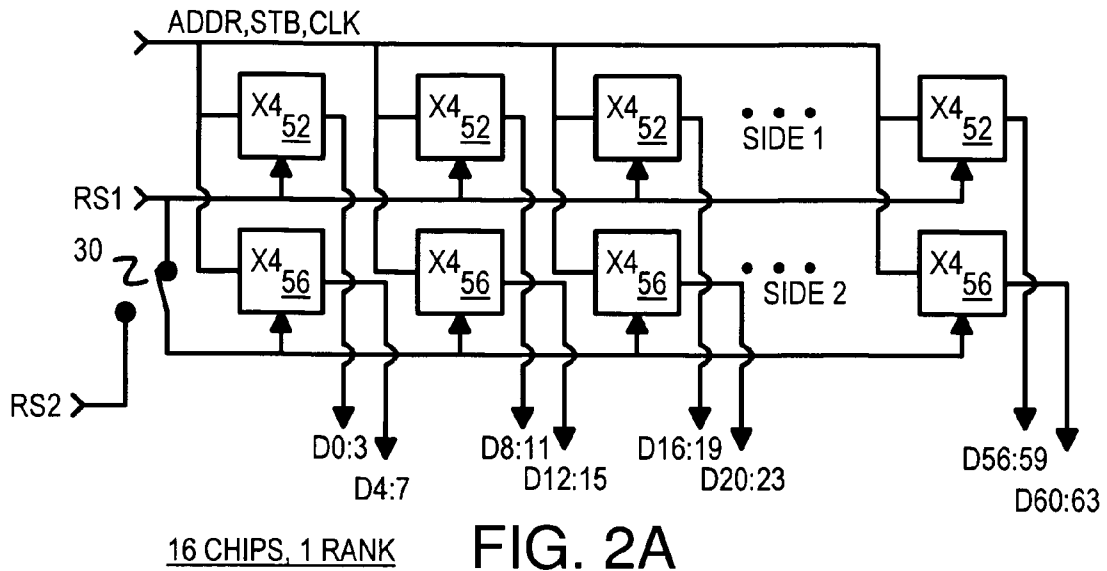


FIG. 2A

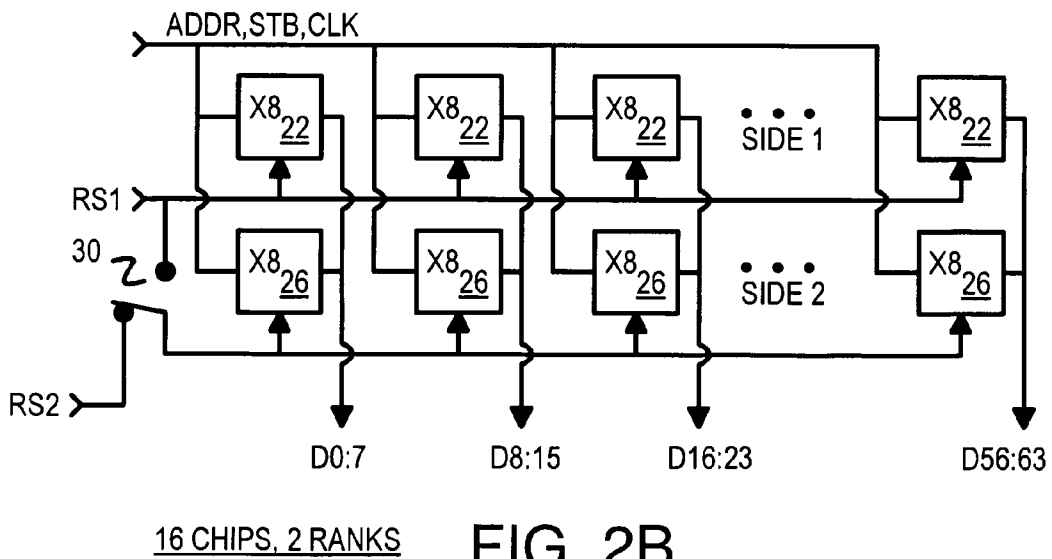


FIG. 2B

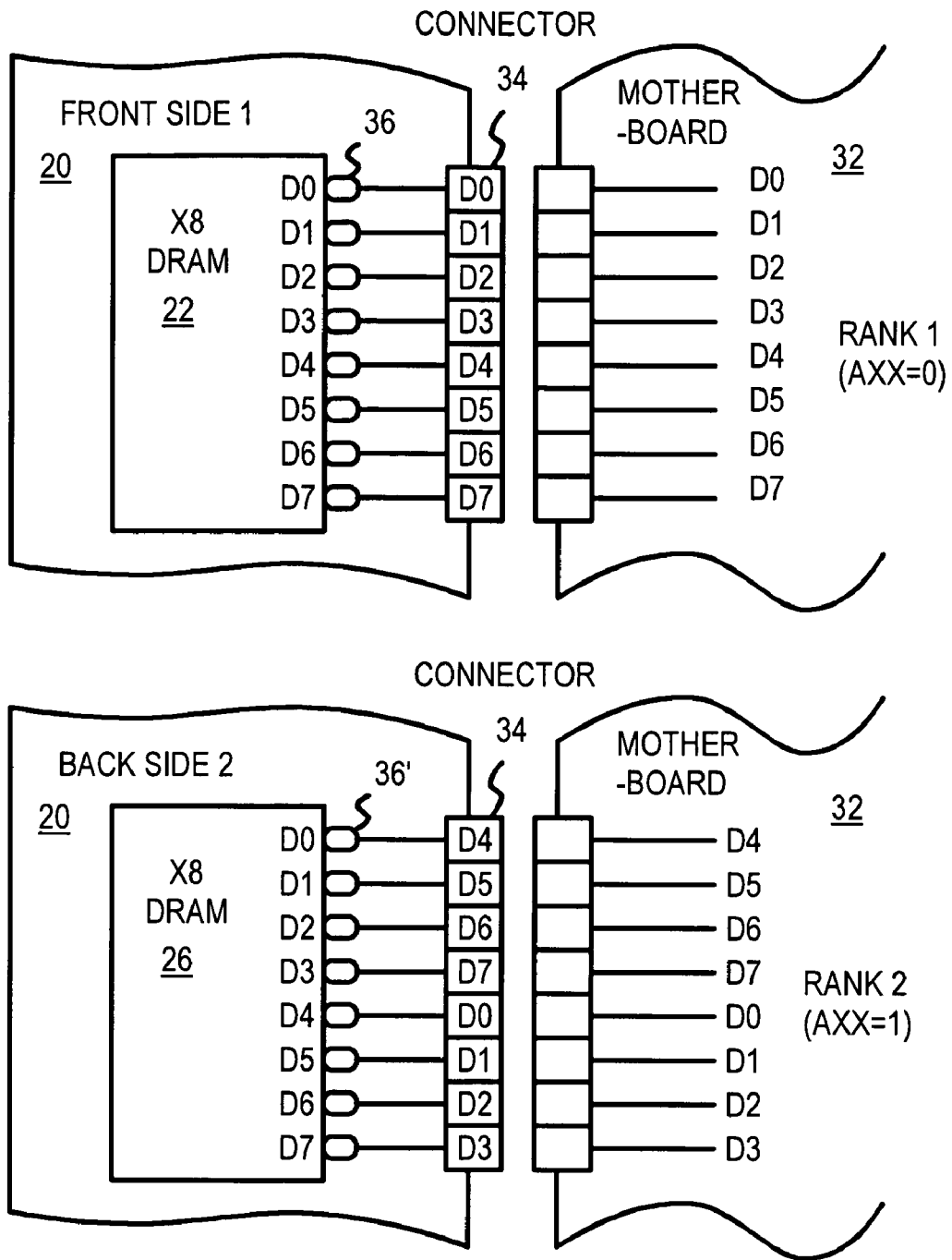


FIG. 3

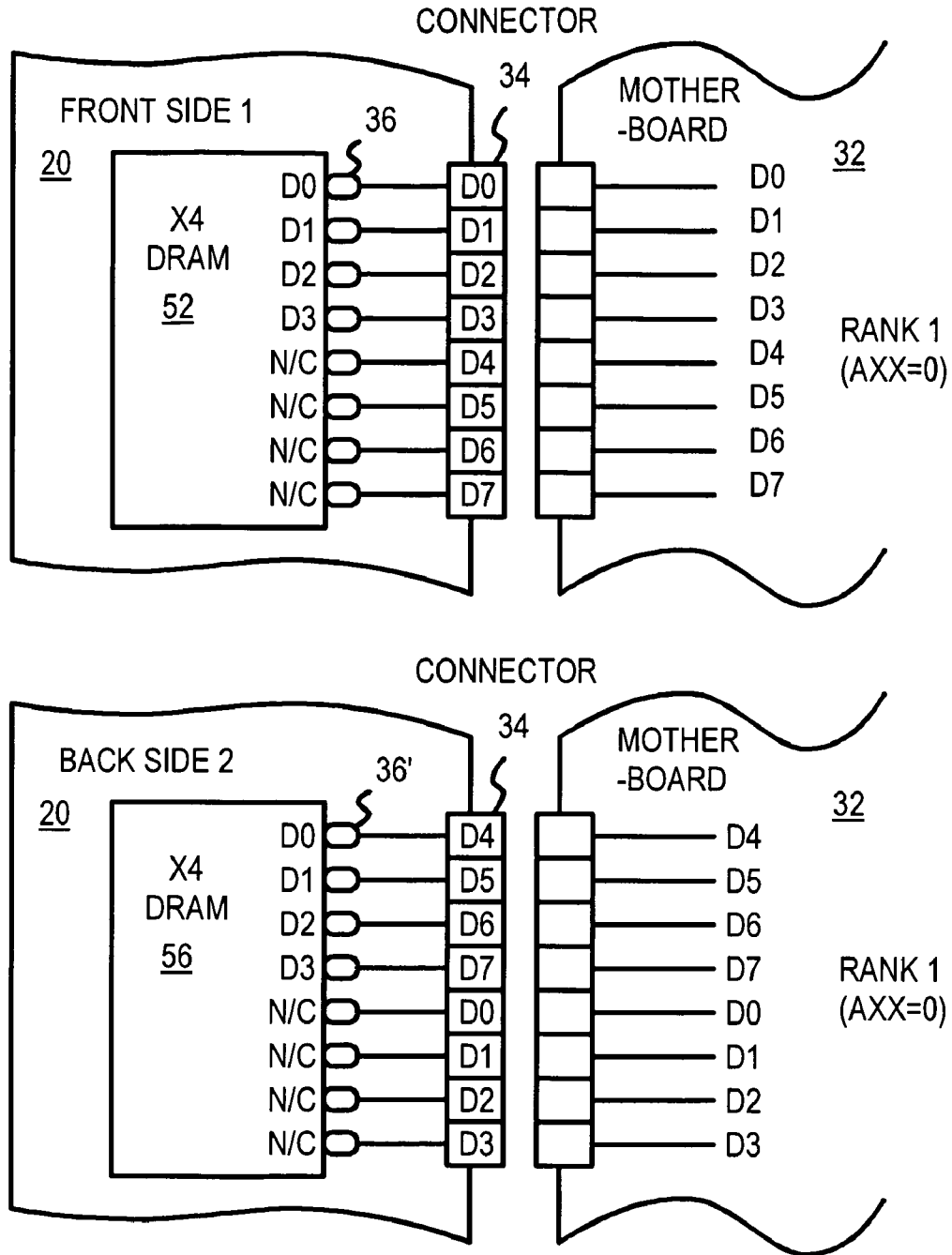


FIG. 4

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