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U1S S2121

(56) Documents Cited
GB 2130025 A EP 0398188 A2 WO 89/10593 A1
US 5272664 A US 5064378 A

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INT CL^6 G11C 5/00 5/06 , H05K 7/00 7/02 7/06 7/10 10/00
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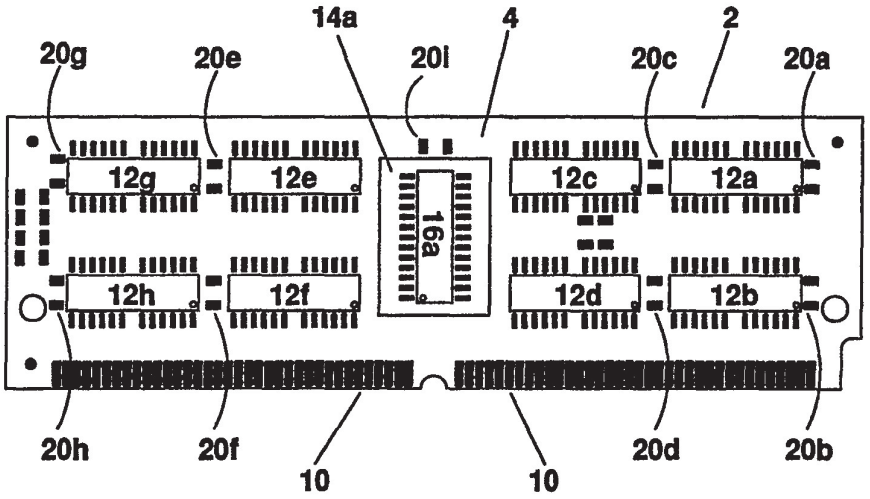
(54) Memory module

(57) A memory module (2) has a substrate (4), memory devices (12a - 12h) and means (10) for coupling the module to a module receptacle, sockets (14a) are provided on one or both faces of the module for coupling additional memory devices (16a) whereby at least one memory device (16a) can be added to the memory module (2).

Fig 1



At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

This print takes account of replacement documents submitted after the date of filing to enable the application to comply with the formal requirements of the Patents Rules 1990.

Fig 1

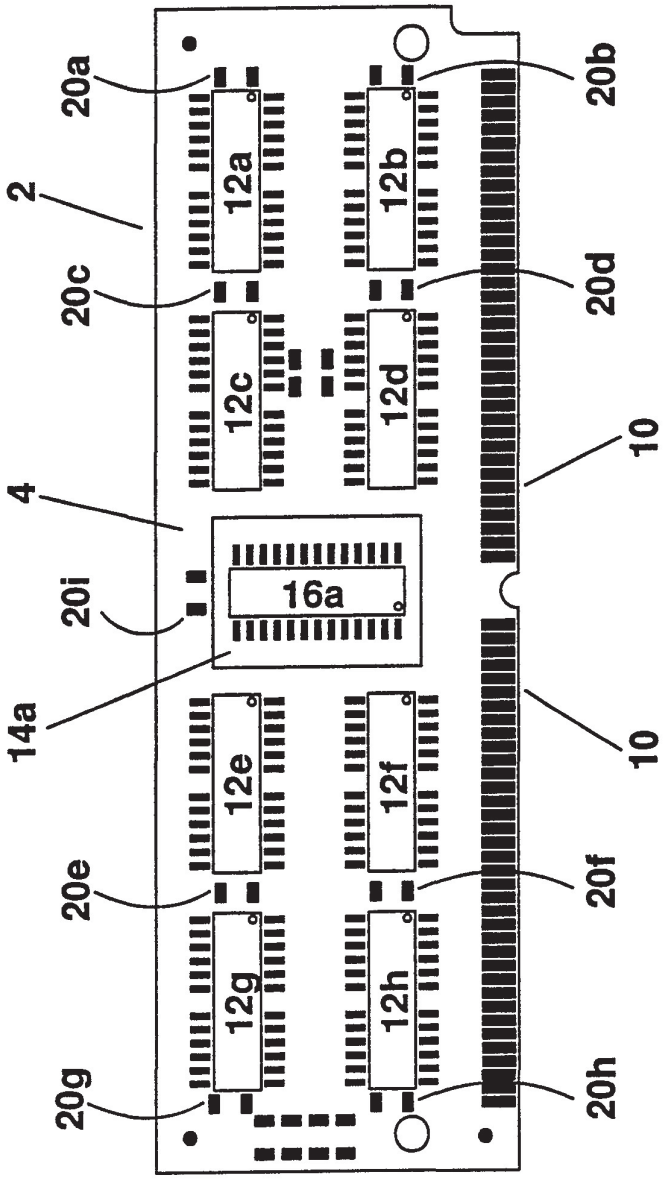

20a
20b
2
12a
12b
20c
20d
12c
12d
10
4
16a
20i
14a
12e
12f
10
20e
20f
12g
12h
20g
20h

Fig 2

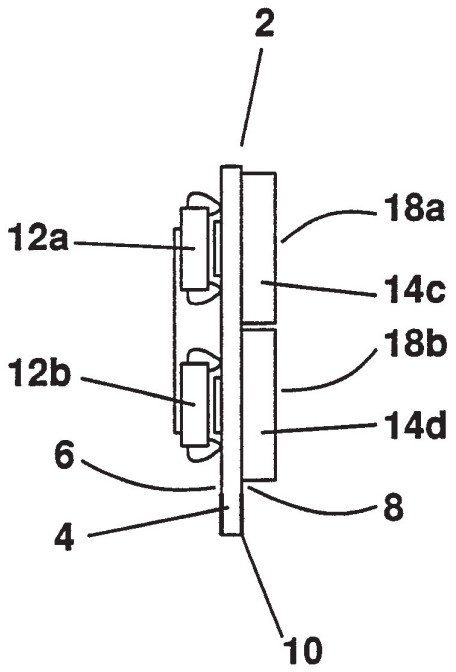
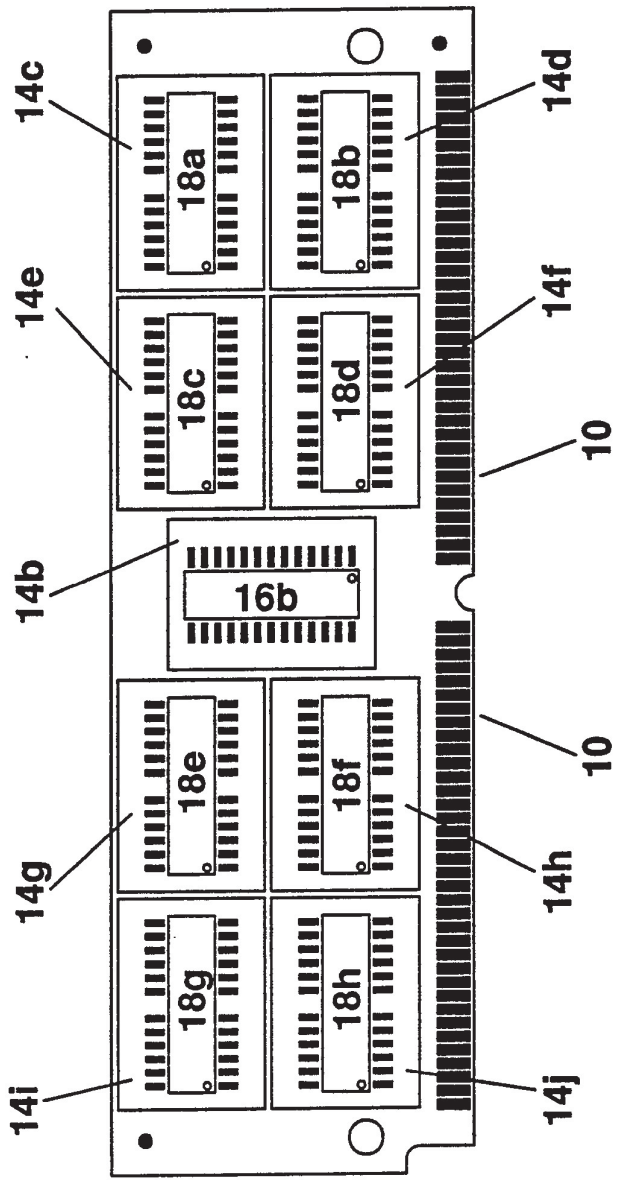


Fig 3


14c
14d
14e
14f
10
14b
16b
10
14g
14h
14i
14j
18a
18b
18c
18d
18e
18f
18g
18h

MEMORY MODULE

Field of Invention

The present invention relates to memory modules in the field of computers and their hardware memory.

Background to the Invention

Traditionally the memory of a computer system has been designed using individual memory devices mounted on a PCB (Printed Circuit Board) arranged in such a way as to give the required storage size and configuration. This circuit board either was part of the main PCB of the computer, or was designed specifically to connect with it. For many years during the design and manufacture of a computer, the memory had specifically to be tailored for that design.

Distinct memory modules comprising a number of standard parts and other passive components on a small PCB which can be connected to the main PCB are known. The first such module was the single in line memory module or SIMM, see also EP O 135 821 the content of which is incorporated herein by reference. The main benefits of this SIMM are four fold:

Firstly, the design of the computer is much simplified as a pre-wired module can be used without having to go back to first principles to work out the connections between each individual memory device. Secondly, the modules can be mounted vertically so the size of the circuit board can be reduced. Thirdly, the assembly cost of a computer can be reduced as a module containing 'n' devices requires one assembly operation compared with 'n' operations for

individual components. Lastly, as the memory existed on separate boards, there is a certain degree of flexibility in fitting modules to the computer in addition to those (if any) fitted by the manufacturer.

This has given the customer the ability to upgrade the computer's memory by replacing the existing modules with new ones of higher capacity as they become available.

Since the introduction of the "30 Pin SIMM" several variations of the basic design have been implemented by others to provide different organisations of memory with a standardised connection specification so that modules of the same type from one vendor can be freely interchanged with those from another.

Known memory modules consist of a PCB containing a plurality of memory devices and associated decoupling components wired to a connector for coupling to the computer system. Several connection systems are used, but can, for convenience, be divided into two types. First, pins attached to the edge of the module can be used, which are either soldered directly to the circuit board or plugged into sockets. Secondly, a strip of conductive tabs near the edge of the module can be arranged as an edge connector to be plugged into a receptacle on the circuit board which makes electrical connection with the tabs. The tabs can either be on one side of the module or on both; with opposing tabs independent or connected together.

A memory device is designed to store binary data written to it and maintain the information until it is changed. Unfortunately, the data can sometimes accidentally be changed by external influences such as electrical

interference, cosmic rays and other high energy particles such as radiation, or just through device failure. To guard against corruption of data, as well as providing the memory to store the information for the processor of the computer, extra auxiliary devices can be included on a module to provide for extra data integrity as either error detection or error correction.

The most common form of error detection is "parity". Traditionally, this is a system whereby an extra parity bit is assigned to every group of eight data bits of memory whose stored value is dependant upon the value of the eight data bits. On subsequent reading of data from a particular memory location, if the parity bit does not tally with its stored data then a memory error has occurred and appropriate action can be taken. Parity has the disadvantage of only being able to detect single errors and there is no way of correcting the stored information if an error is found. Error correction overcomes this but at the expense of additional memory devices to store the correction key data and associated error detection and correction logic.

Several types of memory modules are known: 30, 72, 144 and 168 terminal modules are examples; having a range of capacities and widths of data path, and some with extra devices for parity or error correction.

The computer market being extremely competitive takes every opportunity to reduce manufacturing costs. If total data integrity is not an issue, as with commercial mass produced computers, costs can be cut by not providing parity or error correction which need extra memory devices and logic on each module. Costs can also be cut by fitting cheaper low capacity memory modules which have few

devices on them or by reducing the number of module receptacles for memory in each computer relying on the customer replacing existing fitted modules with ones of higher capacity as more memory storage is needed.

Once all of the receptacles are occupied, no matter what capacity of module is fitted there comes a time when, to increase the memory capacity of the computer, the existing modules must be discarded and new ones fitted.

For every type of module there are different module capacities, some with parity or error correction and some without. Each type of memory module, therefore has to be individually designed and manufactured, which leads to a large number of possible permutations which all have to be supported by the manufacturers and their distributors. This requires a large inventory to be held to give consistent supply of each type and if one should be unavailable, severe delays can occur before re-manufacture whilst computer production is at a standstill.

Furthermore, replacing and throwing away modules each time memory capacity is increased is both costly and wasteful of resources.

Summary of the Invention

According to the present invention, there is provided a memory module comprising a substrate having a first major face and a second major face, means for coupling the module to a module receptacle, at least one means for coupling a memory device to the first major face or the second major face of the substrate, interconnections between the at least one device coupling means and the means for coupling the module to the module receptacle,

and means for signalling a write operation to a memory device, whereby at least one memory device can be added to the memory module wherein the usable memory capacity of the memory module can be increased by discrete memory devices while maintaining a valid architecture.

A "valid architecture" is one which enables substantially the full memory capacity of the memory devices on the memory module to be accessed once the module is coupled to the module receptacle.

Suitably, the means for coupling a memory device comprises means for mounting a plurality of discrete memory devices and the means for coupling is configured whereby memory capacity of the module can be incremented by a plurality of discrete memory devices.

Clearly, the discrete memory devices may be memory chips.

Suitably, the memory module includes at least one memory device hardwired to the first or second major face of the substrate, and in which there are interconnections between the at least one memory device and the at least one device coupling means. Hardwiring can be carried out eg by soldering or using a conductive adhesive.

Suitably, the device coupling means are located on the first and second major faces.

Normally, the device coupling means will comprise both electrical and mechanical coupling means, which suitably will be sockets.

Conveniently, the device coupling means enable both memory and logic devices to be mounted.

Suitably, the logic device may include a decoding function to extend the normal addressing range of a module for any given organisation of memory device. This is beyond that normally possible with direct unmodified connection of the standard control lines from the module receptacle to the memory devices themselves.

Suitably, the logic device comprises a parity or error correction device.

Suitably, the memory or logic devices are surface mounted.

Suitably, the signalling means comprises a write contact.

Also according to the present invention there is provided a computer comprising a memory module of the type referred to above.

According to another aspect of the present invention, there is provided a method of expanding the memory capacity of a computer or numerical calculating electronic machine, which method comprises the steps of:

a) providing a memory module according to any one of the preceding paragraphs,

b) coupling the memory module to a module receptacle of the computer or numerical calculating electronic machine, and

c) coupling to the memory module at least one writable or re-writable memory device.

The capacity of the module can be increased by providing sockets on the module to take additional plug in devices. A module can be produced with a base level capacity which can then be added to by the user until all sockets are filled, so eliminating the need to completely replace an ordinary module at each stage of upgrading.

The invention allows the user to customize the module at the point of use rather than having to use a specific module configured during its manufacture. The usable memory of the apparatus to which the module is to be coupled can thereby be increased.

In effect the invention can be said to provide an in-line memory module to which individual memory devices may be added to increase the memory capacity by discrete amounts while maintaining a valid architecture.

By mounting sockets on the module during manufacture, it is possible to manufacture one type of module which can have parity or error correction devices added later if required by simply plugging the necessary components into the vacant sockets.

Although providing sockets adds to the basic module cost, this additional cost is negligible to that of discarding existing modules and replacing them with ones of higher capacity. As an example, a 16Mb module may cost as much as a whole computer, so discarding it in favour of one with twice the capacity and price (32 Mb) will in total effectively cost three times the original.

With the ability to add parity or error correction, only one type of module need be purchased and stocked to cover almost all requirements. Dependency on one specific type

of module is therefore avoided as the basic module can be modified quickly as required by plugging in extra components.

It will be appreciated that within the scope of the invention any devices extra to the minimum required to make the module function in a basic form such as the parity and (second face) memory devices could be omitted and replaced with sockets. These empty sockets could then be populated with devices as required to add back any of the omitted functions.

Brief Description of the Drawings

The invention will now be described, by way of example only, with reference to the drawings that follow; in which:

Figure 1 is an enlarged schematic front view of a memory module according to the present invention.

Figure 2 is a schematic side view of the memory module shown in Figure 1.

Figure 3 is a schematic rear view of the memory module shown in Figures 1 and 2.

Description of the Preferred Embodiments

Two specific examples of the invention will now be described:

FIRST EMBODIMENT

The first example is based on a standard 72 terminal DRAM memory module but not restricted to it as this technique can equally be applied to current 30, 144 and 168 terminal modules, and also to other types of memory.

Referring to Figures 1-3 of the drawings, there is shown a memory module 2 comprising a substrate 4 having a first major face 6 and a second major face 8. Along one long edge of the substrate 4 is a connector terminal strip 10 to which reference will be made below. Also on the substrate 4, but not visible, are electrical interconnections between the various devices mounted thereon and the connector terminal strip 10 to enable it to operate satisfactorily.

The base module 2 consists of an array of memory devices 12A-12H on the first major face 6 arranged as 4Mbits in length with a data bus width of 32 bits. Additional sockets 14A-14J are provided into which additional memory and/or logic devices may be plugged to couple them to the device 2. Additional devices can be plugged into and subsequently removed from the sockets 14A-14J if desired. Sockets 14A and 14B are located centrally on opposite sides of the module 2. Sockets 14C-14J are located opposite the memory devices 12A-12H and transverse to them on the other side of the module 2.

Each socket 14A-14H includes a write contact (not shown) for writing (or re-writing) data to the memory devices 12A-12H and which can signal the write operation to the memory device. Clearly, it could comprise any suitable type of contact or terminal.

The memory devices 12A-12H are electrically and mechanically connected to the substrate 4. The preferred way is to use a soldering process to connect terminals of each device to the electrically conducting interconnections of the substrate. In addition to the memory devices 12A-12H, the sockets 14A-14J to take additional devices are also attached to the substrate 4. These extra devices are memory devices, but could also be other devices to perform error detection and correction or other logic functions. The quantity, position and type are dependant upon the design preference of the module designer and the organisation of module chosen.

In this case, the module 2 can be upgraded by populating the empty sockets 14A-14B to provide parity memory devices 16A, 16B (one parity information bit for every eight data bits to give a data bus width of 36 bits) and increasing the memory capacity from 4Mbits to 8Mbits in length by plugging into sockets 14C-14J memory devices 18A-18H.

For a module 2 to conform to the full 72 terminal module standard, there must be a collection of electrical power, data and control signals wired from each memory device 12A-12H, 16A, 16B and 18A-18H on the module 2 to the connection terminals 10 of the module 2 so that the signals are presented in the correct order and position for the module receptacle (not shown). Such a wiring configuration can easily be designed by a person skilled in the art. By way of example, a configuration will now be described.

The organisation of a fully expanded module will now be described ie with all of the extra parity memory 16 and memory 18 devices present.

The data lines are grouped into four groups of eight binary digits called bytes and have a parity bit (P0, P1, P2 and P3) associated with each byte. Address lines are connected in parallel to each memory device. Control lines CAS0-3 (Column Address Strobe) are used to simultaneously or individually activate the memory devices for each of the four data bytes. RAS0-3 (Row Address Strobes) are used to select banks of memory with RAS0 and 2 normally activating the devices on one face and RAS1 and 3 for the devices on the other face. One or more parity memory devices to store the parity information are normally situated about the centre of the module on both faces.

There is however a move in the industry towards 'Multi-Bit' memories such as the use of Byte-wide, Word-wide (16bit) and Double-word-wide (32bit). Some multi-bit memory devices can have parity options built in. This obviously eliminates the need for separate parity memory devices so freeing up more substrate area to mount additional sockets to expand the module capacity further. The increase of module capacity is not limited to only double from its unexpanded form (ie with no sockets filled), but with the addition of appropriate decoding logic the capacity is limited only by the physical ability to fit sockets or directly mounted memory devices onto a module of given size. There is a possible limitation imposed by the organisation as it is usual, but not mandatory to have symmetrical contiguous addressing of the memory.

It should be noted that the electrical loading generated by such a multiple chip memory module may exceed the recommended drive capability of most computer systems. It may, therefore, be necessary to integrate additional logic

onto the module to provide buffering means to relieve this load as proposed by Advanced Micro Devices Inc in generally available publication 15148 issued in August 1991.

For this example of the present invention a socket to take surface mount devices is to be used. This type of package currently accounts for 95% of world production.

Power is supplied to each memory device 12A-12H, 16A, 16B and 18A-18H with a quantity of capacitors 20A-20I distributed around the module 2 to decouple the noise in supply to the ground reference. Power in supplied to the capacitors 20A-20I from the connector 10.

SECOND EMBODIMENT

The second example, which is not illustrated, is based on the popular 30 terminal 'Byte-wide' module which has one byte of memory arranged on one face of a substrate fabricated from either one memory device per data bit or in a departure from the original design by using two nibble (half byte) wide devices or one byte-wide device.

In this embodiment of the present invention a socket is mounted on the substrate to provide for an auxiliary parity or error correction device should this be needed in a particular application. The other face of the substrate contains sockets to allow the memory capacity of the module to be increased. One version of this module would allow the capacity to be doubled by dividing the module into two banks: the first, with memory fitted as standard controlled by one RAS signal, and the second face containing sockets to take additional memory are controlled by a second RAS signal. Auxiliary devices are

fitted to their respective sockets to provide parity or error correction. As for the previous example, if space permits, the increase in capacity is not limited to double that of the base module. Generally the two embodiments are otherwise similar.

It will be appreciated by those skilled in the art that various modifications, alterations and substitutions may be made within the scope of the present invention. For instance, the sockets 14A-14J may be mounted on either one or both sides of the substrate 4. Further, memory devices 12 may be mounted on both sides of the module 2.

The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

CLAIMS

1 A memory module comprising a substrate having a first major face and a second major face, means for coupling the module to a module receptacle, at least one means for coupling a memory device to the first major face or the second major face of the substrate, interconnections between the at least one device coupling means and the means for coupling the module to the module receptacle, and means for signalling a write operation to a memory device, whereby at least one memory device can be added to the memory module wherein the usable memory capacity of the memory module can be increased by discrete memory devices while maintaining a valid architecture.

2 A memory module according to Claim 1, in which the means for coupling a memory device comprises means for mounting a plurality of discrete memory devices and the means for coupling is configured whereby memory capacity of the module can be incremented by a plurality of discrete memory devices.

3 A memory module according to Claim 1 or Claim 2, in which there is at least one memory device hardwired to the first or second major face of the substrate, and in which there are interconnections between the at least one memory device and the at least one device coupling means.

4 A memory module according to any preceding Claim, in which device coupling means are located on the first and second major faces.

A memory module according to any preceding Claim, in which the device coupling means comprise electrical and mechanical coupling means.

A memory module according to Claim 5, in which the device coupling means comprise sockets.

A memory module according to any preceding Claim, in which the device coupling means enable both memory and logic devices to be mounted.

A memory module according to Claim 7, in which the logic device includes a decoding function to extend the normal addressing range of a module for any given organisation of memory device.

A memory module according to Claim 7 or Claim 8, in which the logic device comprises a parity or error correction device.

A memory module according to any preceding Claim, in which the memory or logic devices are surface mounted.

11. A memory module according to any preceding Claim, in which the signalling means comprises a write contact.

A computer or numerical calculating electronics means comprising a memory module according to any preceding Claim.

A method of expanding the memory capacity of a computer or numerical calculating electronic machine, which method comprises the steps of:

a) providing a memory module according to any one of claims 1-11,

b) coupling the memory module to a module receptacle of the computer or numerical calculating electronic machine, and

c) coupling to the memory module at least one writable or re-writable memory device.

14 A memory module substantially as described herein, with reference to and, for the first embodiment only, as shown in the accompanying drawings.

15 A computer or numerical calculating electronic machine comprising a memory module according to Claim 14.

16 A method of expanding the memory capacity of a computer or electronic calculating numerical machine, substantially as described herein.

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Patents Act 1977
Examiner's report to the Comptroller under Section 17
(Search report)

Application number
GB 9510176.2

Relevant Technical Fields

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(ii) Int Cl (Ed.6) G11C 5/00, 5/06: H05K 7/00, 7/02, 7/06, 7/10, 10/00

Search Examiner
J DONALDSON

Date of completion of Search
23 JUNE 1995

Databases (see below)
(i) UK Patent Office collections of GB, EP, WO and US patent specifications.

(ii) ONLINE: WPI

Documents considered relevant following a search in respect of Claims :-
1 TO 16

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages		Relevant to claim(s)
X	GB 2130025 A	(CONTROL DATA) see page 1, line 99 - page 2, line 119	1-13
X	EP 0398188 A2	(COMPAQ) see column 3, line 56 - column 4, line 48, column 5, lines 1-58	1-13
X	WO 89/10593 A1	(FANUC) see Abstract	1-3, 5-13
X	US 5272664	(ALEXANDER) see column 4, lines 31-49, column 21, line 65 - column 22, line 28	1-13
X	US 5064378	(OLSON) see column 3, line 38 - column 4, line 32	1-3, 5-13

Databases: The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).