Significance of JEDEC DIMM Module

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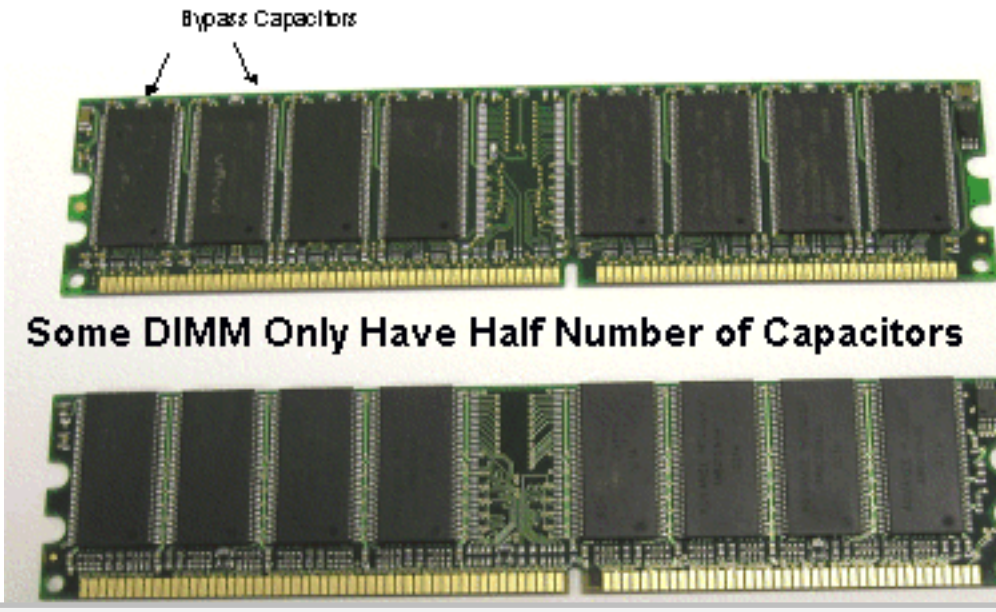
Abstract

Non-JEDEC compliance memory modules have been flooding the market resulti
computer systems and confusion. System integrators and consumer are easily te
short-term cost saving without knowing its long-term consequence. This article in
design process in JEDEC Raw cards. It highlights the details on proper memory
Whether it is clock net, stub length, termination resistor, or impedance control, th
thousands of hours of simulation and engineering. The resulting Gerbers are offe
to you. It might make you think differently next time you pick up a memory modu

General

We are seeing DIMM modules with only half of the number of bypass capacitors
modules with screened on resistors with value vary 30% across the same board.
modules made out of 4 layer printed circuit boards instead of 6 layer boards. We
module that has the correct circuitry but fail to work in the computer system. We
memory module manufacturers cut all corners to reduce cost and to gain sales.
we are frustrated at the many memory modules that do not work properly in our
That is when JEDEC, the semiconductor standard setting committee, gets into th
standard on memory modules is needed to make sure every memory module wo
computer. With a unified standard, we can therefore, enjoy the benefit of state-of
same time attending the lowest price.



Some DIMM Only Have Half Number of Capacitors

Why is JEDEC Important?

JEDEC is an organization made up of 300 plus member companies from all over consist of memory vendor companies like Micron, Samsung, Infineon, Hynix and module manufacturers like Kingston, Smart Modular, and Wintec. Connector ma Molex, and Foxconn. Memory user companies like Sun Micro, Silicon Graphics, companies like Tektronix, Agilent and CST. Chipset companies like Nvidia, Via a

All these companies realize that the only way to have the best price for memory system is to promote one mainstream technology for the entire industry. Therefo companies get together 4 times a year all into one room with their difference set concentrate on formulating a standard memory that the industry can accept. The design memory devices and modules that will work reliably in the computer syste becomes the minimum requirement for the memory market. It is recognized by a manufacturers and is supported by the entire industry.

Member companies worked together on specification, simulation, prototyping, ex parameters and system validations. A guideline is set down so that all JEDEC co memories will be functionally inter-changeable with similar performances

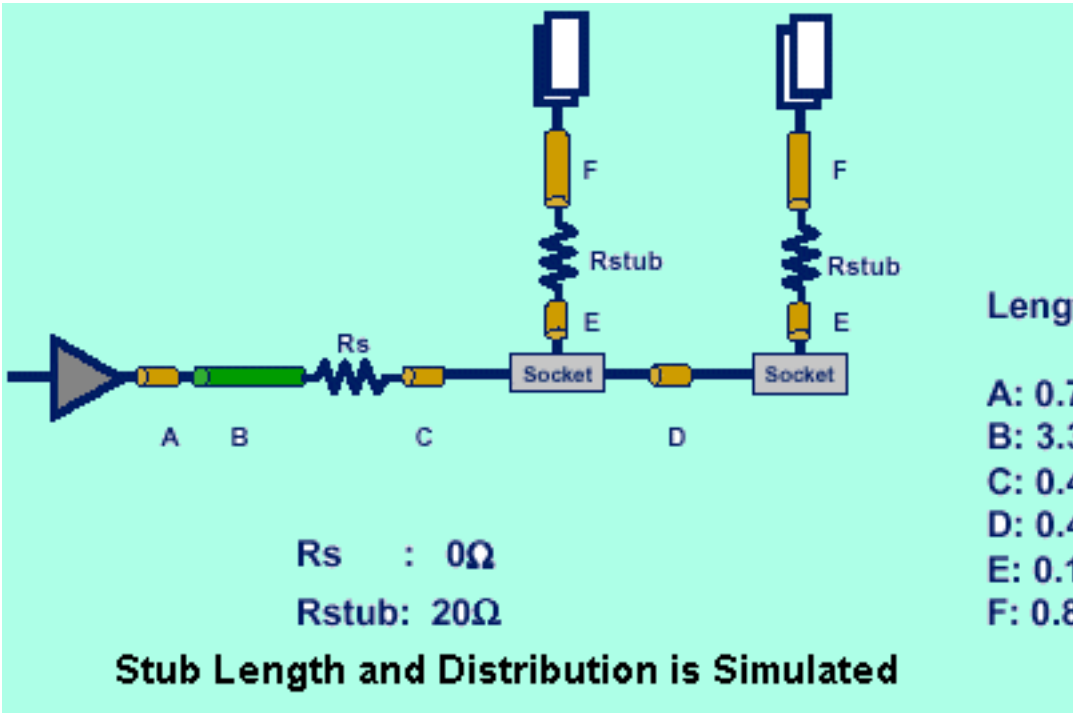
Developing a JEDEC Memory Specification

JEDEC has been looking ahead for the needs of the semiconductor memory ind of many years. It started the work on DDR memory back in 1997. Through its eff the mainstream memory in the computer industry. JEDEC has just now complete for DDR-II which should fill the market by 2005. The next task is DDR-III which is materialize by 2007

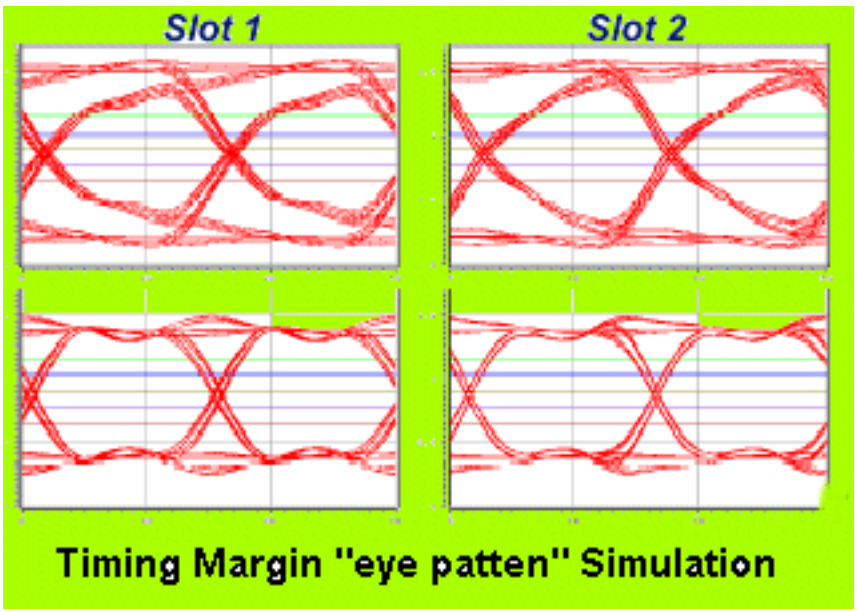
JEDEC's design procedure starts out with series of survey to users and semicon The user companies are asked what they would want while vendor companies a they can practically produced economically not now but several years down the companies have to look at the memory bandwidth required to support their appli line. Whether it is video streaming, 4G handset or fiber-to-home networking, syst have to forecast their memory requirements in speed, feature, and in density. Th vendors are asked to look at their process technology down the line. The challen before them for tighter line width technologies. Memory cores working at 2.5V po will have to go to 1.8V and 1.2V to gain the extra speed and bandwidth in a few

One of the major tasks for JEDEC is to assign pin-out for memory device and me Whether it is for the memory chip or the memory module, pin-out assignment is layouts of the motherboard and the DIMM have to be done to find the optimum re attention is applied to minimize lead inductance and to accommodate a universa different die sizes in the future. Not to mention mechanical support and reliability

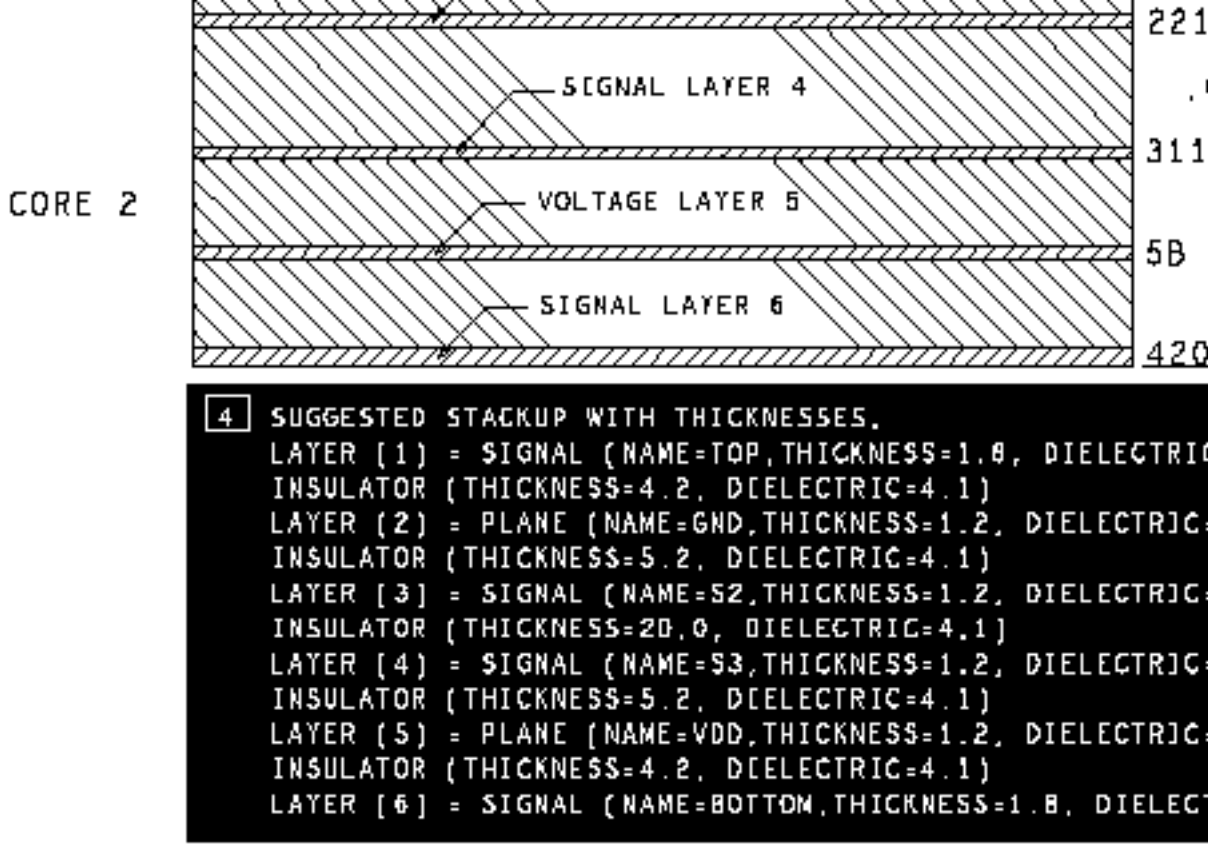
specifications.



Before the engineer has a chance to build the system, he must also figure out ho
margin his system has before hand. He takes the worst cases tolerance on hold
jittering, and a lot of other factors into the calculation and comes up with an "eye
simulation that tells how much margin the system has when incorporated with th

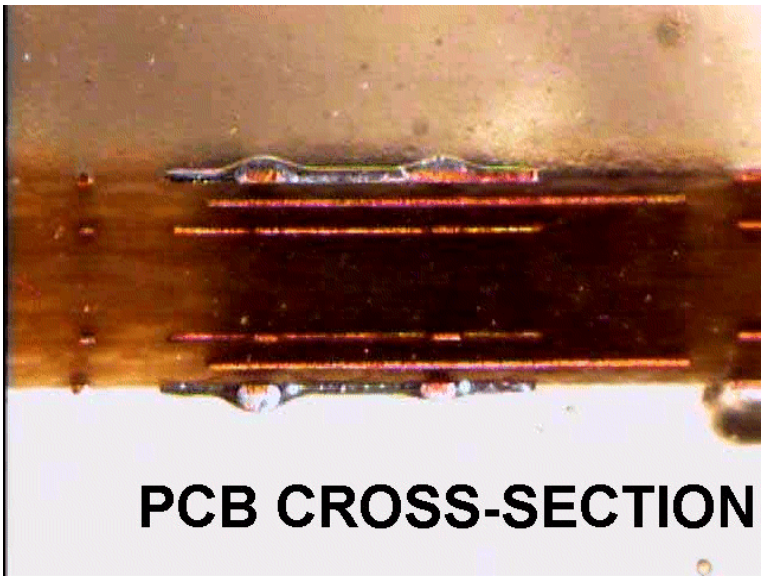


After all these simulation and calculations, the engineer might decide on one par
value for the PC board to give best performance. He has, therefore, layout his P



PCB Stack Specifications

Engineers also like to add measurement coupons (blank lines) on their PC board measurement of the actual impedance. In such case, a TDR (Termination Deper measurement is taken at the PC board manufacturing to determine the accuracy impedance. The impedance control can also be examined with a cross-section c measured under a microscope.

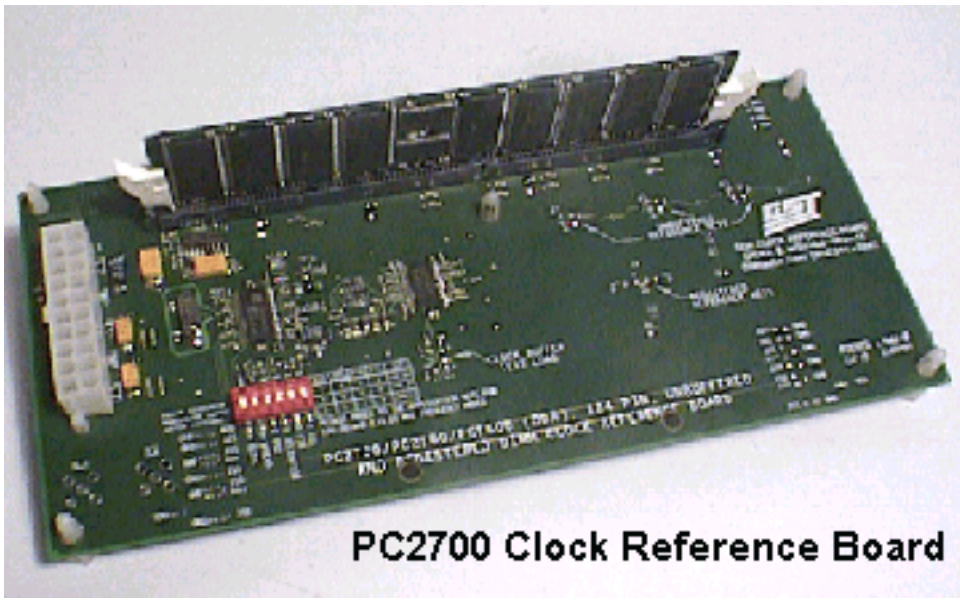


Memory Module System Validation

JEDEC members put these Raw Cards to test in different motherboards to verify in the system. The motherboard memory sockets are usually fully populated. Fur performed at 4 temperature/voltage extreme corners (low and high) to uncover a actual operational environment. Clock arrival at the memory chip is also checked delays with the help of a JEDEC Standard Clock Reference Board.

JEDEC Standard Clock Reference Board

JEDEC members have determined that if common design modules are to work w motherboard, the module clock skew is a very critical factor. Therefore, JEDEC h Clock Reference Board to be used for an industry wide uniform calibration. Many Clock Reference Boards are made over time for the different generations of mem There is the 133MHz CRB for 133Mhz SDRAM modules. There are also CRB fo DIMM as well as a new version for the PC2700 DIMM



PC2700 Clock Reference Board

The Clock Reference Board is a standard clock generator split into different cloc CRB. One path goes to a standard clock termination load while the other clock p DRAM chips. This provides the engineer with a mechanism to measure and to ca arrival
time to the chips on the module with an oscilloscope. Any unwanted skew can, th corrected by adding capacitors to the feedback of the clock PLL (phase lock loop

These CRB's are manufactured in one batch of PCB and one batch of uniform co minimize the variations. The result is the best way to unify the industry on clock a thus the assurance of modules will work in different systems.

Proper Memory Module Manufacturing, Meeting JEDEC Standard

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