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10 *Attorneys for Defendant*
Kingston Technology Company, Inc.

11
12 **UNITED STATES DISTRICT COURT**
13 **CENTRAL DISTRICT OF CALIFORNIA**
14

15 POLARIS INNOVATIONS LIMITED,
16
17 Plaintiff,

17 vs.

18 KINGSTON TECHNOLOGY COMPANY,
19 INC.,
20 Defendant.

Case No. 8:16-cv-00300-CJC-RAO

**KINGSTON TECHNOLOGY
COMPANY, INC.’S FIRST
AMENDED ANSWER,
AFFIRMATIVE DEFENSES,
AND COUNTERCLAIMS TO
PLAINTIFF’S COMPLAINT FOR
PATENT INFRINGEMENT**

21
22
23 Defendant Kingston Technology Company, Inc. (“Kingston”), by and through
24 undersigned counsel, hereby files its First Amended Answer, Affirmative Defenses,
25 and Counterclaims to Plaintiff Polaris Innovations Limited’s (“Polaris”) Complaint as
26 follows:
27
28

1 use, sale, offering for sale, and/or importation of products and methods incorporating
2 Polaris's patented inventions. Any remaining allegations of Paragraph 6 are denied.

3 7. Kingston is without knowledge or information sufficient to form a belief
4 as to the truth of the allegations of Paragraph 7 and therefore denies them.

5 8. Paragraph 8 states legal conclusions to which no response is required.
6 Kingston denies that it makes, sells, offers for sale, or imports products and methods
7 that infringe the Asserted Patents. Any remaining allegations of Paragraph 8 are
8 denied.

9 **THE ASSERTED PATENTS**

10 9. Kingston admits that what purports to be a copy of the United States
11 Patent No. 6,157,589 ("the '589 Patent") is attached to the Complaint as Exhibit 1 and
12 that the face of the '589 Patent bears the title "Dynamic semiconductor memory
13 device and method for initializing a dynamic semiconductor memory device." Any
14 remaining allegations of Paragraph 9 are denied.

15 10. Kingston is without knowledge or information sufficient to form a belief
16 as to the truth of the allegations of Paragraph 10 and therefore denies them.

17 11. Kingston admits that what purports to be a copy of the United States
18 Patent No. 6,438,057 B1 ("the '057 Patent") is attached to the Complaint as Exhibit 2
19 and that the face of the '057 Patent bears the title "DRAM refresh timing adjustment
20 device, system and method." Any remaining allegations of Paragraph 11 are denied.

21 12. Kingston is without knowledge or information sufficient to form a belief
22 as to the truth of the allegations of Paragraph 12 and therefore denies them.

23 13. Kingston admits that what purports to be a copy of the United States
24 Patent No. 6,850,414 B2 ("the '414 Patent") is attached to the Complaint as Exhibit 3
25 and that the face of the '414 Patent bears the title "Electronic printed circuit board
26 having a plurality of identically designed housing-encapsulated semiconductor
27 memories." Any remaining allegations of Paragraph 13 are denied.

1 22. Paragraph 22 states legal conclusions to which no response is required.
2 Kingston denies that it infringes, literally or under the doctrine of equivalents, the
3 '589 Patent, and denies that any alleged infringement was willful. Any remaining
4 allegations of Paragraph 22 are denied.

5 23. Kingston admits that what purports to be an image of the front and back
6 views of Kingston's SM2280S3/120G product is shown in Paragraph 23. Any
7 remaining allegations of Paragraph 23 are denied.

8 24. Kingston admits that what purports to be a front image of Kingston's
9 SM2280S3/120G product is shown in Paragraph 24. Kingston admits that the
10 purported SM2280S3 product shown in Paragraph 24 includes a dynamic random
11 access memory (DRAM) chip (labeled Nanya NT5CC128M16FP in the photo shown
12 in Paragraph 24) and a controller chip (labeled Phison PS3108 in the photo shown in
13 Paragraph 24). Kingston denies that when Kingston, its customers, and other third
14 parties turn on the products accused of infringing the '589 Patent, the controller chip
15 supplies, via an initialization circuit, a supply voltage stable signal once a supply
16 voltage has been stabilized after the switching-on operation of the dynamic
17 semiconductor memory device. Kingston denies that the identified controller chip
18 also supplies, via an enable circuit of the initialization circuit, an enable signal, the
19 initialization circuit receiving the supply voltage stable signal and further command
20 signals externally applied to the dynamic semiconductor memory device, after an
21 identification of a predetermined proper initialization sequence of the further
22 command signals, the enable signal being generated and effecting an unlatching of a
23 control circuit provided for a proper operation of the dynamic semiconductor memory
24 device. Kingston admits that Paragraph 24 alleges that a so-called Clock Enable
25 Signal ("CKE signal") supplied by the Phison controller chip to the Nanya chips is the
26 purported enable signal claimed in the '589 Patent. Kingston admits that Paragraph
27 24 also alleges that the so-called Mode Register Set ("MRS") command and/or the ZQ
28 Calibration ("ZQCL") command is the initialization sequence of the command

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