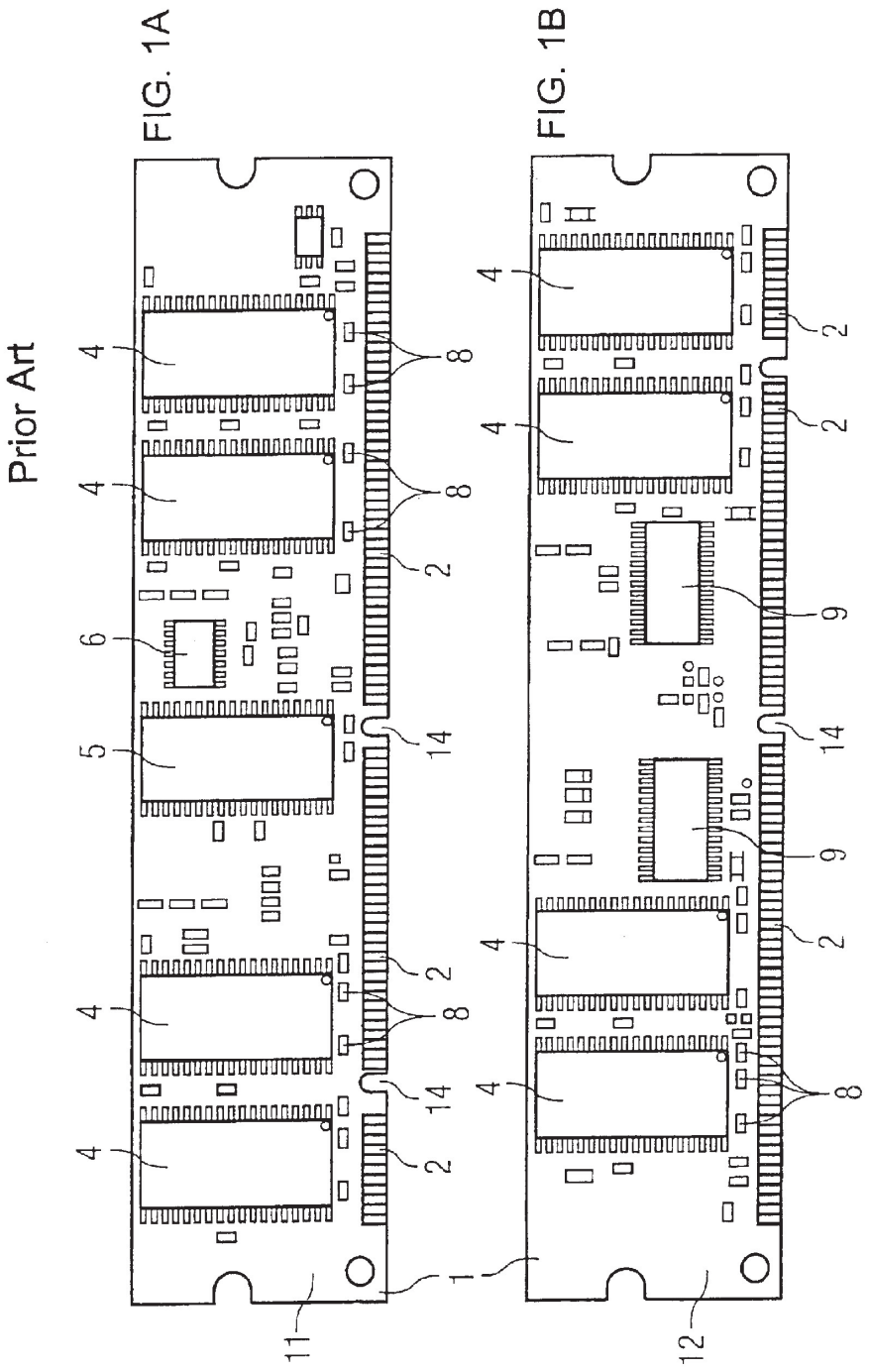
Prior Art
FIG. 1A
FIG. 1B
4
8
2
6
5
14
1
11
12
9

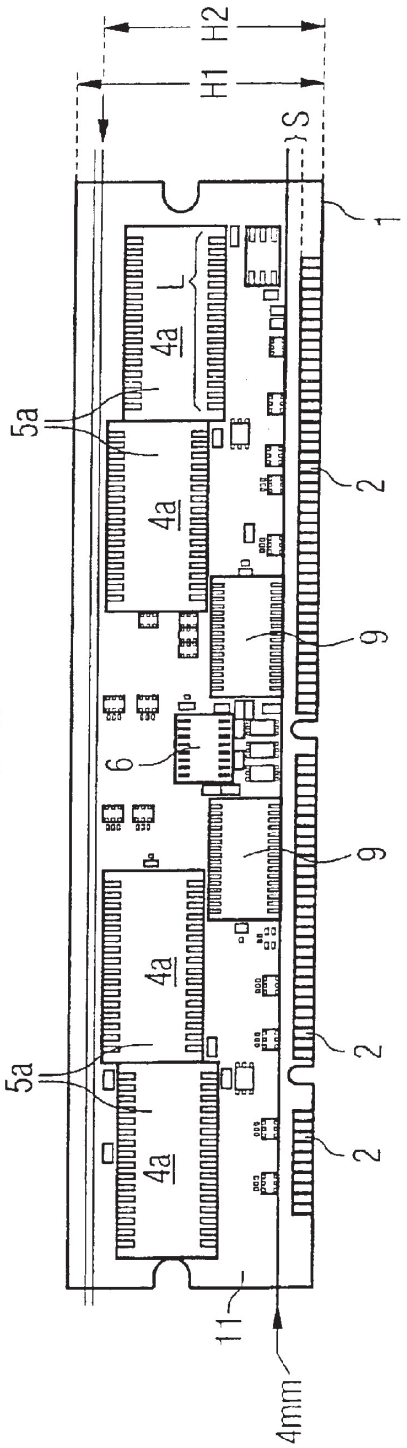

FIG 2

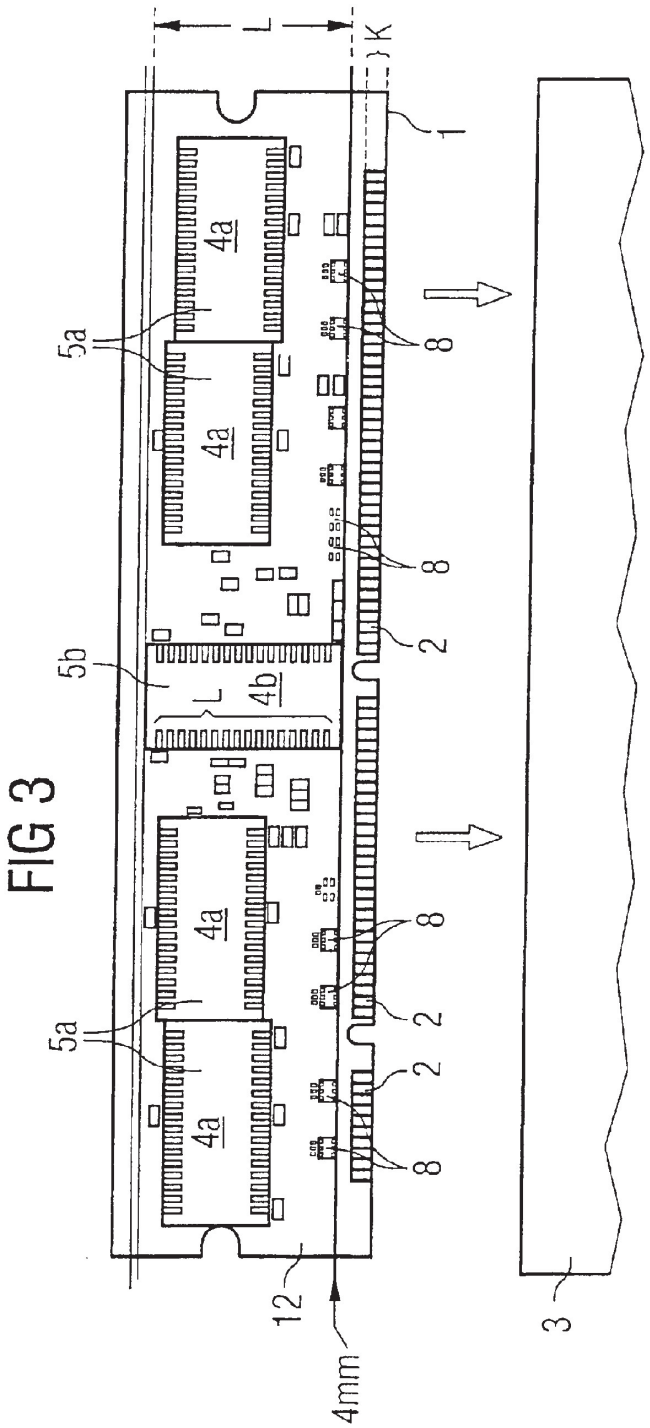

FIG 3

ELECTRONIC PRINTED CIRCUIT BOARD HAVING A PLURALITY OF IDENTICALLY DESIGNED, HOUSING-ENCAPSULATED SEMICONDUCTOR MEMORIES

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to an electronic printed circuit board, which has a memory module and a contact strip that can be inserted into another electronic unit. The memory module has at least nine identically designed integrated semiconductor memories encapsulated in identically designed rectangular housings. The housings are each individually connected to the printed circuit board. One of the semiconductor memories is connected as an error correction chip on the printed circuit board and the rectangular housing of that memory is arranged on the printed circuit board in a manner such that the longer dimension is oriented perpendicular to the contact strip.

Printed circuit boards of this type are inserted into motherboards of personal computers or network computers and serve as the main memory, for example. In network computers, the printed circuit boards are inserted into compartment-type elements having a small height, for which reason the printed circuit boards themselves should also have only a small height (the dimension perpendicular to the contact strip). Therefore, compared with their width, which is essentially determined by the length of the contact strip, insertable printed circuit boards are not very high so that the compartment-type elements can be made very flat.

The height of a printed circuit board essentially depends on the dimensions of the largest components arranged on the printed circuit board. The largest components that are arranged on a printed circuit board are generally housings for semiconductor chips containing integrated circuits. The connections of the semiconductor chips are connected by the housing to corresponding contacts on the printed circuit board that are significantly larger than the chip connections. The housings themselves are also much larger than the integrated circuits and thus concomitantly determine the minimum height of the printed circuit board. In the case of printed circuit boards which carry memory modules, the largest housings are those for semiconductor memories, for example, for SDRAMS (synchronous dynamic random access memories). The housings therefore have a rectangular form and are always arranged on the printed circuit board vertically, i.e they are oriented with their longer dimension perpendicular to the contact strip.

The reason for this arrangement is that one of the semiconductor memories is used as an error correction chip in order to perform error checking on data that will be stored in the rest of the semiconductor memories or that will be read from the memories. The error correction chip is arranged approximately in the center of the contact strip, is arranged above the contact strip, and is arranged vertically, i.e. with the longer dimension of its housing at right angles to the contact strip, because of prescribed lengths of the conductor tracks which connect the error correction chip to the contact strip.

The rest of the semiconductor memories are arranged on both sides of the error correction chip and also on the front and rear sides of the printed circuit board in the same orientation as the error correction chip, so that all of the identically designed semiconductor memories are lined up along the contact strip in a conventional arrangement. The

contact strip has electrical contacts on the front side and also on the rear side of the printed circuit board. Equally, the housing-encapsulated semiconductor memories are present both on the front side and on the rear side of the printed circuit board. Only a single error correction chip is provided and is situated, for example, on the front side of the printed circuit board.

In addition to further semiconductor chips that are encapsulated in smaller housings than the memory chips and that are arranged in proximity to the center of the contact strip, the printed circuit board has further, still smaller components, primarily passive components such as resistors and capacitors. In particular, many resistors are arranged in the outer regions of the contact strip. The resistors require a short connection to corresponding contacts of the contact strip.

By contrast, the housing-encapsulated semiconductor memories arranged in the outer regions of the contact strip are arranged at a somewhat larger distance from the contact strip, since their leads to the contact strip are permitted to be longer than the leads of the passive components to the contact strip.

The distance of all of the semiconductor memories from the contact strip is chosen in a uniform fashion, so that the vertically arranged memory housings concomitantly determine a certain minimum height of the printed circuit board. This is composed of the longer dimension of a memory housing, the height of resistors that are arranged between the housings and the contact strip, the height of the contact strip itself, and possibly a safety clearance between the contact strip and the components on the printed circuit board. This safety clearance serves, in the event of a slightly inclined attitude of the printed circuit board during insertion into motherboards, to protect the nearest components on the printed circuit board from mechanical damage, and is chosen to be as small as possible.

In the case of this conventional arrangement, in which the edges of the memory housings lined up along the contact strip are aligned, there is no more leeway for a further reduction of the circuit board height (the height of the printed circuit board perpendicular to the contact strip).

SUMMARY OF THE INVENTION

It is accordingly an object of the invention to provide an electronic printed circuit board having a memory module and a contact strip that can be inserted into another electronic unit, in which the printed circuit board overcomes the above-mentioned disadvantages of the prior art apparatus of this general type.

In particular, it is an object of the invention to reduce the height of the printed circuit board still further while using the same memory housings.

With the foregoing and other objects in view there is provided, in accordance with the invention, an electronic printed circuit board configuration including: an electronic printed circuit board having a contact strip for insertion into another electronic unit; and a memory module having at least nine identically designed integrated semiconductor memories. Each one of the semiconductor memories is encapsulated in a rectangular housing having a shorter dimension and a longer dimension. The housing of each one of the semiconductor memories is identically designed and is individually connected to the printed circuit board. One of the semiconductor memories is connected as an error correction chip. The longer dimension of the housing of the error correction chip is oriented perpendicular to the contact

strip. The longer dimension of the housing of each one of the semiconductor memories, other than the error correction chip, is oriented parallel with the contact strip.

The object of the invention is achieved by virtue of the fact that, in the case of the printed circuit board of the generic type, the housings of the identically designed semiconductor memories, other than the error correction chip, are arranged on the printed circuit board in a manner such that they are oriented with their longer dimension parallel to the contact strip.

The housings of the semiconductor memories, which are identically designed, and therefore, all have the same dimensions, are arranged on the printed circuit board with a different orientation. While the semiconductor memory that is to be connected up as the error correction chip is still arranged vertically in order to comply with the specifications for the conductor track lengths of its leads, the rest of the identically designed semiconductor memories are arranged horizontally, that is to say parallel to the contact strip. In this position, the longer dimension of the rectangular housings extend parallel to the contact strip, and each horizontally oriented semiconductor memory requires a smaller circuit board height than in the case of a vertical orientation. The semiconductor memory that is used as the error correction chip and that concomitantly determines the height of the printed circuit board still requires the same space and thus actually, moreover, the original circuit board height.

However, this semiconductor memory, and this is something that is exploited according to the invention, is the only one that can be brought still closer to the contact strip, since no resistors have to be arranged between it and the contact strip. As a result, the board height is reduced by the distance that is taken up by the resistors that are arranged between the memory housings and the contact strip. Although these resistors are present over the outer regions of the contact strip on the printed circuit board, the semiconductor memories that are arranged horizontally overall lie closer to the contact strip, since they are narrower horizontally. The semiconductor memory used as the error correction chip can be brought up to the contact strip by the distance that is required by the resistors arranged in the outer regions of the contact strip.

This results in a certain, albeit small, narrowing of the printed circuit board. In many cases, however, this suffices to actually enable the incorporation into network computers.

A preferred embodiment provides for the semiconductor memories to be arranged such that the housing of the error correction chip extends, as seen from the contact strip, through to a greater distance from the contact strip than the housings of the other identically designed semiconductor memories. In this case, the horizontally oriented semiconductor memories are brought so close to the resistors at the contact strip that they do not require the printed circuit board to have a larger height than that required by the error correction chip that is brought up to the contact strip. This exploits the maximum space saving that can be obtained by using the invention.

Accordingly, in a preferred embodiment, the printed circuit board has a height that is perpendicular to the contact strip and that is composed of the sum of the longer dimension of a rectangular housing, the length of a contact of the contact strip and a safety clearance between the error correction chip and the contact strip of less than 2 mm. Accordingly, the error correction chip is brought up to the contact strip in a manner that leaves a slight safety clearance. The safety clearance serves for, in the event that the printed circuit board is placed in an inclined position during the insertion or withdrawal from a motherboard, for example, avoiding damage to the housing of the error correction chip (or further modules arranged in the same proximity to the contact strip). It goes without saying that the safety clearance can be reduced to the amount that is still just required.

The printed circuit board preferably has a height of 1 to 1.2 inches perpendicular to the contact strip. The height of a printed circuit board is the length of the edge of the printed circuit board—considered from the direction of the printed circuit board area—which extends perpendicularly to the contact strip. By contrast, the length of the edge parallel to which the contact strip runs is called the board width. The board height is generally quite smaller than the board width. The dimension of the printed circuit board perpendicular to its surface is referred to, not as the height of the printed circuit board, but rather as the printed circuit board thickness.

The housings of the identically designed semiconductor memories are preferably TSOP housings (thin small outline packages). These are standardized housings of predetermined dimensions (thin small outline package). Using the present invention, the height of the printed circuit board can be further reduced even when these housings continue to be used.

In a further preferred embodiment, the memory module has nine identically designed semiconductor memories. This embodiment allows high utilization of the printed circuit board area in the case of a symmetrical arrangement when two identically designed semiconductor memories are configured on each side of the error correction chip on both the front side and also on the rear side of the printed circuit board.

In a preferred embodiment, the printed circuit board is configured according to the standard of the PC 133 SDRAM registered DIMM design specification, raw card A or raw card F. This standard relates to the type of interconnection of the individual components of the memory module and the individual contacts of the contact strip. This standard defines length specifications of about 800 conductor tracks that are laid on the printed circuit board, except for permissible length tolerances. This standard furthermore contains specifications concerning the thickness of conductor tracks, concerning the approximate course of conductor tracks and also the time windows for the temporal sequence of signal transmissions. The raw cards A and F, special standard groups within the PC 133 SDRAM registered DIMM design specification, are defined for printed circuit boards that already have a very small height anyway. Using the present invention, even printed circuit boards that are configured according to these standard groups can be narrowed further.

Finally, the printed circuit board has a width of 5.25 inches. This board width has gained acceptance in the case of memory module boards.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in an electronic printed circuit board having a plurality of identically designed, housing-encapsulated semiconductor memories, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and

advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1**A shows the front side of a conventional printed circuit board;

FIG. **1**B shows the rear side of the conventional printed circuit board;

FIG. **2** shows the front side of an inventive printed circuit board; and

FIG. **3** shows the rear side of the printed circuit board shown in FIG. **2**.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the figures of the drawing in detail and first, particularly, to FIG. **1**A thereof, there is shown a plan view of the front side **11** of a conventional printed circuit board **1** having, at its lower edge, a contact strip **2** interrupted by two indentations **14**. If the printed circuit board is rotated about a vertical axis extending through the right-hand indentation **14**, then the rear side **12** of the printed circuit board becomes visible. The rear side is illustrated in FIG. **1**B. The front side **11** and the rear side **12** overlap in a mirror-inverted fashion, so that the left-hand half of the front side **11** corresponds to the right-hand half of the rear side **12**.

The printed circuit board **1** has a number of memory chips **4** on both printed circuit board areas **11**, **12** and also has a further identically designed chip, which is used as an error correction chip **5**. Furthermore, further semiconductor modules are present, for example two register chips **9**, with which memory addresses in the memory chips **4** are amplified synchronously, and a clock synchronization chip **6**—also called PLL (phase locked loop)—for matching the memory module to an external clock frequency. Each of these semiconductor modules is encapsulated in a housing that connects the connections of the semiconductor module to significantly larger contacts of the printed circuit board. The dimensions of the housings are standardized, in which case, of all the semiconductor modules **4**, **5**, **6** arranged on the printed circuit board, the memory modules **4**, **5** have the largest housings. For this reason, the size of their housings is determinative of the required height of the printed circuit board. In FIG. **1**, the housings for the respective semiconductor modules **4**, **5**, **6** are designated by the reference symbols of the semiconductor modules themselves, since the housings determine their space requirement on the printed circuit board.

On the conventional printed circuit board **1** illustrated in FIG. **1**, all of the semiconductor memories **4** are arranged on the printed circuit board vertically, i.e. such that the longer dimension of their rectangular housings is oriented perpendicular to the extent of the contact strip **2**. The semiconductor memories are thus lined up parallel to one another on the front side and the rear side of the printed circuit board along the extent of the contact strip **2**. In this arrangement, the smaller edges of the housings of the semiconductor memories **4** and **5** are aligned, i.e. all the memory modules **4**, **5** are arranged in a line. They are all situated at the same distance from the contact strip **2**. This distance is predetermined by the width of the resistors **8** that are arranged in between the contact strip **2** and the memory modules **4**, **5** and by the mechanically dictated or thermally dictated safety clearances on both sides of the resistors **8**. In each case, two of these resistors **8** must be arranged between one semiconductor memory **4** and the contact strip **2**, because the upper limit for the length of the leads of the resistors from the contact strip **2** permits no other arrangement.

The contact strip **2**, the resistors **8**, the larger dimension of the housings of the semiconductor memories **4**, **5** and also certain safety clearances between these together produce the required board height of this conventionally configured printed circuit board.

FIG. **2** shows the front side **11** of an inventive printed circuit board. FIG. **3** shows the rear side **12** of the printed circuit board and diagrammatically shows, an electronic unit **3**, for example a motherboard, into which the contact strip **2** of the printed circuit board **1** can be inserted.

FIGS. **2** and **3** show the front side **11** and the rear side **12** of a printed circuit board **1** configured according to the invention. The identically designed semiconductor memories are designated by **4***a*, **4***b* and their likewise identically designed housings are designated by **5***a*, **5***b*.

On the printed circuit board that is populated according to the invention, as shown by FIGS. **2** and **3**, the housings **5***a* of those semiconductor memories **4***a* which are not connected up as the error correction chip are arranged horizontally on the printed circuit board **1**, i.e. the respective longer dimension L of the rectangular housings **5***a* runs parallel to the extent of the contact strip **2**. Only the housing **5***b* of the error correction chip **4***b* is arranged vertically and takes up the same printed circuit board height as on a conventional printed circuit board. However, the housing of the error correction chip is brought up to the contact strip **2** as close as possible. This is possible because, between the error correction chip or its housing **5***b* and the contact strip **2**, there is no need to arrange any passive components. In particular, there is no need for any resistors **8**, as in the case of all of the other identically designed semiconductor memories **4***a* that are configured horizontally. By contrast, these semiconductor memories **4***a* take up for themselves a significantly smaller printed circuit board height than when in the vertical orientation, so that the actual printed circuit board height is determined only by the error correction chip **4***b* that is brought up to the contact strip **2**.

As a result, the height of the printed circuit board can be reduced from a value H_1 to a smaller value H_2 composed of the longer dimension L of the identically-designed housings **5***b*, the length K of the contacts of the contact strip **2** (in the direction of the double arrow to L), and a safety clearance S between the contacts of the contact strip and the resistors **8**. This reduction of the printed circuit board height enables incorporation into even flatter elements of e.g. network computers.

The printed circuit board illustrated in FIGS. **2** and **3** is populated in such a way that it can be connected up in accordance with the raw card A or raw card F of the standard "PC 133 SDRAM registered DIMM design specification" (133 MHz; dual inline memory module). It has a height of between 1 and 1.2 inches between the lower edge, at which the contact strip **2** is situated, and the upper edge.

The remainder of the components illustrated and their functions correspond to the prior art. The memory modules **4***a*, **4***b* are SDRAMs (synchronous dynamic random access memory modules). They are encapsulated in TSOP housings (thin small outline package) **5***a*, **5***b*.

The clock synchronization chip **6** (PLL; phase locked loop) ensures that, after a few clock cycles of the clock signal that is output from the electronic unit **3** via the contact strip **2** to the memory modules of the printed circuit board **1**, the latter can operate synchronously with the motherboard.

Data that is transported to the semiconductor memory modules **4***a* always contain check data. The error correction chip, namely memory module, **4***b* checks the correctness of the data before the data are passed on.

A wide variety of methods are known according to which the error correction chip, namely memory module, **4***b* can operate. An example that shall be mentioned here is the ECC method (error correcting code), in which a check bit is added to eight bits of data to be communicated.

FIG. **2** furthermore shows two register chips **9**, with which the memory addresses in the memory chips **4** are amplified synchronously.

All of the components situated on the printed circuit board are connected to one another and to the contact strip by conductor tracks. At the present time, printed circuit boards usually have six different conductor track planes lying one above the other in which the conductor tracks are arranged. The course of the conductor tracks is configured according to a suitable raw card of the above standard. The conductor tracks are not illustrated in the figures since their specific course is not essential with regard to the present invention.

We claim:

1. An electronic printed circuit board configuration, comprising:

an electronic printed circuit board having a contact strip for insertion into another electronic unit; and

a memory module having at least nine identically designed integrated semiconductor memories;

each one of said semiconductor memories being encapsulated in a rectangular housing having a shorter dimension and a longer dimension;

said housing of each one of said semiconductor memories being identically designed and being individually connected to said printed circuit board;

one of said semiconductor memories being connected as an error correction chip;

said longer dimension of said housing of said error correction chip being oriented perpendicular to said contact strip; and

said longer dimension of said housing of each one of said semiconductor memories, other than said error correction chip, being oriented parallel with said contact strip.

2. The printed circuit board according to claim **1**, wherein:

said housing of said error correction chip extends a greater distance away from said contact strip than said housing of each one of said semiconductor memories, other than said error correction chip.

3. The printed circuit board according to claim **1**, wherein:

said contact strip has a contact with a length;

said printed circuit board has a height extending perpendicular to said contact strip; and

said height of said printed circuit board is equal to a sum of said longer dimension of said housing of said error correction chip, said length of said contact of said contact strip and a safety clearance between said error correction chip and said contact strip of less than 2 mm.

4. The printed circuit board according to claim **1**, wherein:

said printed circuit board has a height of 1 to 1.2 inches perpendicular to said contact strip.

5. The printed circuit board according to claim **1**, wherein:

said housing of each one of said semiconductor memories is a TSOP housing.

6. The printed circuit board according to claim **1**, wherein:

said at least nine semiconductor memories define exactly nine semiconductor memories.

7. The printed circuit board according to claim **1**, wherein:

said printed circuit board is configured according to a specification selected from a group consisting of a raw card A of a PC 133 SDRAM registered DIMM design specification and a raw card F of the PC 133 SDRAM registered DIMM design specification.

8. The printed circuit board according to claim **1**, wherein:

said printed circuit board has a width of 5.25 inches.

* * * * *

EXHIBIT 4

US007206978B2

(12) **United States Patent**
Kuzmenka et al.

(10) **Patent No.: US 7,206,978 B2**
(45) **Date of Patent: Apr. 17, 2007**

(54) **ERROR DETECTION IN A CIRCUIT MODULE**

(75) Inventors: **Maksim Kuzmenka**, Munich (DE); **Siva Raghurma**, Germering (DE)

(73) Assignee: **Infineon Technologies AG**, Munich (DE)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 185 days.

(21) Appl. No.: **10/857,596**

(22) Filed: **May 27, 2004**

(65) **Prior Publication Data**

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(30) **Foreign Application Priority Data**

May 28, 2003 (EP) 03012064

(51) **Int. Cl.**
G06F 11/00 (2006.01)

(52) **U.S. Cl.** **714/56**

(58) **Field of Classification Search** 710/22, 710/26–27, 52; 714/48, 49, 52–54, 56, 768, 714/769, 799–801, 805
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,360,917 A 11/1982 Sindelar et al.
5,173,905 A * 12/1992 Parkinson et al. 714/768
5,423,030 A 6/1995 Byers et al.
6,137,734 A * 10/2000 Schoner et al. 365/194
6,496,946 B2 * 12/2002 Bannatyne et al. 714/25
6,941,493 B2 * 9/2005 Phelps 714/53

OTHER PUBLICATIONS

Error Correction and Detection (Wikipedia definition).*
Identify RAM Chips, Skeeterbytes.com.*
DIMM, Computers, the Past, Present, and Future.*

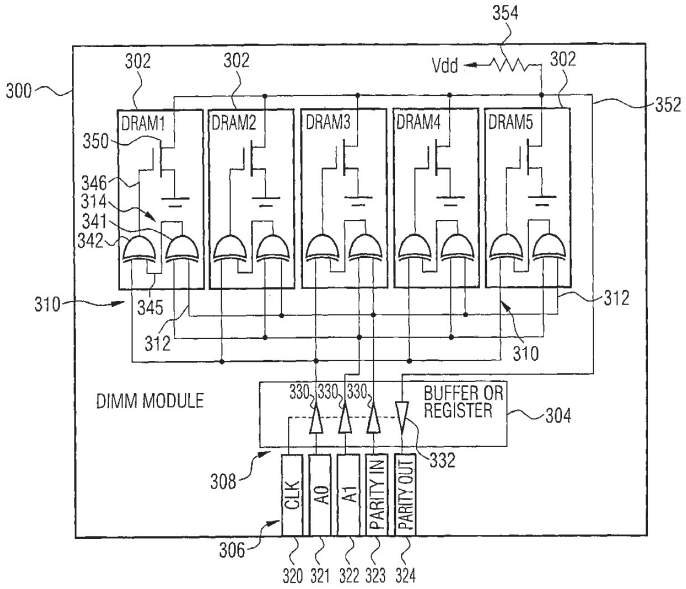
* cited by examiner

Primary Examiner—Khanh Dang
(74) *Attorney, Agent, or Firm*—Slater & Matsil, L.L.P.

(57) **ABSTRACT**

A circuit module has a module board and a plurality of circuit chips that are arranged on the module board. A module main bus having a plurality of lines of the circuit module branches into a plurality of sub-buses having a plurality of lines. Each of the sub-buses is connected to one of the circuit chips. Each circuit chip has an indication signal generating unit for providing an indication signal based on a combination of the signals received on the plurality of lines of the sub-bus connected to the respective circuit chip, and an indication signal output for outputting the indication signal.

14 Claims, 4 Drawing Sheets



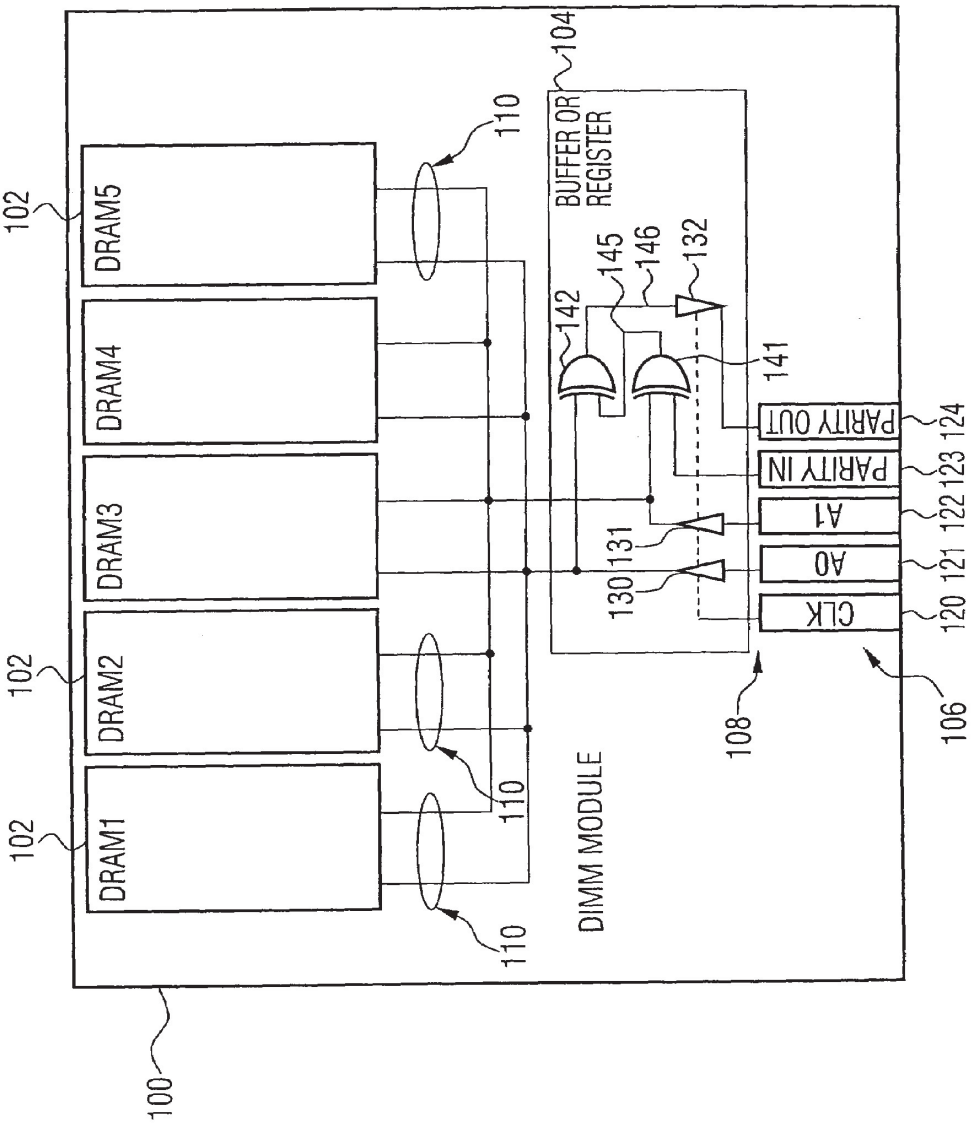


FIG 1
(PRIOR ART)

Exhibit 4
Page 064

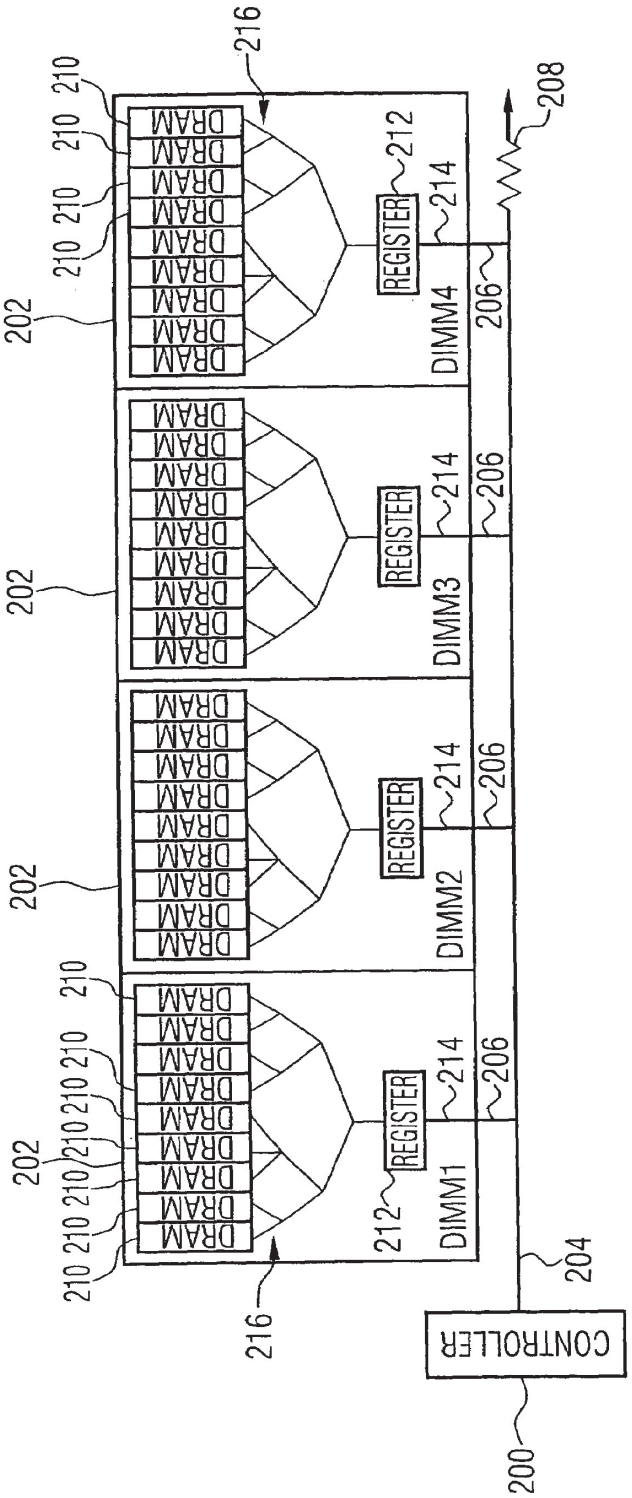
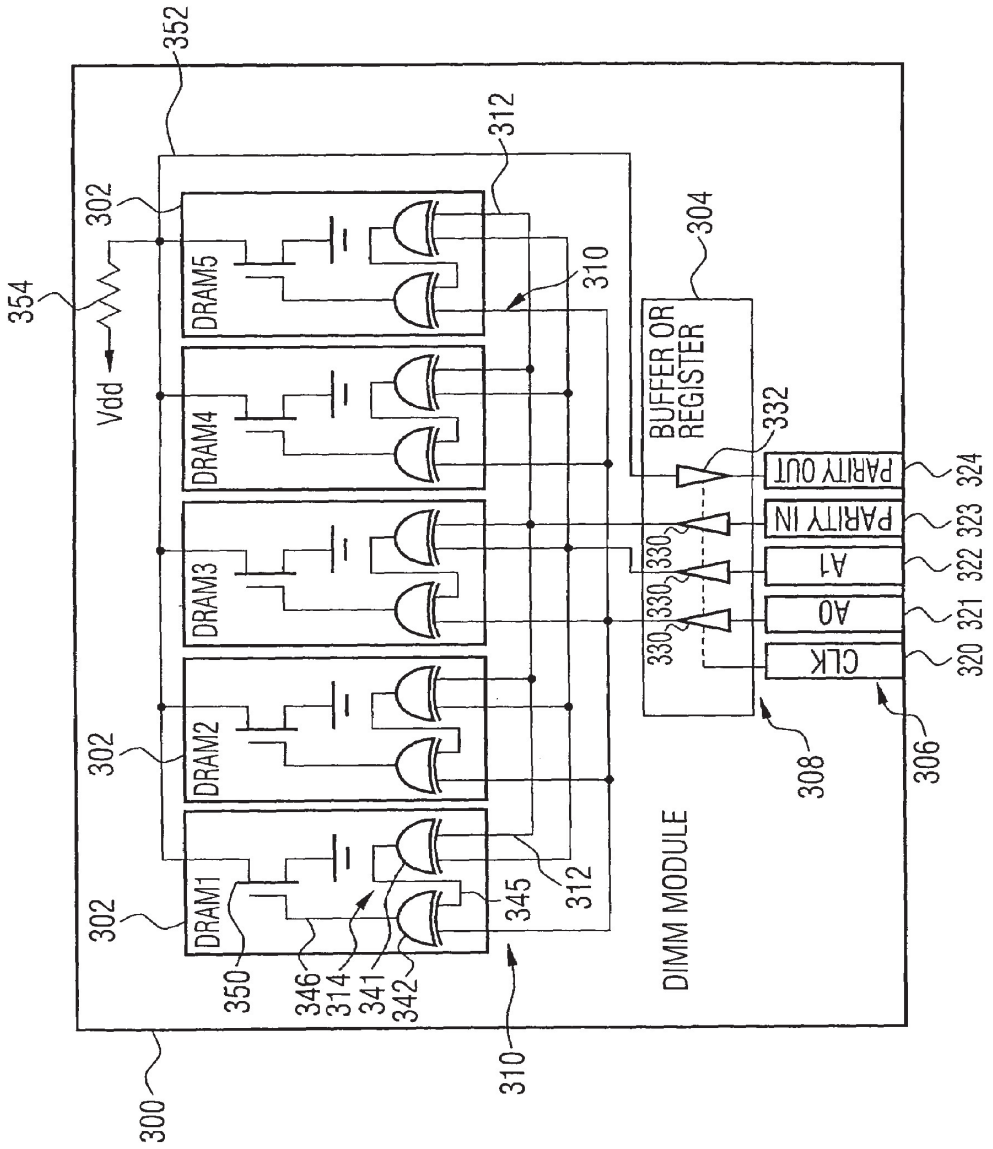


FIG 2 (PRIOR ART)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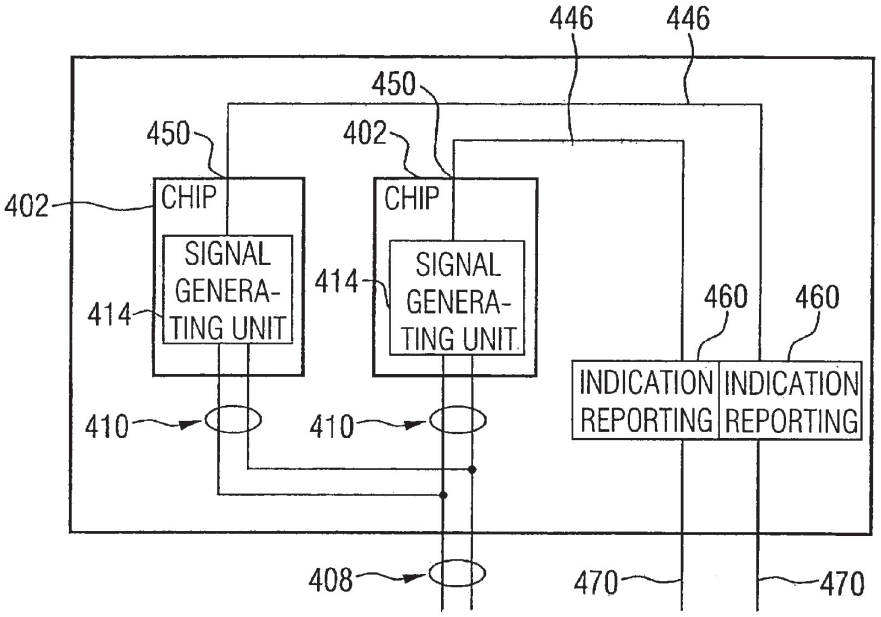
312
302
304
354
Vdd
DRAM5
DRAM4
DRAM3
DRAM2
DRAM1
310
BUFFER OR REGISTER
332
PARITY OUT
PARITY IN
A1
A0
CLK
324
323
322
321
320
330
330
330
308
306
DIMM MODULE
302
302
302
350
346
314
341
342
345
312
310
300

FIG 3

FIG 4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SIGNAL GENERA-TING UNIT
SIGNAL GENERA-TING UNIT
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INDICATION REPORTING
410
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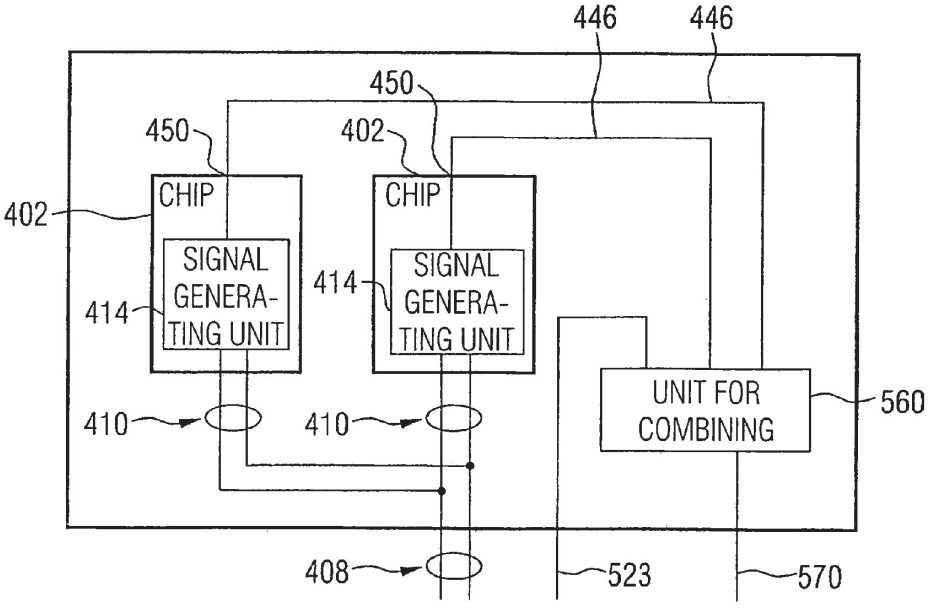
408
470
470

FIG 5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410
408
523
570

ERROR DETECTION IN A CIRCUIT MODULE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a circuit module and, in particular, to an error detection in a circuit module comprising a module board and a plurality of circuit chips arranged on the module board.

2. Description of the Related Art

A conventional structure of computer main memory systems includes a memory controller, a main memory bus and memory chips, DRAM chips for example, that are arranged on memory modules, DIMMs (DIMM=Duals In-Line Memory Module) for example. The main memory bus connects the memory modules to the memory controller. In general, the main memory bus comprises a data bus, a command/address bus, and lines carrying clock signals and check signals.

Conventionally, error detection and correction on the main memory bus is done on the data bus only, by including additional bits or even chips and by using special algorithms for processing data received via the data bus.

Some prior art computer main memory systems comprise additional error detection means to detect errors on the command/address bus. In such systems, the memory controller generates a check signal which is driven to the memory modules. Each memory module comprises an error detection unit that detects an error on the command/address bus by making use of the check signal. In case of a detected error, the error detection unit generates an error signal that is driven back to the memory controller.

FIG. **1** shows a schematic view of such a prior art memory module. The memory module is in the form of a registered DIMM. The memory module comprises a module board **100**, a plurality of memory chips (DRAMs) **102**, a buffer or register **104** and a connector portion **106**. The connector portion **106** is connected to the buffer or register **104** via a module main bus **108**. At the output of the buffer or register **104**, the module main bus **108** branches into sub-busses **110** each of which being connected to one of the memory chips **102**.

The connector portion **106** comprises a plurality of terminals **120** to **124** to receive or drive a plurality of signals from or to a memory bus on a motherboard (not shown) to which the memory module is connected. A clock signal CLK is applied at terminal **120**, address signals A**0** and Al are applied at terminals **121** and **122**, a check signal Parity IN is applied at terminal **123** and an error signal Parity OUT is applied at terminal **124**. In FIG. **1** only those components necessary to explain the functionality of interest, i.e. the components associated to the command/address bus are shown. Moreover, for simplicity, only two address bits A**0** and A**1** of the command/address bus are shown, while usual command/address busses comprise 24 to 27 bits.

The buffer or register **104** comprises buffer or register elements, drivers **130**, **131** and **132** and an error detection circuit, comprising XOR-gates **141** and **142**.

The drivers **130** and **131** are operable to drive the address lines and are controlled by the clock signal CLK.

First and second inputs of the first XOR-gate **141** are connected to the terminals **122** and **123**, respectively. Thus, the memory bus signals A**1** and Parity IN provide the input signals for the first XOR-gate **141**. The output **145** of the first XOR-gate **141** is connected to a first input of the second XOR-gate **142** which is also connected to the terminal **121**.

The terminal **121** provides the A**0** bit, which is the next less significant bit of the memory bus bits. The output **146** of the second XOR-gate **142** is connected to the driver **132** which samples the output **146** with the signal CLK. The output of the driver **132** is connected to the terminal **125** which applies the error signal Parity OUT to the memory bus.

The error detection circuit provides error detection by way of parity checking. The check signal Parity IN provides a parity bit for the memory bus signal bits A**0** and A**1** that is generated and provided by a memory controller (not shown). The value of the parity bit depends on the number of "1" bits on the memory bus signals A**0** and A**1**, at a time. If there is an odd number of "1" bits, the corresponding parity bit has a high value, otherwise if there is an even number of "1" bits, the parity bit has a low value. The Parity Checking is done by way of XOR-gates. There are as many XOR-gates as there are bits on the memory command/address bus. The output of each XOR-gate and the next less significant command/address bus bit, referred to the command/address bus bit taken as input for the current XOR-gate, are taken as input for the next XOR-gate. The output bit of the last XOR-gate is an error bit and is driven back to the memory controller.

The Signal Parity OUT has a low value as long as there is no error detected on the module main bus **108** by the error detection circuit. In case of a single bit error the Signal Parity OUT will turn to an high value. A memory controller that checks the Signal Parity OUT can therefore detect single bit errors on the memory bus. Multiple bit errors cannot be detected for sure.

The error detection method as described in FIG. **1** is restricted to registered (buffered) memory modules and has the disadvantage that errors that occur on one of the sub-busses **110** are not detected.

The complexity of non-protected sub-buses on a memory module of a kind as shown in FIG. **1** is illustrated in FIG. **2**. FIG. **2** shows a schematic view of a computer main memory system comprising a memory controller **200** and a plurality of memory modules **202** in the form of registered DIMMs. The memory controller **200** is connected to a main memory bus **204**, which branches into a plurality of memory busses **206** each of which is connected to one of the memory modules **202**. The main memory bus **204** is terminated by a termination resistor **208**.

Each memory module **202** comprises a plurality of memory chips **210** in the form of DRAM chips. To be more specific, in the embodiment shown in FIG. **2** four memory modules **202** are shown and nine memory chips **210** are arranged on each memory module **202**. Each memory module **202** comprises a buffer or register **212** that comprises error detection circuit elements as described in FIG. **1**. (The error detection circuit elements are not shown in particular in FIG. **2**.) On each memory module **202** a module main bus **214** connects the respective memory bus **206** to the buffer or register **212**. At the output of the buffer or register **212** the module main bus **214** branches into a plurality of sub-busses **216** each of which is connected to one of the memory chips **210**. This high number of sub-busses **216** is not protected by the error detection circuit elements that are embedded in the registers **210**. Thus, as outlined above, errors that occur on command/address lines of the sub-busses **216** cannot be detected according to this prior art approach.

SUMMARY OF THE INVENTION

In one aspect, the present invention provides a circuit module comprising a plurality of circuit chips that allows improved error detection.

In accordance with a first aspect, the present invention provides a circuit module having a module board; a plurality of circuit chips arranged on the module board; a main bus having a plurality of lines, branching into a plurality of sub-buses having a plurality of lines, each of the sub-busses being connected to one of the plurality of circuit chips; wherein each circuit chip has an indication signal generating unit for providing an indication signal based on a combination of the signals received on the plurality of lines of the sub-bus connected to the respective circuit chip, and an indication signal output for outputting the indication signal.

In accordance with a second aspect, the present invention provides a memory chip having a memory bus input for receiving signals from a memory bus having a plurality of lines; wherein the circuit chip has an indication signal generating unit for providing an indication signal based on a combination of the signals received on the plurality of lines of the memory bus connected to the circuit chip, and an indication signal output for outputting the indication signal.

The present invention is based on the finding that in new generations of memory systems that provide high data rates, errors that happen on a command/address bus on a memory module become significant for the error rate of the whole system.

Therefore, according to the inventive arrangement, indication signal generating units are embedded within each circuit chip of a circuit module (a memory module, for example). Each circuit chip is connected to a sub-bus (a memory command/address sub-bus, for example) having a plurality of lines. The indication signal generating units comprise check sum calculation means that allow to indicate an error on the lines of the sub-bus connected to the respective circuit chip by way of calculating a check sum of the signals of the sub-bus and by providing an indication signal.

In a first embodiment, means for providing a check signal to each of the circuit chips are provided, wherein, in the circuit chips, the check sum and the check signal are combined to form the indication signal, which, in this case, represent an error signal.

In alternative embodiments, error detection is provided downstream by comparing the indication signal with a check signal that provides checksum information for the signals of the memory sub-bus and is provided by a memory controller. Means for comparing the indication signal with the check signal provide a module error out signal that informs the memory controller about a detected error. The means for comparing can be arranged, on the module board or even in the memory controller.

Arranging the means for comparing outside the circuit chip has the advantage that resources of the circuit chip, otherwise used for providing and combining the check signal to the sub-bus signals are available for additional features.

The advantage of the inventive method is that errors on a command/address bus of a computer main memory system are detected irrespective of whether same occur before or after a buffer or register on a registered memory module (a registered DIMM, for example) and the method also works for un-registered memory modules. The inventive approach of error detection allows to detect errors occurred on the command/address bus between a memory controller and each of the memory chips (DRAMs, for example) on the memory modules. In case of a detected error, it allows the memory controller to repeat sending data, reduce the data rate or change parameters like slew rate or drive strength.

In a preferred embodiment the memory chips are grouped in groups or banks of memory chips and an individual indication out or module error out signal is generated for each group. This provides the memory controller with detailed information about the location an error occurred.

In case of highly stable system requirements, each individual memory chip may have a separate indication or error bit reporting to the memory controller.

In a further embodiment error detection circuit elements in a buffer or register on a module board, according to the prior art, are combined with error detection means, according to the present invention. This combination provides exact information about the source on an error.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the present invention are described hereinafter making reference to the appended drawings.

FIG. **1** shows a schematic view of a memory module according to the prior art;

FIG. **2** shows a schematic view of a computer main memory system according to the prior art;

FIG. **3** shows a schematic view of a memory module embodying the present invention;

FIG. **4** shows a schematic view of a further preferred embodiment of a memory module according to the present invention; and

FIG. **5** shows a schematic view of another preferred embodiment of a memory module according to the present invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

FIG. **3** shows a schematic view of a memory module, according to the present invention. The memory module is in the form of a registered DIMM. The memory module comprises a module board **300**, a plurality of memory chips (DRAMs) **302**, a buffer or register **304** and a connector portion **306**. The connector portion **306** is connected to the buffer or register **304** via a module main bus **308**. At the output of the buffer or register **304**, the module main bus **308** branches into sub-busses **310** each of which being connected to one of the memory chips **302**. Each sub-bus **310** comprises a check signal line **312**, which provides a check bit to an indication signal generating unit **314** that is embedded in each memory chip **302**.

The connector portion **306** comprises a plurality of terminals **320** to **324** to receive or drive a plurality of signals from or to a memory bus on a motherboard (not shown) to which the memory module is connected. A clock signal CLK is applied at terminal **320**, address signals A**0** and A**1** are applied at terminals **321** and **322**, a check signal Parity IN is applied at terminal **323** and an error signal Parity OUT is applied at terminal **324**. In FIG. **3** only those components necessary to explain the invention, i.e. the components associated to the command/address bus are shown. Moreover, for simplicity, only two address bits A**0** and A**1** of the command/address bus are shown, while usual command/address busses comprise 24 to 27 bits.

The buffer or register **304** comprises buffer or register elements, input drivers **330** and an output driver **332**.

The inputs of the drivers **330** are connected to the terminals **321**, **322** and **323**. The drivers **330** and **332** are also connected to the terminal **320** to be supplied with the clock signal CLK. At the output of the drivers **330** the module main bus **308** branches into the sub-busses **310**, each of which is connected to one of the memory chips **302**.

Usually each DRAM chip **302** comprises on the input a latch device, which latches command/address signals **321** and **322** with a rising edge of a clock signal. The indication signal generating unit **314** is arranged downstream of this latch, in order to prevent that slight differences in an arrival time of the command/address signals **321** and **322** generate short glitches on an output of the indication signal generating unit **314**. For sake of simplicity, this latch device is not shown in the figures.

In the embodiment shown in FIG. **3**, the indication signal generating unit **314** comprises two XOR gates **341** and **342**. The first XOR-gate **341** is connected to a sub-bus signal line that provides the signal A**1** and to the check signal line **312**. Both lines provide the input bits for the first XOR-gate **341**. Bit A**1** is the most significant of the command/address sub-bus bits. The output **345** of the first XOR-gate **341** is connected to the second XOR-gate **342**, which is additionally connected to the sub-bus signal line that provides the signal A**1**, which is the next less significant bit of the command/address sub-bus bits. The second XOR-gate **342** outputs an indication signal **346** that is connected to an open-drain output buffer **350**.

In this embodiment the indication signals **346** are generated in the indication signal generating units **314** by calculating a check-sum of the command/address signals **321** and **322** of the sub-busses **310** and by combining the check signal **312** with the calculated check-sums. Due to the distributive law, the result of the combining is not affected by the ordering of the signals being combined. The check signal **312** is provided by the memory controller and is a pre-calculated check bit, representing a parity bit for the command/address signal **321** and **322**. Thus, in this embodiment the indication signal generating unit **314** is configured to indicate and to detect and error on the address/command signals **321** and **322** and the generated indication signal **346** represents therefore an error signal.

In this embodiment, the output buffers **350** of all memory chips **302** are connected to an error signal line **352**. In case there is no error detected, the error signal at line **352** has a high value, due to a pull-up resistor **354** that is connected to the error signal **352**. In case of an error detected by an indication signal generating unit **314** in any of the memory chips **302**, the error signal **352** is pulled down to a low value by the output buffer **350** of the respective memory chip **302** the error was detected in. As all output buffers **350** are connected together, an error is indicated by the error signal **352** independently of being detected in one of the indication signal generating units **314** or in several of the indication signal generating units **314**. The error signal line **352** is connected to the output driver **332**. The output of the driver **332** is connected to the terminal **325**, which applies the error signal Parity OUT to the memory bus.

In cases the error signal line **352** could be not fast enough to deliver one bit long error signal back to the register/buffer **304**, it might be preferable to include a pulse time expander (not shown) between the output of the XOR gate **342** and the gate of the transistor **350**. The pulse time expander represents a sticky bit unit that can be implemented by way of a flip-flop which is set-up by the indication signal **346**, independently of the duration the indication signal **346** is driven, and reset back to normal state after a defined time period (after a number of clock cycles counted by a counter, for example) or a special command provided on the command/address bus.

In operation, the memory controller receives information about an error occurred on command/address bus lines anywhere between the memory controller and the circuit chips.

In the embodiments shown in FIG. **3**, the error signal output of the DRAMs represent the indication signal of the inventive circuit module or memory chip. Alternatively, the indication signal can be formed by combining the signals on the lines of a respective sub-bus only as it is described hereinafter making reference to FIGS. **4** and **5**.

FIG. **4** shows a circuit module according to a preferred embodiment of the invention in that an indication signal is formed by combining signals on lines of a respective sub-bus.

A circuit module comprises a module board **400** and two circuit chips **402** that are arranged on the module board **400**. A main bus **408** branches into two sub-busses **410**. Each sub-bus **410** has a plurality of lines that are connected to an indication signal generating unit **414** that is arranged in each circuit chip **402**. The indication signal generating units **414** combine the signals of the respective sub-bus **410** that is connected to the indication signal generating unit **414** and provide an indication signal **446**, each. Each indication signal line **446** is driven by a indication signal output **450** and connected to an indication reporting means **460** that is configured to drive an module indication out signal **470**.

A value of the indication signal **446** at a time depends on the number of "1" bits that are driven on the lines of the sub-bus **410**. Thus, the indication signal generating unit **414** calculates a check sum of the bits of the sub-bus **410**. This check-sum bit is driven back via the indication signal **446** and the module indication out signal **470** to a memory controller (not shown) which compares the received module indication out signal bit **470** with a pre-calculated check-sum bit. If the two bits do not coincide, an error has occurred.

FIG. **5** shows another embodiment in that an indication signal is formed by combining signals on lines of a respective sub-bus. Objects corresponding to objects shown in FIG. **4** have the same reference number and are not described hereinafter.

In addition to the embodiment shown in FIG. **4**, a module board **500** comprises a check signal **523** that is provide by a memory controller (not shown) as described in FIG. **3**. The check signal **523** is connected to an unit for combining **560** which is arranged on the module board **500**. Two indication signals **446** are provided in the was as can be seen from FIG. **4**. The indication signal lines **446** are connected to the unit for combining **560**, too.

The unit for combining **560** is configured to compare the check signal **523** with each of the indication signals **446**. If the check signal **523** and one of the indication signals **446** do not coincide, an error has occurred and is reported via an module error out signal **570** to the memory controller.

In a preferred embodiment, memory chips on a memory module are grouped in different groups or banks. Indication signals of indication signal generating units of memory chips belonging to the same group are combined together and connected to additional group-indicating signal lines associated to the respective group. The group-indicating signals are driven to the memory controller. Thus, there is detailed information provided about where an error has occurred.

In an embodiment for a highly stable system, each individual memory chip comprises a separate indicating bit which is set by an indicating signal generating unit in the respective memory chip. In operation, the value of the error bit is reported to a memory controller.

In a further embodiment, a memory module combines an error detection method as described in the present invention with a prior art error detection method as described in FIG. **1**. Thus, in operation it can be distinguished between an error source on a memory bus or on a memory sub-bus on the memory module.

Although the present invention has been described above, making reference to memory modules, it is clear that the present invention can also be used in connection with other circuit modules which comprise circuit chips that are connected to a data bus. Additionally, the inventive arrangement of an indication signal generating unit embedded within a circuit chip can also be used for systems comprising a single circuit chip.

While this invention has been described in terms of several preferred embodiments, there are alterations, permutations, and equivalents which fall within the scope of this invention. It should also be noted that there are many alternative ways of implementing the methods and compositions of the present invention. It is therefore intended that the following appended claims be interpreted as including all such alterations, permutations, and equivalents as fall within the true spirit and scope of the present invention.

What is claimed is:

1. A circuit module comprising:

a module board;

a plurality of circuit units arranged on the module board, each circuit unit consisting of a single integrated circuit memory chip;

a main bus having a plurality of lines, branching into a plurality of sub-buses having a plurality of lines, each of the sub-busses being connected to one of the plurality of circuit units;

wherein each circuit unit comprises an indication signal generating unit for providing an indication signal based on a combination of the signals received on the plurality of lines of the sub-bus connected to the respective circuit unit, and an indication signal output for outputting the indication signal.

2. The circuit module according to claim **1**, further comprising means for providing a check signal to each of the circuit unit, and wherein said indication signal generating unit generates said indication signal based on a combination of the signals on the plurality of lines of the respective sub-bus and the check signal, so that the indication signal represents an error signal.

3. The circuit module according to claim **2**, further comprising an error reporting means, being connected to the indication signal outputs of the circuit units, and wherein each error reporting means is configured to drive a module error out signal.

4. The circuit module according to claim **3**, wherein the error reporting means is configured to indicate the circuit unit, the error signal is received from, or to indicate a group of circuit unit, the error signal is received from.

5. The circuit module according to claim **1**, further comprising a plurality of indication reporting means, each being connected to one of the indication signal outputs of the circuit unit, and wherein each indication reporting means is configured to drive a module indication out signal.

6. The circuit module according to claim **1**, wherein the circuit module comprises a unit for combining the indication signal with a check signal to provide a module error out signal.

7. The circuit module according to claim **6**, wherein the unit for combining is configured to indicate the circuit unit an error was detected in or to indicate a group of circuit unit, an error was detected in.

8. The circuit module according to claim **1**, further comprising a main bus error detection unit for detecting errors on the main bus making use of the check signal.

9. The circuit module according to claim I, wherein each circuit unit comprises a sticky bit unit, arranged between the indication signal generating unit and the indication signal output, for holding information of the indication signal.

10. The circuit module according to claim **1**, wherein the circuit module is a dual in-line memory module (DIMM), wherein the circuit units are memory units, wherein the main bus is a memory main bus, and the sub-busses are memory sub-busses.

11. The circuit module according to claim **10**, wherein the memory main bus is a command/address bus.

12. The circuit module according to claim **2**, wherein the check signal is a panty signal.

13. A memory unit, consisting of a single integrated circuit memory chip, comprising:

a memory bus input for receiving signals from a memory bus having a plurality of lines;

wherein the memory unit comprises an indication signal generating unit for providing an indication signal based on a combination of the signals received on the plurality of lines of the memory bus connected to the memory unit, and an indication signal output for outputting the indication signal.

14. The memory unit according to claim **13**, comprising a check signal input for receiving a check signal, and wherein said indication signal generating unit generates said indication signal based on a combination of the signals on the plurality of lines of the memory bus and the check signal, so that the indication signal represents an error signal.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

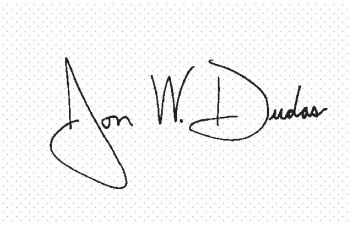
PATENT NO. : 7,206,978 B2
APPLICATION NO. : 10/857596
DATED : April 17, 2007
INVENTOR(S) : Kuzmenka et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 8, line 17; delete “unit” insert --units--
Column 8, line 23; delete “I” insert --1--
Column 8, line 36; delete “panty” insert --parity--

Signed and Sealed this

Nineteenth Day of June, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office

EXHIBIT 5

US007315454B2

(12) **United States Patent**
Schuster

(10) **Patent No.: US 7,315,454 B2**
(45) **Date of Patent: Jan. 1, 2008**

(54) **SEMICONDUCTOR MEMORY MODULE**

(75) Inventor: **Josef Schuster**, München (DE)

(73) Assignee: **Infineon Technologies AG**, Neubiberg (DE)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(51) **Int. Cl.**
H05K 7/02 (2006.01)

(52) **U.S. Cl.** **361/736**; 361/760; 361/748; 174/260; 29/834; 365/63; 257/723

(58) **Field of Classification Search** 361/720, 361/722, 723, 737, 736, 748, 760, 764, 783; 174/260; 365/63; 257/723, 724, 778, 698, 257/700, 686; 29/832, 834–836
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,885,841 A * 12/1989 McNabb 29/834
5,974,331 A * 10/1999 Cook et al. 455/461
5,982,654 A * 11/1999 Corisis 365/63
6,160,718 A * 12/2000 Vakilian 361/803
6,169,325 B1 * 1/2001 Azuma et al. 257/685
6,181,004 B1 * 1/2001 Koontz et al. 257/691
6,222,739 B1 * 4/2001 Bhakta et al. 361/790
6,266,265 B1 * 7/2001 Sakuragi 365/63
6,301,141 B1 * 10/2001 Morgan et al. 365/51
6,320,779 B1 * 11/2001 Morgan et al. 365/51
6,327,127 B1 * 12/2001 Utsunomiya et al. 361/92
6,353,539 B1 * 3/2002 Horine et al. 361/736
6,430,075 B2 * 8/2002 Morgan et al. 365/51
6,502,161 B1 * 12/2002 Perego et al. 711/5
6,850,414 B2 * 2/2005 Benisek et al. 361/748
6,873,534 B2 * 3/2005 Bhakta et al. 365/63
6,891,729 B2 * 5/2005 Ko et al. 361/736
6,930,900 B2 * 8/2005 Bhakta et al. 365/51
2002/0006032 A1 * 1/2002 Karabatsos 361/760
2002/0196612 A1 12/2002 Gall et al.
2007/0091704 A1 * 4/2007 RaghuRam et al. 365/218

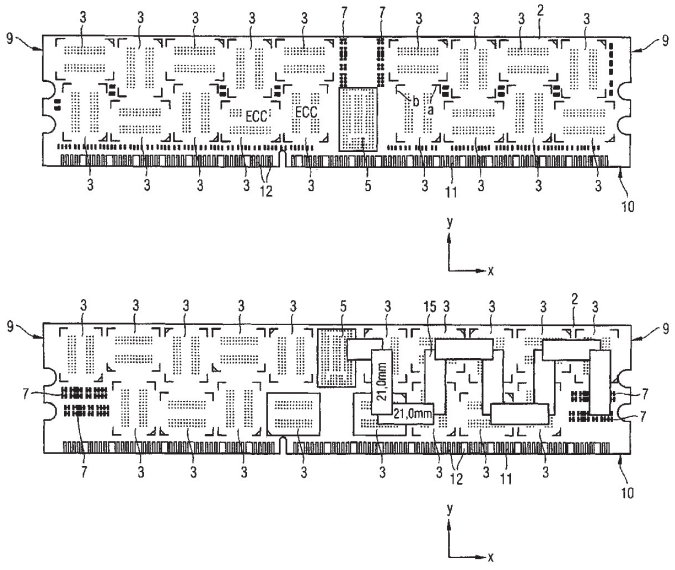
* cited by examiner

Primary Examiner—Dean A. Reichard
Assistant Examiner—Dameon E. Levi
(74) *Attorney, Agent, or Firm*—Edell, Shapiro & Finnan, LLC

(57) **ABSTRACT**

A semiconductor memory module includes an electronic printed circuit board with a contact strip and a plurality of semiconductor memory chips of identical type that are mounted on at least one external area of the printed circuit board. The semiconductor memory chips are rectangular in shape and are arranged, in at least two rows with the adjacent chips being oriented perpendicular to one another, such that the area used on the PC board is optimized.

7 Claims, 8 Drawing Sheets



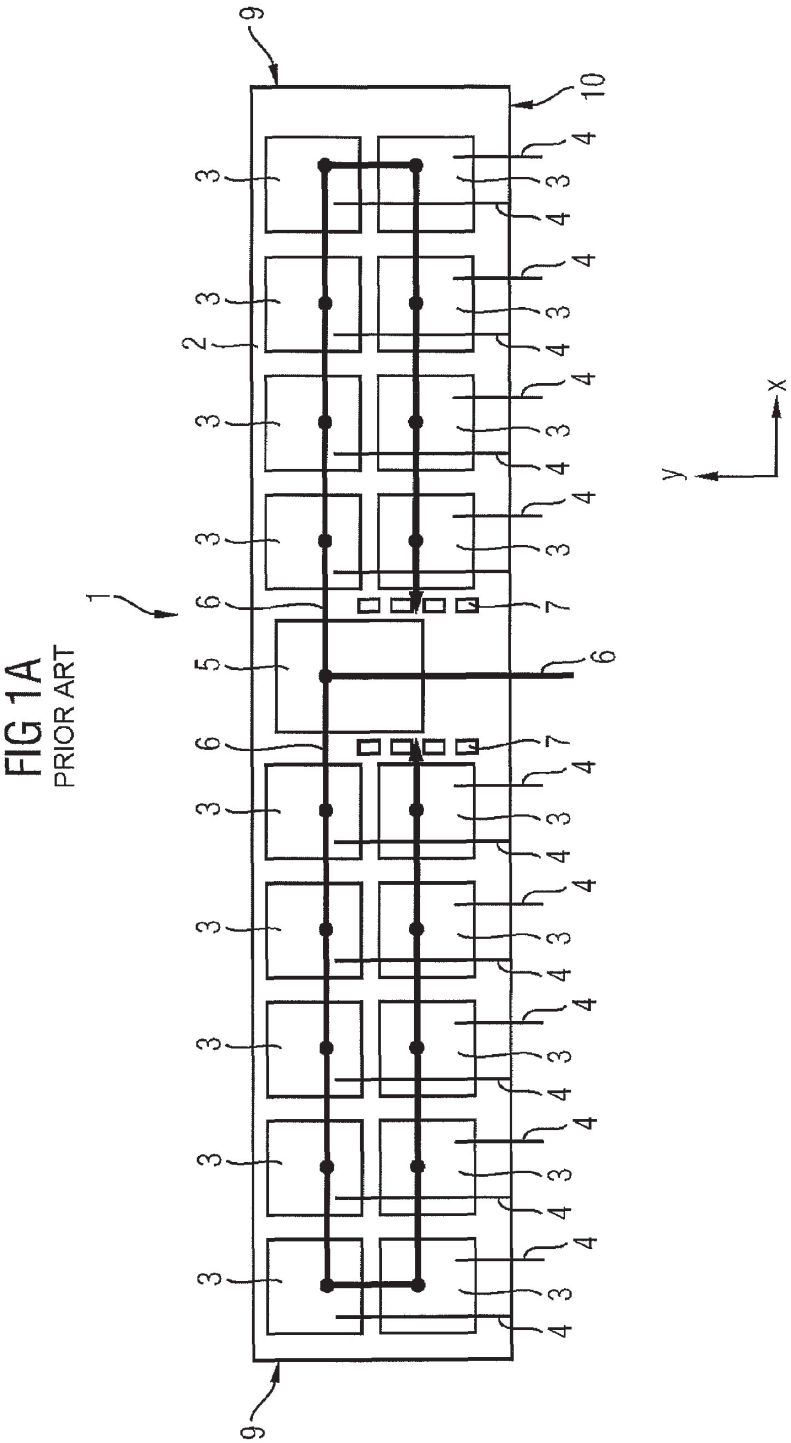


FIG 1A
PRIOR ART