POS-010

ATTORNEY OR PARTY WITHOUT ATTORNEY (Name, State Bar number, and address):	FOR COURT USE ONLY
Steven Cherensky (Bar No. 168275) Tensegrity Law Group LLP 555 Twin Dolphin Drive, Suite 650 Redwood Shores, CA 94065 TELEPHONE NO.: 650-802-6000 FAX NO. (Optional): 650-802-6001 E-MAIL ADDRESS (Optional): Steven.Cherensky@tensegritylawgroup.com ATTORNEY FOR (Name): Polaris Innovations Limited	
UNITED STATES DISTRICT COURT, CENTRAL DISTRICT OF CALIFORNIA STREET ADDRESS: 411 West Fourth Street MAILING ADDRESS: 411 West Fourth Street, Room 1053 CITY AND ZIP CODE: Santa Ana, CA 92701-4516 BRANCH NAME:	
PLAINTIFF/PETITIONER: Polaris Innovations Limited DEFENDANT/RESPONDENT: Kingston Technology Company, Inc.	CASE NUMBER: 8:16-cv-300 CJC (RAOx)
PROOF OF SERVICE OF SUMMONS	Ref. No. or File No.: Polaris-Kingston

(Separate proof of service is required for each party served.)

1. At the time of service I was at least 18 years of age and not a party to this action.
2. I served copies of:
   a. [✓] summons
   b. [✓] complaint
   c. [ ] Alternative Dispute Resolution (ADR) package
   d. [✓] Civil Case Cover Sheet *(served in complex cases only)*
   e. [ ] cross-complaint
   f. [✓] other *(specify documents):* see attached list of ADDITIONAL DOCUMENTS SERVED
3. a. Party served *(specify name of party as shown on documents served):*
   Kingston Technology Company, Inc.
   b. [X] Person (other than the party in item 3a) served on behalf of an entity or as an authorized agent (and not a person under item 5b on whom substituted service was made) *(specify name and relationship to the party named in item 3a):*
   ACCEPTED BY LYNANNE GARES (MANAGING AGENT OF CORPORATION)
4. Address where the party was served: CORPORATION SERVICE COMPANY
   2711 CENTERVILLE RD., WILMINGTON, DE 19808
5. I served the party *(check proper box)*
   a. [XX] **by personal service.** I personally delivered the documents listed in item 2 to the party or person authorized to receive service of process for the party (1) on *(date):* 2/25/16 (2) at *(time):* 12:30pm
   b. [ ] **by substituted service.** On *(date):* at *(time):* I left the documents listed in item 2 with or in the presence of *(name and title or relationship to person indicated in item 3):*
      (1) [ ] **(business)** a person at least 18 years of age apparently in charge at the office or usual place of business of the person to be served. I informed him or her of the general nature of the papers.
      (2) [ ] **(home)** a competent member of the household (at least 18 years of age) at the dwelling house or usual place of abode of the party. I informed him or her of the general nature of the papers.
      (3) [ ] **(physical address unknown)** a person at least 18 years of age apparently in charge at the usual mailing address of the person to be served, other than a United States Postal Service post office box. I informed him or her of the general nature of the papers.
      (4) [ ] I thereafter mailed (by first-class, postage prepaid) copies of the documents to the person to be served at the place where the copies were left (Code Civ. Proc., § 415.20). I mailed the documents on *(date):* from *(city):* **or** [ ] a declaration of mailing is attached.
      (5) [ ] I attach a **declaration of diligence** stating actions taken first to attempt personal service.

Form Adopted for Mandatory Use
Judicial Council of California
POS-010 [Rev. January 1, 2007]

PLAINTIFF/PETITIONER: Polaris Innovations Limited	CASE NUMBER:
DEFENDANT/RESPONDENT: Kingston Technology Company, Inc.	8:16-cv-300 CJC (RAOx)

5. c. ☐ **by mail and acknowledgment of receipt of service.** I mailed the documents listed in item 2 to the party, to the address shown in item 4, by first-class mail, postage prepaid,
   (1) on *(date):* (2) from *(city):*
   (3) ☐ with two copies of the *Notice and Acknowledgment of Receipt* and a postage-paid return envelope addressed to me. *(Attach completed* Notice and Acknowledgement of Receipt.*)* (Code Civ. Proc., § 415.30.)
   (4) ☐ to an address outside California with return receipt requested. (Code Civ. Proc., § 415.40.)

   d. ☐ **by other means** *(specify means of service and authorizing code section):*

   ☐ Additional page describing service is attached.

6. The "Notice to the Person Served" (on the summons) was completed as follows:
   a. ☐ as an individual defendant.
   b. ☐ as the person sued under the fictitious name of *(specify):*
   c. ☐ as occupant.
   d. XXX On behalf of *(specify):* KINGSTON TECHNOLOGY COMPANY, INC.
   under the following Code of Civil Procedure section:

☒ 416.10 (corporation)	☐ 415.95 (business organization, form unknown)
☐ 416.20 (defunct corporation)	☐ 416.60 (minor)
☐ 416.30 (joint stock company/association)	☐ 416.70 (ward or conservatee)
☐ 416.40 (association or partnership)	☐ 416.90 (authorized person)
☐ 416.50 (public entity)	☐ 415.46 (occupant)
	☐ other:

7. **Person who served papers**
   a. Name: KEVIN S. DUNN
   b. Address: PO BOX 1360, WILMINGTON, DE 19899
   c. Telephone number: 302-475-2600
   d. **The fee** for service was: $89.00
   e. I am:
      (1) XX not a registered California process server.
      (2) ☐ exempt from registration under Business and Professions Code section 22350(b).
      (3) ☐ a registered California process server:
         (i) ☐ owner ☐ employee ☐ independent contractor.
         (ii) Registration No.:
         (iii) County:

8. XX **I declare** under penalty of perjury under the laws of the State of California that the foregoing is true and correct.

   or

9. ☐ **I am a California sheriff or marshal and** I certify that the foregoing is true and correct.

Date: 2/25/16

KEVIN S. DUNN
(NAME OF PERSON WHO SERVED PAPERS/SHERIFF OR MARSHAL)

▶ (SIGNATURE)

UNITED STATES DISTRICT COURT
CENTRAL DISTRICT OF CALIFORNIA
SOUTHERN DIVISION

POLARIS INNOVATIONS LIMITED, an Irish limited company, Plaintiff, vs. KINGSTON TECHNOLOGY COMPANY, INC., a Delaware corporation, Defendant.	Case No. 8:16-cv-300 CJC (RAOx) **ADDITIOANL DOCUMENTS SERVED**

- REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
- PLAINTIFF'S APPLICATION FOR LEAVE TO FILE UNDER SEAL CERTIFICATION AND NOTICE OF INTERESTED PARTIES
- [PROPOSED] ORDER GRANTING PLAINTIFF'S APPLICATION FOR LEAVE TO FILE UNDER SEAL CERTIFICATION AND NOTICE OF INTERESTED PARTIES
- REDACTED VERSION OF CERTIFICATION AND NOTICE OF INTERESTED PARTIES (Local Rule 7.1-1)
- NOTICE OF ASSIGNMENT TO UNITED STATES JUDGES
- NOTICE TO PARTIES OF COURT–DIRECTED ADR PROGRAM
- ORDER GRANTING PLAINTIFF'S APPLICATION FOR LEAVE TO FILE UNDER SEAL CERTIFICATION AND NOTICE OF INTERESTED PARTIES

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UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

SOUTHERN DIVISION

POLARIS INNOVATIONS LIMITED, an Irish limited company, Plaintiff, vs. KINGSTON TECHNOLOGY COMPANY, INC., a Delaware corporation, Defendant.	Case No. 8:16-cv-300 **COMPLAINT FOR PATENT INFRINGEMENT AND DEMAND FOR JURY TRIAL**

Plaintiff Polaris Innovations Limited ("Polaris" or "Plaintiff") hereby alleges for its Complaint against Defendant Kingston Technology Company, Inc. ("Kingston" or "Defendant") as follows:

JURISDICTION

1. This is an action for patent infringement arising under the patent laws of the United States, Title 35 of the United States Code. This Court has subject matter jurisdiction of this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

2. This Court has personal jurisdiction over Kingston. Kingston is headquartered in the Central District of California, has systematic and continuous contacts with the forum, and conducts substantial business within this district. Upon information and belief, Kingston has committed and continues to commit acts of patent infringement, including making, selling, offering to sell, directly or through intermediaries, subsidiaries and/or agents, infringing products within this district, including to customers in this district.

VENUE

3. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391 and 1400(b) because Kingston is subject to personal jurisdiction in this district, and because a substantial part of the events giving rise to Polaris's claims occurred in this district, and Kingston, which is headquartered in Fountain Valley, California, has a regular and established place of business within this district.

THE PARTIES

4. Polaris Innovations Limited is a corporation organized and existing under the laws of Ireland, with its principal place of business at Polaris Innovations Limited, 29 Earlsfort Terrace, Dublin 2, Republic of Ireland.

5. On information and belief, Kingston Technology Company, Inc. is a corporation organized and existing under the laws of Delaware with its principal place of business at 17600 Newhope Street, Fountain Valley, California, 92708.

NATURE OF THE ACTION

6. This is a patent infringement action by Polaris to end Kingston's unauthorized, willful, and infringing manufacture, use, sale, offering for sale, and/or importation of products and methods incorporating Polaris's patented inventions.

7. Polaris holds all substantial rights and interest in the Asserted Patents described below, including the exclusive right to sue Kingston for infringement and recover damages.

8. Kingston makes, uses, sells, offers for sale, and imports products and methods that infringe the Asserted Patents. Polaris seeks monetary damages and prejudgment interest for Kingston's past and ongoing infringement of the Asserted Patents.

THE ASSERTED PATENTS

9. On December 5, 2000, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 6,157,589 ("the 589 Patent"), entitled "Dynamic semiconductor memory device and method for initializing a dynamic semiconductor memory device." A copy of the 589 Patent is attached hereto as Ex. 1.

10. Polaris owns all substantial right, title, and interest in the 589 Patent, and holds the right to sue and recover damages for infringement thereof, including past infringement.

11. On August 20, 2002, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 6,438,057 B1 ("the 057 Patent"), entitled "DRAM refresh timing adjustment device, system and method." A copy of the 057 Patent is attached hereto as Ex. 2.

12. Polaris owns all substantial right, title, and interest in the 057 Patent, and holds the right to sue and recover damages for infringement thereof, including past infringement.

13. On February 1, 2005, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 6,850,414 B2 ("the 414 Patent"), entitled "Electronic printed circuit board having a plurality of identically designed, housing-encapsulated semiconductor memories." A copy of the 414 Patent is attached hereto as Ex. 3.

14. Polaris owns all substantial right, title, and interest in the 414 Patent, and holds the right to sue and recover damages for infringement thereof, including past infringement.

15. On April 17, 2007, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 7,206,978 B2 ("the 978 Patent"), entitled "Error detection in a circuit module." A copy of the 978 Patent is attached hereto as Ex. 4.

16. Polaris owns all substantial right, title, and interest in the 978 Patent, and holds the right to sue and recover damages for infringement thereof, including past infringement.

17. On January 1, 2008, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 7,315,454 B2 ("the 454 Patent"), entitled "Semiconductor memory module." A copy of the 454 Patent is attached hereto as Ex. 5.

18. Polaris owns all substantial right, title, and interest in the 454 Patent, and holds the right to sue and recover damages for infringement thereof, including past infringement.

19. On February 19, 2008, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 7,334,150 B2 ("the 150 Patent"), entitled "Memory module with a clock signal regeneration circuit and a register circuit for temporarily storing the incoming command and address signals." A copy of the 150 Patent is attached hereto as Ex. 6.

20. Polaris owns all substantial right, title, and interest in the 150 Patent,

and holds the right to sue and recover damages for infringement thereof, including past infringement.

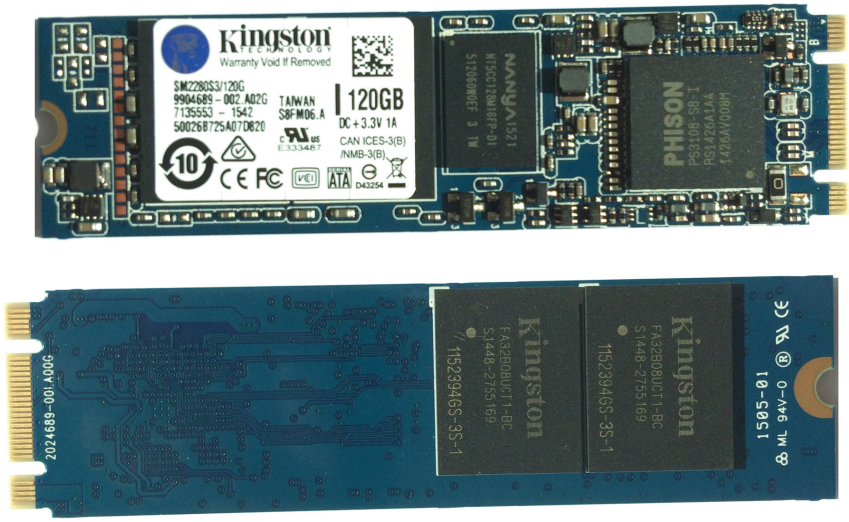
COUNT I:

INFRINGEMENT OF U.S. PATENT NO. 6,157,589

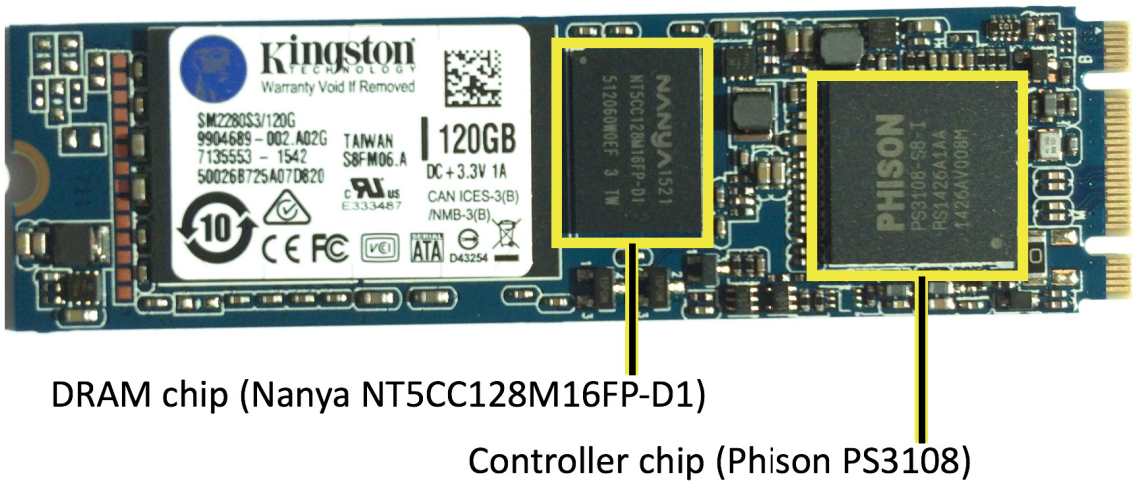
21. Polaris incorporates and realleges paragraphs 1-20 above as if fully set forth herein.

22. On information and belief, Kingston has willfully infringed and continues to willfully infringe one or more claims of the 589 Patent, including, but not limited to, Claims 11 and 12, pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, selling, offering to sell in the United States without authority, and/or importing into the United States without authority, solid-state drives (SSDs) performing the claimed methods for initializing a dynamic semiconductor memory device. These products, the "589 Patent Infringing Products," including by way of a non-limiting example only, Kingston's SSDs with model number SM2280S3/120G, perform the methods for initializing a dynamic semiconductor memory device as required by the claims of the 589 Patent.

23. By way of example, the front and back views of a representative 589 Patent Infringing Product (SM2280S3/120G) that performs the claimed methods are shown in the image below.



24. The front image of this representative 589 Infringing Product (SM2280S3/120G) is annotated below for illustration.



Specifically, the 589 Patent Infringing Products, such as SM2280S3/120G, include a dynamic random access memory (DRAM) chip (labeled Nanya NT5CC128M16FP in the photo above) and a controller chip (labeled Phison PS3108 in the photo above). *See generally* 2Gb DDR3 SDRAM H-Die datasheet, Nanya Technology ("Nanya Datasheet"), *available at* http://www.nanya.com/NanyaAdmin/GetFiles.ashx?ID=1199 (last visited February 3, 2016). On information and belief, when Kingston, its customers, and other third parties turn on the 589 Patent Infringing Products, the controller chip supplies, via an initialization circuit, a supply voltage stable signal (for example, the Active Low Asynchronous Reset signal, $\overline{RESET}$, *see* Nanya Datasheet at 8) once a supply voltage has been stabilized (for example, at the time labeled Tb, *see* Nanya Datasheet, Fig. 3 at 13, and as described in Step 1 of the initialization sequence, Nanya Datasheet at 11) after the switching-on operation of the dynamic semiconductor memory device (for example, in the "Reset Procedure" state which follows the "Power ON" state, Nanya Datasheet, Fig. 2 at 10). The controller chip also supplies, via an enable circuit of the initialization circuit, an enable signal (for

example, the Clock Enable signal, CKE, Nanya Datasheet, Table 3 at 7, which the DRAM waits for as described in Step 2 of the initialization sequence, Nanya Datasheet at 11), the initialization circuit receiving the supply voltage stable signal (for example, as described in Step 2 of the Reset and Initialization Procedure, Nanya Datasheet at 11) and further command signals (for example, the "Command" signals, Nanya Datasheet, Fig. 3 at 13) externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals (for example, the Mode Register Set ("MRS") and/or ZQ Calibration ("ZQCL") commands issued in Steps 6-10 of the initialization sequence, Nanya Datasheet at 12-14) the enable signal being generated (for example, as shown on the CKE line, Nanya Datasheet, Fig. 3 at 13, and as described in Step 3 of the initialization sequence, Nanya Datasheet at 11) and effecting an unlatching of a control circuit (for example, the control circuits contained in the DRAM chip which prepare the SDRAM for receiving valid commands during normal operation as described in Steps 10 and 12 of the initialization sequence, Nanya Datasheet at 12) provided for a proper operation of the dynamic semiconductor memory device. *See id.*

25. On information and belief, the controller provides at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal as the further command signals (for example, the MRS command, which acts both as a preparation command signal and as a loading configuration register command signal, *see* Nanya Datasheet at 12-14).

26. On information and belief, Kingston has induced and continues to induce infringement of one or more claims of the 589 Patent, including, but not limited to, Claims 11 and 12, pursuant to 35 U.S.C. § 271(b), by encouraging its customers and other third parties to perform the claimed method for initializing a dynamic semiconductor memory device. This performance of the claimed method

for initializing a dynamic semiconductor memory device, constitutes infringement, literally or under the doctrine of equivalents, of one or more claims of the 589 Patent by such customers or third parties. Kingston's acts of inducement include: providing its customers with the 589 Patent Infringing Products and intending its customers to use the 589 Infringing Products with hardware, software, and other infrastructure that enable and/or make use of these products; advertising these products through its own and third-party websites (for example, http://www.kingston.com/ssd); encouraging customers and other third parties to communicate directly with Kingston representatives about these products (for example, through the "Ask an Expert" feature on its website); and providing instructions on how to use these products. For example, Kingston's documentation supplied with the representative 589 Patent Infringing Product instructs users to install the product in a computer system and restart the computer system, and thus to perform the claimed methods. *See* Kingston Technology SSDNow Series Solid State Drive Getting Started, No. 4402105-001.B00, *available at* http://media.kingston.com/support/downloads/SSD_mSATA_Installguide.pdf (last visited on February 3, 2016).

27. Kingston proceeded in this manner despite its actual knowledge of the 589 Patent and its knowledge that the specific actions it actively induced on the part of its customers and other third parties constitute infringement of the 589 Patent at least as of February 1, 2016 when Polaris placed Kingston on notice of infringement of the 589 Patent and identified Kingston's infringing products. At the very least, because Kingston has been and remains on notice of the 589 Patent and the accused infringement, it has been and remains willfully blind regarding the infringement it has induced and continues to induce.

28. On information and belief, Kingston has contributed to and continues to contribute to infringement of one or more claims of the 589 Patent, including, but not limited to, Claims 11 and 12, pursuant to 35 U.S.C. § 271(c) by, without

authority, selling and/or offering to sell within the United States, importing, and/or supplying components of systems that perform the claimed methods for initializing a dynamic semiconductor memory device, including without limitation the 589 Patent Infringing Products. These components supplied by Kingston are key components to building computer systems such as laptops or desktop computers. When, for example, these products are installed on a computing device and used for storage, the claimed dynamic semiconductor memory device is used, and/or the claimed methods performed, thereby infringing, literally or under the doctrine of equivalents, one or more claims of the 589 Patent. Kingston supplied and continues to supply these components, including without limitation the 589 Patent Infringing Products, with the knowledge of the 589 Patent and with the knowledge that these components constitute material parts of the claimed inventions of the 589 Patent. Kingston knows that these components are especially made and/or especially adapted for use as claimed in the 589 Patent. Further, Kingston knows that there is no substantial non-infringing use of these components.

29. Polaris has suffered damages as a result of Kingston's infringement of the 589 Patent.

30. Kingston's infringement of the 589 Patent has been and continues to be willful, deliberate, and in disregard of Polaris's patent rights. At least as of February 1, 2016, when Polaris placed Kingston on notice of infringement of the 589 Patent and identified Kingston's infringing products, Kingston has had actual knowledge of infringement of the 589 Patent and has proceeded to infringe the 589 Patent with full and complete knowledge of that patent and its applicability to Kingston's products without taking a license under the 589 Patent. Despite knowledge of the 589 Patent, Kingston has acted and is acting despite an objectively high likelihood that its actions constitute patent infringement. This objective risk was and is known to Kingston, and is also so obvious that it should have been known to Kingston. Such willful and deliberate conduct entitles Polaris

to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

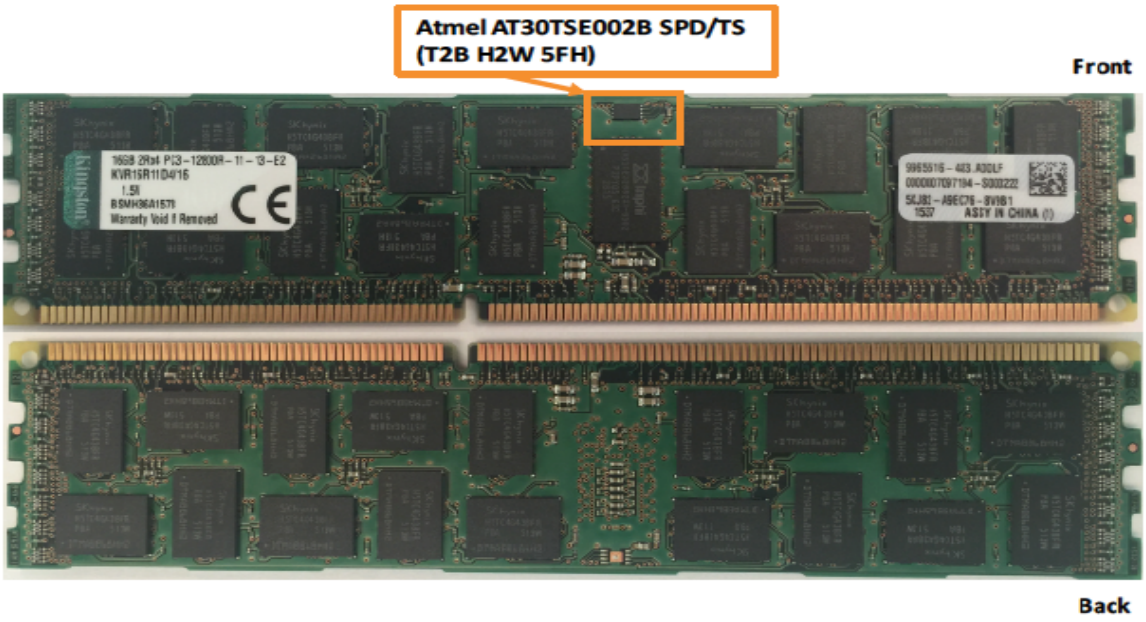
COUNT II:

INFRINGEMENT OF U.S. PATENT NO. 6,438,057

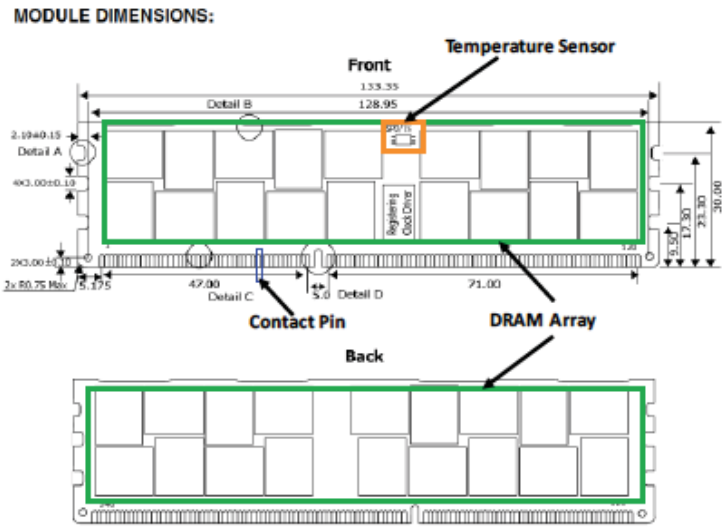
31. Polaris incorporates and realleges paragraphs 1-20 above as if fully set forth herein.

32. On information and belief, Kingston has willfully infringed and continues to willfully infringe one or more claims of the 057 Patent, including, but not limited to, Claims 1 and 2, pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, selling, and/or offering to sell in the United States without authority and/or importing into the United States without authority, Double Data Rate 3 (DDR3) Dual In-line Memory Module (DIMM) products, devices, systems, and/or components of systems that support the Extended Temperature Range (85°C to 95°C). These products, the "057 Patent Infringing Products," including by way of a non-limiting example only, Kingston's memory module product with model number KVR16R11D4/16, include the temperature-based refresh rate adjustment required by the claims of the 057 Patent.

33. By way of example, the front and back views of a representative 057 Patent Infringing Product (KVR16R11D4/16) that uses the claimed temperature-based refresh rate adjustment are shown in the image below.



34. The schematic diagram of this representative 057 Infringing Product (KVR16R11D4/16) is reproduced from publicly available Kingston documentation and annotated below for illustration.



Kingston Value RAM Memory Module Specifications, Doc. No. VALUERAM1123-001.A00 (Apr. 25, 2012) ("KVR16R11D4/16 Datasheet") at 2, *available at* http://www.kingston.com/dataSheets/KVR16R11D4_16.pdf (last visited February 3, 2016) (annotations added). Specifically, the 057 Patent Infringing Products, such as KVR16R11D4/16, are apparatuses comprising a

semiconductor package of the memory module including at least one contact pin (one example shown in the blue box in the diagram above) and at least one dynamic random access memory (DRAM) array comprising one or more DRAM chips (shown in the green box in the diagram above), such as "DDR3-1600 CL11 SDRAM" in KVR16R11D4/16, *see* KVR16R11D4/16 Datasheet at 1. On information and belief, all 057 Patent Infringing Products that support the Extended Temperature Range comprise at least one temperature sensor (an example shown in the orange box above) in thermal communication with the DRAM array, operable to produce a signal indicative of a temperature of the DRAM array or the equivalent, and coupled to at least one connection pin such that the signal may be provided to external circuitry. For example, the representative 057 Patent Infringing Product (KVR16R11D4/16) comprises an Atmel AT30TSE002B integrated temperature sensor with SEEPROM (annotated in the product image above). *See* AT30TSE002B Integrated Temperature Sensor with SEEPROM datasheet ("Atmel Datasheet") at 1, *available at* http://www.atmel.com/images/doc8711.pdf (last visited February 3, 2016). This AT30TSE002B temperature sensor is in thermal communication with the DRAM array, operable to produce a signal indicative of a temperature of the DRAM array (for example, the Temperature Alert signal output by the EVENT pin) or the equivalent, and coupled to at least one connection pin (for example, the EVENT pin), such that the signal may be provided to external circuitry (for example, the controller). *See* Atmel Datasheet at 1-4, 11, 16-18. Further, the DRAM array on the 057 Infringing Products is refreshed at a rate that decreases as the temperature of the DRAM array decreases and that increases as the temperature of the DRAM array increases. *See*, *e.g.*, KVR16R11D4/16 Datasheet at 1 ("Average Refresh Period 7.8µs at lower than TCASE 85ºC, 3.9µs at 85ºC < TCASE ≤ 95ºC").

35. On information and belief, at least one temperature sensor of one or more of the 057 Infringing Products includes at least one diode having a forward

voltage drop that varies as a function of the temperature of the DRAM array, and the signal corresponds to the forward voltage drop of the at least one diode. *See*, *e.g.*, Atmel Datasheet at 3 ("Band Gap Temperature Sensor") and 11 ("a band gap type temperature sensor").

36. On information and belief, Kingston has induced and continues to induce infringement of one or more claims of the 057 Patent, including, but not limited to, Claims 1, 2, 6, 7, 8, 9, 10, 11, 13, 14, 15, 16, and 17, pursuant to 35 U.S.C. § 271(b) by inducing its customers and other third parties to make, use, sell, offer to sell, import into the United States without authorization infringing products that comprise an 057 Infringing Product as described above and a refresh unit and/or chip performing the temperature-based refresh rate adjustment (the "057 Infringing Systems"), and by inducing its customers and other third parties to perform the claimed method of the temperature-based refresh rate adjustment. This making, using, selling, offering to sell, importing into the United States without authorization one or more of the 057 Infringing Systems, and performance of the claimed method constitute infringement, literally or under the doctrine of equivalents, of one or more claims of the 057 Patent by such customers or third parties as further explained below.

37. Specifically, on information and belief, the 057 Infringing Systems comprise one of the 057 Infringing Products, as described in the paragraph 34 *supra*, and a refresh unit (for example, a unit performing the temperature-based refresh rate adjustment in the controller, not shown in the images above) operable to refresh the DRAM array at a rate that varies in response to the signal (such as the Temperature Alert signal output by the EVENT pin). *See*, *e.g.*, KVR16R11D4/16 Datasheet at 1 ("Average Refresh Period 7.8µs at lower than TCASE 85ºC, 3.9µs at 85ºC < TCASE ≤ 95ºC").

38. On information and belief, such refresh unit of the 057 Infringing Systems further includes a refresh timing unit operable to establish the rate at

which the DRAM array is refreshed in response to the signal (such as the Temperature Alert signal output by the EVENT pin). *Id.*

39. On information and belief, such refresh timing unit of one or more of the 057 Infringing Systems further includes a refresh timing unit operable to decrease the rate at which the DRAM array is refreshed as the signal (such as the Temperature Alert signal output by the EVENT pin) indicates that the temperature of the DRAM array decreases. *Id.*

40. On information and belief, such refresh timing unit of one or more of the 057 Infringing Systems further includes a refresh timing unit operable to increase the rate at which the DRAM array is refreshed as the signal (such as the Temperature Alert signal output by the EVENT pin) indicates that the temperature of the DRAM array increases. *Id.*

41. On information and belief, at least one temperature sensor of one or more of the 057 Infringing Systems further includes at least one diode having a forward voltage drop that varies as a function of the temperature of the DRAM array, and the signal corresponds to the forward voltage drop of the at least one diode. *See*, *e.g.*, Atmel Datasheet at 3 ("Band Gap Temperature Sensor") and 11 ("a band gap type temperature sensor").

42. On information and belief, the refresh unit of one or more of the 057 Infringing Systems is operable to sense the forward voltage drop of the diode to determine the temperature of the DRAM array. *Id*.

43. On information and belief, one or more of the 057 Infringing Systems comprise at least one DRAM chip including a DRAM array and at least one temperature sensor in thermal communication with the DRAM array, at least one temperature sensor being operable to produce a signal indicative of a temperature of the DRAM array; the DRAM chip further includes at least one connection pin operable to provide the signal to external circuitry. *See* paragraph 34 *supra*. Such 057 Infringing Systems further comprise at least one refresh chip (such as a chip in

the controller performing the temperature-based refresh rate adjustment, not shown in the images above) operable to refresh the DRAM array at a rate that varies in response to the signal, wherein the refresh chip is operable to (i) decrease the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array decreases; and (ii) increase the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array increases. *Id.*

44. On information and belief, at least one temperature sensor of the 057 Infringing Systems as described in paragraph 43 further includes at least one diode having a forward voltage drop that varies as a function of the temperature of the DRAM array, and the signal corresponds to the forward voltage drop of the at least one diode. *See*, *e.g.*, Atmel Datasheet at 3 ("Band Gap Temperature Sensor") and 11 ("a band gap type temperature sensor").

45. On information and belief, the refresh chip in the 057 Infringing Systems is operable to sense the forward voltage drop of the diode to determine the temperature of the DRAM array. *Id.*

46. On information and belief, Kingston's customers and other third parties perform the claimed method of temperature-based refresh rate adjustment by using the 057 Infringing System. Such method comprises sensing a temperature of a dynamic random access memory (DRAM) array; outputting a signal indicative of the temperature of the DRAM array to external circuitry; and refreshing contents of the DRAM array at a rate that (i) decreases as the temperature of the DRAM array decreases; and (ii) increases as the temperature of the DRAM array increases. *See* paragraphs 34 and 37 *supra*.

47. On information and belief, the steps of the claimed method performed by Kingston's customers and other third parties for sensing the temperature of the DRAM array also comprises sensing a forward voltage drop of a diode that is in thermal communication with the DRAM array. *See* paragraphs 35, 41, 42, 44 *supra*.

48. Kingston's acts of active inducement of direct infringement by its customers and other third parties include: providing its customers with the 057 Infringing Products and intending its customers to use these infringing memory module products with hardware and software and other infrastructure, including a controller that comprises a refresh unit and/or chip to make and use the 057 Infringing Systems; advertising its infringing memory module products through its own and third-party websites (for example, http://www.kingston.com/us/memory/search/MemoryType/Default.aspx?MemoryType=DIMM,3,,); encouraging customers and other third parties to communicate regarding these products directly with Kingston representatives (for example, through the "Ask an Expert" feature on its website); and providing its customers and other third parties with instructions on how to combine these infringing memory module products with hardware and software and other infrastructure to make and use the 057 Infringing System, and to perform the claimed method. For example, Kingston's user manual, supplied with the representative 057 Patent Infringing Product, instructs the users to install and use the product in a computer system, thus instructing the users to make and use the 057 Infringing System and enable the users to perform the claimed method. *See* Ex. 7, Kingston Technology Warranty and Installation Guide, Doc. 4402092-001.D00; *see also*, KVR16R11D4/16 Datasheet.

49. Kingston proceeded in this manner despite its actual knowledge of the 057 Patent and its knowledge that the specific actions it actively induced on the part of its customers and other third parties constitute infringement of the 057 Patent at least as of February 1, 2016, when Polaris placed Kingston on notice of infringement of the 057 Patent and identified Kingston's infringing products. At the very least, because Kingston has been and remains on notice of the 057 Patent and the accused infringement, it has been and remains willfully blind regarding the infringement it has induced and continues to induce.

50. On information and belief, Kingston has contributed to and continues to contribute to infringement of one or more claims of the 057 Patent, including, but not limited to, Claims 1, 2, 6, 7, 8, 9, 10, 11, 13, 14, 15, 16, and 17, pursuant to 35 U.S.C. § 271(c) by, without authority, selling, offering to sell within the United States, importing, and/or supplying components of the 057 Infringing Systems, and apparatuses for use in the claimed methods of the temperature-based refresh rate adjustment, including without limitation the 057 Patent Infringing Products. These components and apparatuses supplied by Kingston, including without limitation the 057 Patent Infringing Products, are key components for temperature-based refresh rate adjustment, thus constituting material parts of the claimed inventions of the 057 Patent. Kingston supplied and continues to supply these components and apparatuses, including without limitation the 057 Patent Infringing Products, with the knowledge of the 057 Patent and with the knowledge that these components constitute material parts of the claimed inventions of the 057 Patent. Kingston knows that these components and apparatuses are especially made and/or especially adapted for use as claimed in the 057 Patent to support the Extended Temperature Range (85°C to 95°C) of DDR3 memory module products. Further, Kingston knows that there is no substantial non-infringing use of these components for temperature-based refresh rate adjustment.

51. Polaris has suffered damages as a result of Kingston's infringement of the 057 Patent.

52. Kingston's infringement of the 057 Patent has been and continues to be willful, deliberate, and in disregard of Polaris's patent rights. At least as of February 1, 2016, when Polaris placed Kingston on notice of infringement of the 057 Patent and identified Kingston's infringing products, Kingston has had actual knowledge of infringement of the 057 Patent and has proceeded to infringe the 057 Patent with full and complete knowledge of that patent and its applicability to Kingston's products without taking a license under the 057 Patent. Despite

knowledge of the 057 Patent, Kingston has acted and is acting despite an objectively high likelihood that its actions constitute patent infringement. This objective risk was and is known to Kingston, and is also so obvious that it should have been known to Kingston. Such willful and deliberate conduct entitles Polaris to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

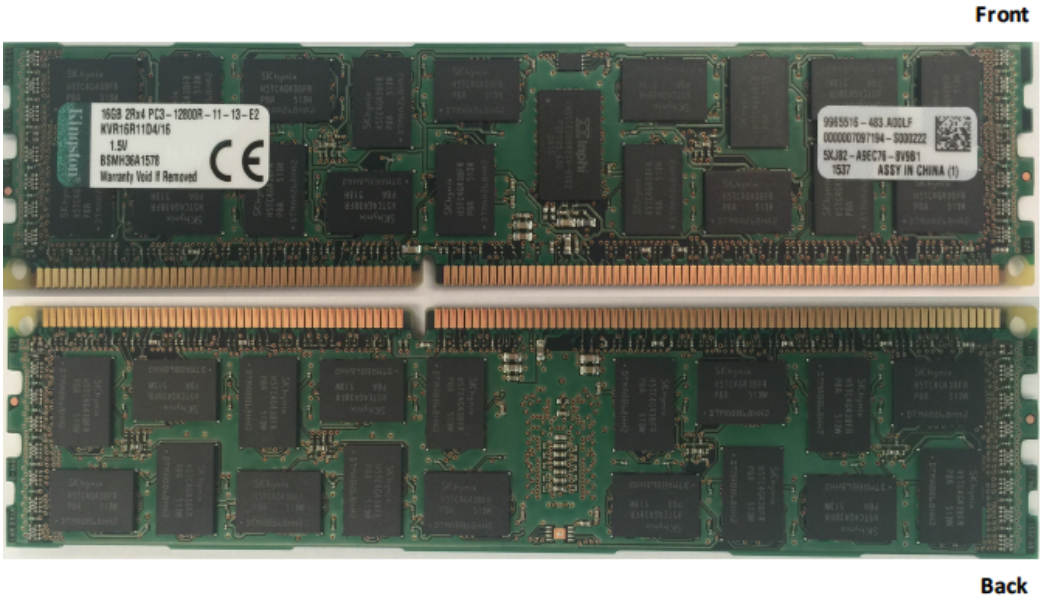
COUNT III:

INFRINGEMENT OF U.S. PATENT NO. 6,850,414

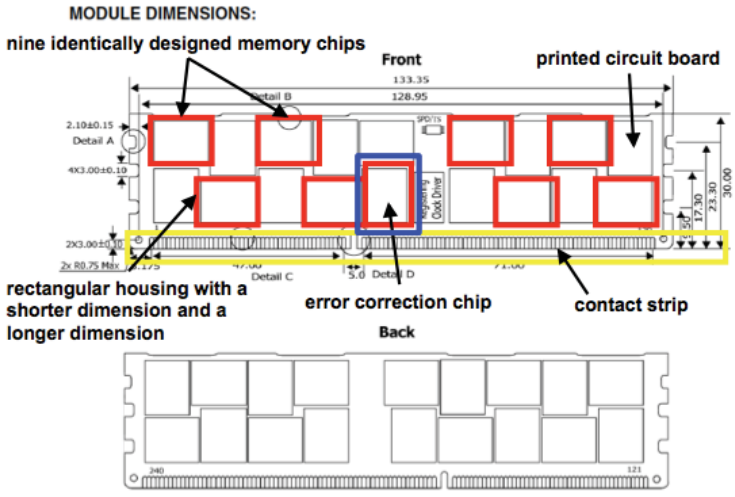
53. Polaris incorporates and realleges paragraphs 1-20 above as if fully set forth herein.

54. On information and belief, Kingston has willfully infringed and continues to willfully infringe one or more claims of the 414 Patent, including, but not limited to, Claims 1, 4, and 8, pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, selling, and/or offering to sell in the United States without authority and/or importing into the United States without authority, memory products, devices, systems, and/or components of systems that include the claimed arrangements and configurations of the memory chips (the "414 Patent Infringing Products"), including, for example, Kingston's memory module products with model number KVR16R11D4/16.

55. By way of example, the front and back views of a representative 414 Patent Infringing Product (KVR16R11D4/16) that uses the claimed arrangement and configuration of the memory chips are shown in the image below.



56. The schematic diagram of this representative 414 Infringing Product (KVR16R11D4/16) is reproduced from publicly available Kingston documentation and annotated below for illustration.



See KVR16R11D4/16 Datasheet at 2 (annotations added).

57. Specifically, the 414 Patent Infringing Products, such as KVR16R11D4/16, are memory modules having at least nine identical semiconductor memories (shown in red in the diagram above) that are encapsulated in rectangular housing with a shorter dimension and a longer

dimension, each of which are individually connected to an electronic printed circuit board, the front and back sides of which are illustrated above. The electronic printed circuit board has a contact strip (one example shown in the yellow box in the diagram above) for insertion into another electronic unit. One of the semiconductor memories is connected as an error correction chip (shown in blue above in the diagram above) with its housing being oriented perpendicular to the contact strip, while the longer dimensions of eight other semiconductor memories are oriented parallel with the contact strip. *See* KVR16R11D4/16 Datasheet at 2.

58. In addition, one or more of the 414 Patent Infringing Products has a height of 1 to 1.2 inches perpendicular to said contact strip. *See id*.

59. Further, one or more of the 414 Patent Infringing Products has a width of 5.25 inches. *See id*.

60. On information and belief, Kingston has induced and continues to induce infringement of one or more claims of the 414 Patent, including, but not limited to, Claims 1, 4, and 8, pursuant to 35 U.S.C. § 271(b) by inducing its customers and other third parties to use without authorization the infringing products that use the claimed arrangement and configuration of the memory chips, including but not limited to the 414 Patent Infringing Products. The use, without authorization, of the infringing products that comprise the claimed arrangement and configuration of the memory chips constitutes infringement, literally or under the doctrine of equivalents, of one or more claims of the 414 Patent by such customers or third parties. Kingston's acts of inducement include: providing its customers with the 414 Patent Infringing Products and intending its customers to use the 414 Infringing Products with hardware, software and other infrastructure that enable and/or make use of these products; advertising these products through its own and third-party websites (for example, http://www.kingston.com/us/memory/search/MemoryType/Default.aspx?Memory

Type=DIMM,3,,); encouraging customers and other third parties to communicate directly with Kingston representatives about these products (for example, through the "Ask an Expert" feature on its website); and providing instructions on how to use these products. For example, Kingston's documentation accompanying the representative 414 Patent Infringing Product provides the users with instructions on how to install the product in a computer system and enables the users to use the product. *See* Ex. 7, Kingston Technology Warranty and Installation Guide, Doc. 4402092-001.D00; *see also*, KVR16R11D4/16 Datasheet.

61. Kingston proceeded in this manner despite its actual knowledge of the 414 Patent and its knowledge that the specific actions it actively induced on the part of its customers and other third parties constitute infringement of the 414 Patent at least as of February 1, 2016 when Polaris placed Kingston on notice of infringement of the 414 Patent and identified Kingston's infringing products. At the very least, because Kingston has been and remains on notice of the 414 Patent and the accused infringement, it has been and remains willfully blind regarding the infringement it has induced and continues to induce.

62. Polaris has suffered damages as a result of Kingston's infringement of the 414 Patent.

63. Kingston's infringement has been and continues to be willful, deliberate and in disregard of Polaris's patent rights. At least as of February 1, 2016, when Polaris placed Kingston on notice of infringement of the 414 Patent and identified Kingston's infringing products, Kingston has had actual knowledge of infringement of the 414 Patent and has proceeded to infringe the 414 Patent with full and complete knowledge of that patent and its applicability to Kingston products without taking a license under the 414 Patent. Despite knowledge of the 414 Patent, Kingston has acted and is acting despite an objectively high likelihood that its actions constitute patent infringement. This objective risk was and is known to Kingston, and is also so obvious that it should have been known to Kingston.

Such willful and deliberate conduct entitles Polaris to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT IV:

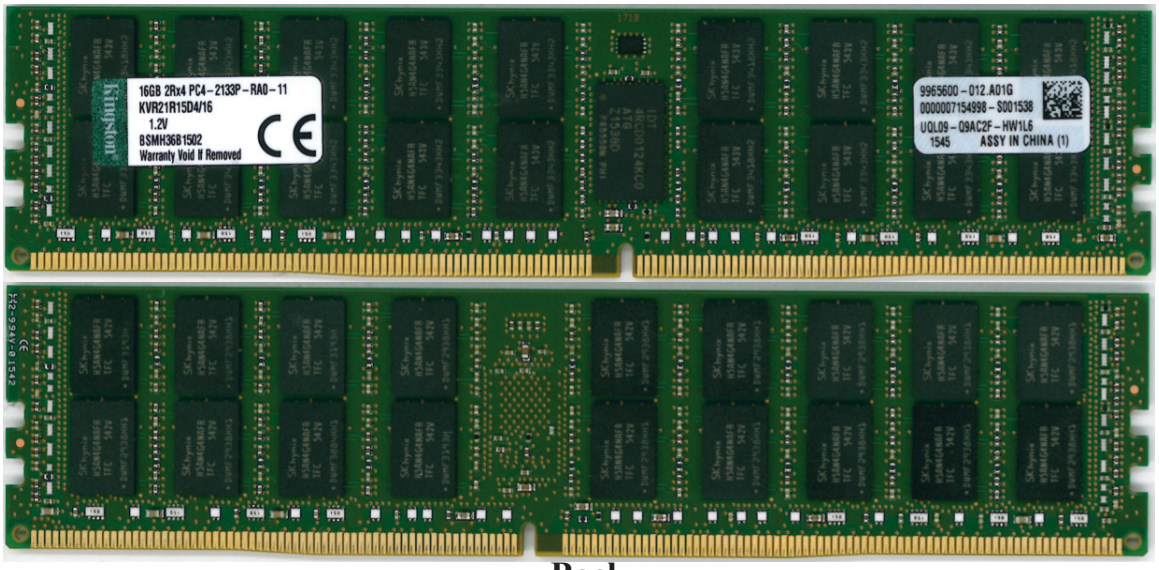
INFRINGEMENT OF U.S. PATENT NO. 7,206,978

64. Polaris incorporates and realleges paragraphs 1-20 above as if fully set forth herein.

65. On information and belief, Kingston has willfully infringed and continues to willfully infringe one or more claims of the 978 Patent, including, but not limited to, Claims 1, 2, 3, 5, 10, 11, and 12, pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, selling, and/or offering to sell in the United States and/or importing into the United States without authority, claimed memory module products, devices, systems, and/or components of systems (the "978 Patent Infringing Products"), including, for example, Kingston's memory module products with model number KVR21R15D4/16.

66. By way of example, the front and back views of a representative 978 Patent Infringing Product (KVR21R15D4/16) are shown in the image below.

Front



Back

67. The 978 Patent Infringing Products, such as KVR21R15D4/16, are circuit modules comprising a module board, the front and back sides of which are shown above. A plurality of circuit units, each consisting of a single integrated circuit memory chip, is arranged on the module board (in the above example, 36 integrated memory chips are arranged on the module board). *See*, *e.g.*, Kingston KVR21R15D4/16 16GB 2Rx4 2G x 72-Bit PC4-2133 CL15 Registered w/Parity 288-Pin DIMM Specification, Doc. No. VALUERAM1447-001.C00 (Feb. 24, 2015) ("KVR21R15D4/16 Datasheet") at 1, *available at* http://www.kingston.com/dataSheets/KVR21R15D4_16.pdf (last visited February 3, 2016). Further, on information and belief, the 978 Patent Infringing Products comprise a main bus having a plurality of lines, branching into a plurality of sub-buses having a plurality of lines, each of the sub-buses being connected to one of the plurality of the circuit units. Further, upon information and belief, each circuit unit (in the example above, each dynamic random access memory, or "DRAM," chip) in the 978 Patent Infringing Products comprises an indication signal generating unit for providing an indication signal based on a combination of the signals received on the plurality of lines of the sub-bus connected to the respective circuit unit (in the example above, each memory chip combines the PAR (command and address parity) input signal with the command and address input signals to determine whether there is an error and generate the appropriate indication signal). *See*, *e.g.*, KVR21R15D4/16 Datasheet at 1 ("CA parity (Command/Address Parity) mode is supported"). Each circuit unit also comprises an indication signal output for outputting the indication signal (in the example above, the ALERT_n pin on each memory chip).

68. In addition, one or more 978 Patent Infringing Products comprise means for providing a check signal to each of the circuit units, the structure of which is the same as or equivalent to that disclosed in the patent specification (in the example above, the PAR (command and address parity) input on each dynamic

random access memory chip). *See*, *e.g.*, KVR21R15D4/16 Datasheet at 1 ("CA parity (Command/Address Parity) mode is supported"). Upon information and belief, this indication signal generating unit generates said indication signal based on a combination of the signals on the plurality of lines of the respective sub-bus and the check signal so that the indication signal represents an error signal (in the example above, each memory chip combines the PAR input signal with the command and address input signals to determine whether there is an error and generate the appropriate indication signal).

69. In addition, on information and belief, one or more 978 Patent Infringing Products comprise an error reporting means, the structure of which is the same as or equivalent to that disclosed in the patent specification, being connected to the indication signal outputs of the circuit units, and wherein each error reporting means is configured to drive a module error out signal (in the example above, the ALERT_n outputs are connected to each other by traces on the printed circuit board, and buffered by a register, they drive the ALERT_n signal for the entire module). *See*, *e.g.*, KVR21R15D4/16 Datasheet at 1 ("CA parity (Command/Address Parity) mode is supported").

70. In addition, on information and belief, one or more 978 Patent Infringing Products comprise an indication reporting means, the structure of which is the same as or equivalent to that disclosed in the patent specification, being connected to the indication signal outputs of the circuit units and wherein each indication reporting means is configured to drive a module indication out signal (in the example above, the ALERT_n outputs are connected to each other by traces on the printed circuit board, and buffered by a register, they drive the ALERT_n signal for the entire module).

71. In addition, on information and belief, one or more 978 Patent Infringing Products comprise a DIMM, wherein the circuit units are memory units, wherein the main bus is a memory main bus, and the sub-busses are memory sub-

buses (in the example above, the module is a DIMM, the circuit units are DRAM memory chips and the traces providing address and command signals to the memory chips form a memory main bus and memory sub-buses). *See*, *e.g.*, KVR21R15D4/16 Datasheet at 1.

72. In addition, on information and belief, one or more 978 Patent Infringing Products comprise a main bus that is a command/address bus (in the example above, the traces providing address and command signals to the dynamic random access memory chips form a memory main bus and memory sub-buses).

73. In addition, on information and belief, one or more 978 Patent Infringing Products comprise means for providing a check signal that is a parity signal, the structure of which is the same as or equivalent to that disclosed in the patent specification (in the example above, the PAR input on each dynamic random access memory chip receives a parity signal from the module board).

74. On information and belief, Kingston has induced and continues to induce infringement of one or more claims of the 978 Patent, including, but not limited to, Claims 1, 2, 3, 5, 10, 11, and 12, pursuant to 35 U.S.C. § 271(b) by inducing its customers and other third parties to use without authorization the infringing products comprising the claimed arrangement of circuit units, including but not limited to the 978 Patent Infringing Products. This use, without authorization, of the infringing products comprising the claimed arrangement of circuit units constitutes infringement, literally or under the doctrine of equivalents, of one or more claims of the 978 Patent by such customers or third parties. Kingston's acts of inducement include: providing its customers with the 978 Patent Infringing Products and intending its customers to use the 978 Infringing Products with hardware, software, and other infrastructure that enable and/or make use of these products; advertising these products through its own and third-party websites (for example, http://www.kingston.com/us/memory/search/MemoryType/Default.aspx?MemoryType=DIMM,3,,); encouraging customers and other third

parties to communicate directly with Kingston representatives about these products (for example, through the "Ask an Expert" feature on its website); and providing instructions on how to use these products. For example, Kingston's documentation accompanying the representative 978 Patent Infringing Product provides the users with instructions on how to install the product in a computer system and enables the users to use the product. *See* Ex. 7, Kingston Technology Warranty and Installation Guide, Doc. 4402092-001.D00; *see also*, KVR21R15D4/16 Datasheet.

75. Kingston proceeded in this manner despite its actual knowledge of the 978 Patent and its knowledge that the specific actions it actively induced on the part of its customers and other third parties constitute infringement of the 978 Patent at least as of February 1, 2016, when Polaris placed Kingston on notice of infringement of the 978 Patent and identified Kingston's infringing products. At the very least, because Kingston has been and remains on notice of the 978 Patent and the accused infringement, it has been and remains willfully blind regarding the infringement it has induced and continues to induce.

76. Polaris has suffered damages as a result of Kingston's infringement of the 978 Patent.

77. Kingston's infringement of the 978 Patent has been and continues to be willful, deliberate, and in disregard of Polaris's patent rights. At least as of February 1, 2016, when Polaris placed Kingston on notice of infringement of the 978 Patent and identified Kingston's infringing products, Kingston has had actual knowledge of infringement of the 978 Patent and has proceeded to infringe the 978 Patent with full and complete knowledge of that patent and its applicability to Kingston's products without taking a license under the 978 Patent. Despite knowledge of the 978 Patent, Kingston has acted and is acting despite an objectively high likelihood that its actions constitute patent infringement. This objective risk was and is known to Kingston, and is also so obvious that it should have been known to Kingston. Such willful and deliberate conduct entitles Polaris

to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

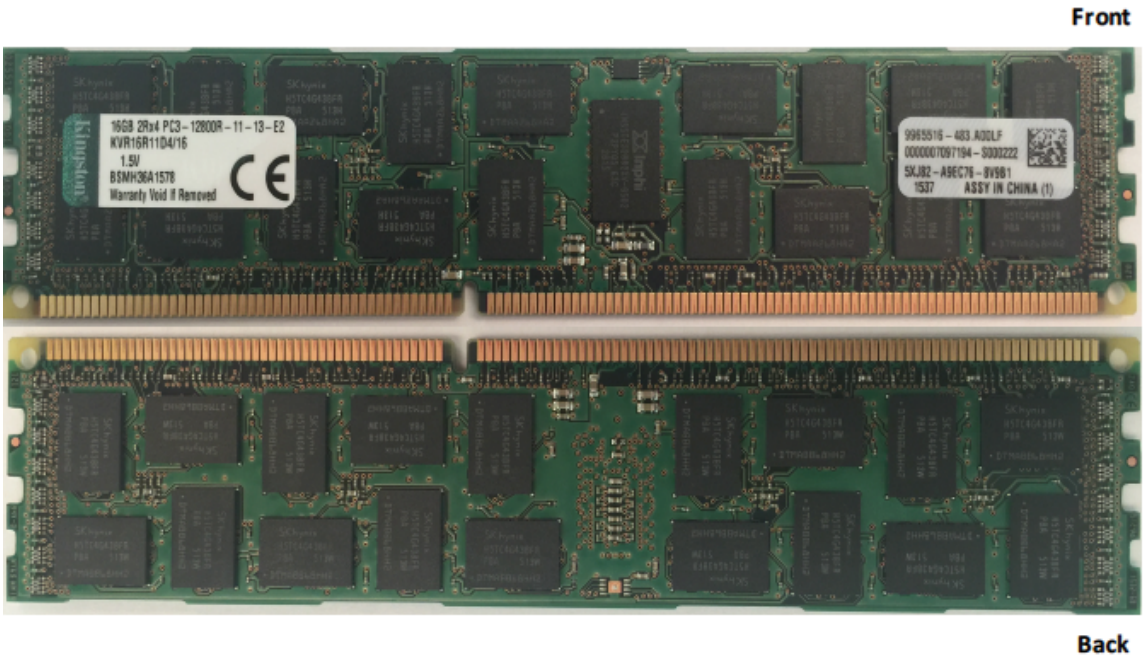
COUNT V:

INFRINGEMENT OF U.S. PATENT NO. 7,315,454

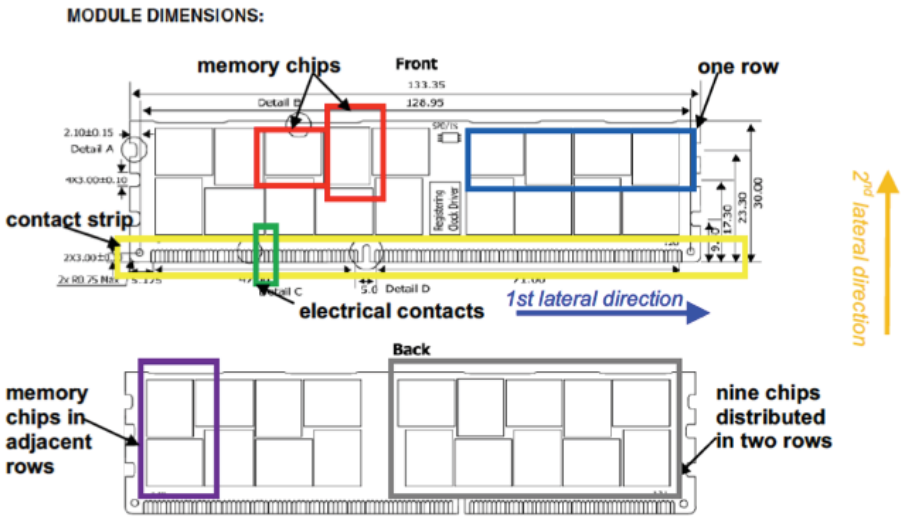
78. Polaris incorporates and realleges paragraphs 1-20 above as if fully set forth herein.

79. On information and belief, Kingston has willfully infringed and continues to willfully infringe one or more claims of the 454 Patent, including, but not limited to, Claims 1, 2, 3, 4, and 7, pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, selling, and/or offering to sell in the United States and/or importing into the United States without authority, memory module products, devices, systems, and/or components of systems that include the claimed arrangements and configurations of the memory chips (the "454 Patent Infringing Products"), including, for example, Kingston's memory module products with model number KVR16R11D4/16.

80. By way of example, the front and back views of a representative 454 Patent Infringing Product (KVR16R11D4/16) that uses the claimed arrangement and configuration of the memory chips are shown in the image below.



81. The schematic diagram of this representative 454 Patent Infringing Product (KVR16R11D4/16) is reproduced from publicly available Kingston documentation and annotated below for illustration.



See KVR16R11D4/16 Datasheet at 2 (annotations added). Specifically, the 454 Patent Infringing Products, such as KVR16R11D4/16, are semiconductor memory modules comprising an electronic printed circuit board, the front and back sides of

which are illustrated above. The electronic printed circuit board has a contact strip (one example shown in the yellow box) that extends at a first edge (for example, the bottom edge) of the printed circuit board along with a first lateral direction and a plurality of electrical contacts (a few shown in the green box as examples) disposed along the first lateral direction between two second edges (left and right edges) that extend in a second lateral direction that is perpendicular to the first lateral direction. The 454 Patent Infringing Products further comprise a plurality of semiconductor memory chips (two exemplary chips are shown in the red boxes) of substantially identical type, such as "DDR3-1600 CL11 SDRAM" in KVR16R11D4/16, *see* KVR16R11D4/16 Datasheet at 1, mounted on at least one external area (the front and/or back sides) of the printed circuit board and having a rectangular form with a shorter dimension and a longer dimension in a direction perpendicular to the shorter dimension. The memory chips are arranged in at least two rows, each row (one exemplary row shown in blue box) extending in the first lateral direction between a center of the printed circuit board and the left or right edge, wherein the memory chips in each row are arranged in an alternating sequence of opposite orientation with the longer dimension of each memory chip being parallel with the shorter dimension of adjacent memory chips in the same row. The memory chips aligned in the second lateral direction and lying in respective adjacent rows (one group of such chips shown in the purple box) have opposite orientations.

82. In addition, one or more 454 Patent Infringing Products include four semiconductor memory chips (one example shown in the blue box) that are mounted in a row on one external area (such as the front side) of the printed circuit board.

83. Further, one or more 454 Patent Infringing Products include nine chips (one example shown in the grey box) that are distributed between two rows arranged in a manner lying one adjacent to another in the second lateral direction.

84. Further, on information and belief, one or more 454 Patent Infringing Products comprise a branching separate line bus comprising a first branch and a second branch, wherein the memory chips mounted on the external area (the front and/or back sides) between the center and the respective second edge (left or right edge) of the printed circuit are connected by the branching separate line bus, such that the memory chips of a first row are connected in series via line tracks of the first branch and the memory chips of a second row are connected in a series via line tracks of the second branch of the branch separate line bus, or the 454 Patent Infringing Products comprise the equivalent.

85. Further, the 454 Patent Infringing Products are standardized memory modules in compliance with a JEDEC standard. *See*, *e.g.*, KVR16R11D4/16 Datasheet at 1.

86. On information and belief, Kingston has induced and continues to induce infringement of one or more claims of the 454 Patent, including, but not limited to, Claims 1, 2, 3, 4, and 7, pursuant to 35 U.S.C. § 271(b) by inducing its customers and other third parties to use without authorization the infringing products comprising the claimed arrangements and configurations of the memory chips, including but not limited to the 454 Patent Infringing Products. This use, without authorization, of the infringing products comprising the claimed arrangements and configurations of the memory chips constitutes infringement, literally or under the doctrine of equivalents, of one or more claims of the 454 Patent by such customers or third parties. Kingston's acts of inducement include: providing its customers with the 454 Patent Infringing Products and intending its customers to use the 454 Infringing Products with hardware, software, and other infrastructure that enable and/or make use of these products; advertising these products through its own and third-party websites (for example, http://www.kingston.com/us/memory/search/MemoryType/Default.aspx?MemoryType=DIMM,3,,); encouraging customers and other third parties to communicate

directly with Kingston representatives about these products (for example, through the "Ask an Expert" feature on its website); and providing instructions on how to use these products. For example, Kingston's documentation accompanying the representative 454 Patent Infringing Product provides the users with instructions on how to install the product in a computer system and enables the users to use the product. *See* Ex. 7, Kingston Technology Warranty and Installation Guide, Doc. 4402092-001.D00; *see also*, KVR16R11D4/16 Datasheet.

87. Kingston proceeded in this manner despite its actual knowledge of the 454 Patent and its knowledge that the specific actions it actively induced on the part of its customers and other third parties constitute infringement of the 454 Patent at least as of February 1, 2016, when Polaris placed Kingston on notice of infringement of the 454 Patent and identified infringing Kingston's products. At the very least, because Kingston has been and remains on notice of the 454 Patent and the accused infringement, it has been and remains willfully blind regarding the infringement it has induced and continues to induce.

88. Polaris has suffered damages as a result of Kingston's infringement of the 454 Patent.

89. Kingston's infringement of the 454 Patent has been and continues to be willful, deliberate, and in disregard of Polaris's patent rights. At least as of February 1, 2016, when Polaris placed Kingston on notice of infringement of the 454 Patent and identified Kingston's infringing products, Kingston has had actual knowledge of infringement of the 454 Patent and has proceeded to infringe the 454 Patent with full and complete knowledge of that patent and its applicability to Kingston's products without taking a license under the 454 Patent. Despite knowledge of the 454 Patent, Kingston has acted and is acting despite an objectively high likelihood that its actions constitute patent infringement. This objective risk was and is known to Kingston, and is also so obvious that it should have been known to Kingston. Such willful and deliberate conduct entitles Polaris

to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

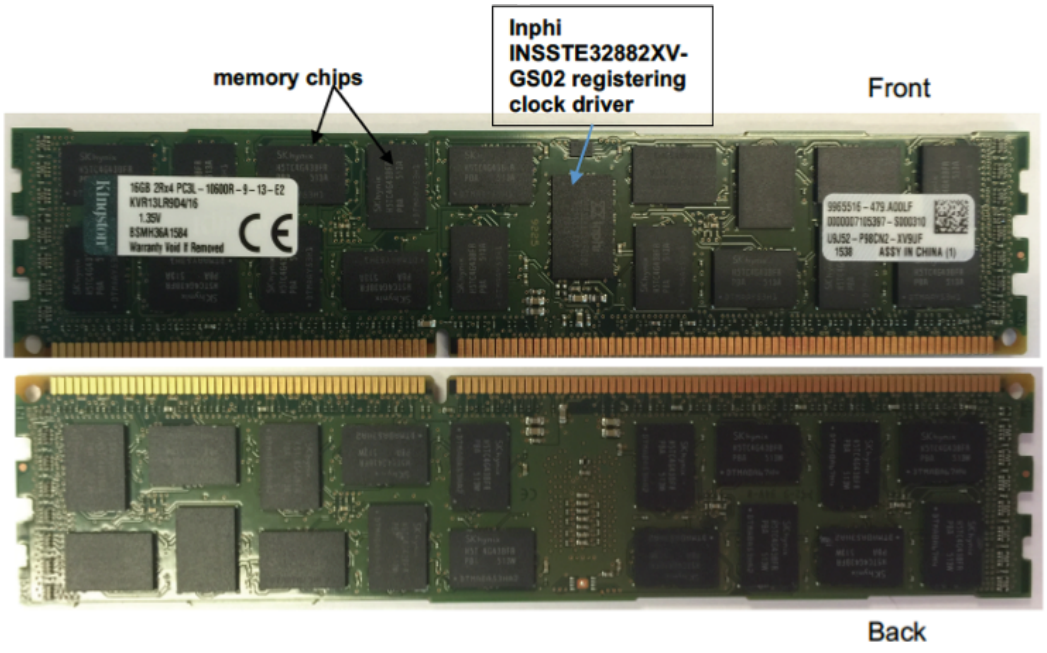
COUNT VI:

INFRINGEMENT OF U.S. PATENT NO. 7,334,150

90. Polaris incorporates and realleges paragraphs 1-20 above as if fully set forth herein.

91. On information and belief, Kingston has willfully infringed and continues to willfully infringe one or more claims of the 150 Patent, including, but not limited to, Claims 1, 2, 3, 5, 6, 8, 9, 10, and 11, pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, selling, and/or offering to sell in the United States and/or importing into the United States without authority, memory module products, devices, systems, and/or components of systems that included the claimed clock signal regeneration circuit and register circuit (the "150 Patent Infringing Products"), including without limitation, Kingston's memory module product with model number KVR13LR9D4/16.

92. By way of example, the front and back views of a representative 150 Patent Infringing Product (KVR13LR9D4/16) are shown in the image below.



93. Specifically, the 150 Patent Infringing Products, such as KVR13LR9D4/16, comprise a plurality of memory chips arranged on the memory module. On information and belief, the 150 Patent Infringing Products, such as KVR13LR9D4/16, comprise a plurality of bus signal lines operable to supply an incoming clock signal (for example, clock signals CK0_t, CK0_c) and incoming command and address signal (for example, address signals A[N:0]) to at least the memory chips. On information and belief, the 150 Patent Infringing Products further comprise a clock signal regeneration circuit (for example, a standard SSTE 32882 registering clock driver) configured to generate a plurality of copies of the incoming clock signal (for example, PCK0A_t, PCK0B_t, PCK_0A_c, PCK_0B_c) and to supply the copies of the incoming clock signal to the memory chip, where the copies of the incoming clock signal have the same frequency as the incoming clock signal. On information and belief, the 150 Patent Infringing Products further comprise a register circuit arranged on the memory module in a common chip packaging with the clock regeneration circuit. *See*, *e.g.*, Kingston Value RAM Memory Module Specifications, Doc. No. VALUERAM1223-001.B00 (Jan. 22, 2013) ("KVR13LR9D4/16 Datasheet") at 2 (the register and the clock driver are within the same chip), *available at* http://www.kingston.com/dataSheets/KVR13LR9D4_16.pdf (last visited February 3, 2016) (annotations added). For example, the representative 150 Patent Infringing Product KVR13LR9D4/16, comprises an Inphi INSSTE32882XV-GS02 registering clock driver chip (as annotated in the product image above), that includes both the clock regeneration circuit and the register circuit. *See* INSSTE32882XV datasheet ("Inphi Datasheet"), *available at* http://www.inphi.com/product_pdf_generator.php?prod_link=960 (last visited December 21, 2015). On information and belief, the register circuit in the 150 Infringing Products is configured to receive one of the copies of the incoming clock signal from the clock regeneration circuit. On information and belief, the

register circuit in the 150 Infringing Products is further configured to temporarily store the incoming command and address signals, and to generate a plurality of copies of the incoming command and address signals and to supply the copies of the incoming command and address signals to the memory chip, where the copies of the incoming command and address signals have the same frequency as the incoming command and address signals.

94. The clock signal regeneration circuit in the 150 Patent Infringing Product comprises a phase locked loop (PLL) circuit. *See*, *e.g.*, KVR13LR9D4/16 Datasheet at 1 ("Register/PLL used").

95. On information and belief, the incoming clock signal and the copies of incoming clock signals in the 150 Patent Infringing Products are each supplied via differential clock signal lines.

96. In addition, in the 150 Patent Infringing Products, the clock signal regeneration circuit and the register circuit are integrated on a common chip in the common chip packaging. *See*, *e.g.*, KVR13LR9D4/16 Datasheet at 2.

97. Further, the common chip packaging is arranged essentially at a central position on the exemplary 150 Patent Infringing Product (KVR13LR9D4/16) or is arranged equivalently. *See*, *e.g.*, KVR13LR9D4/16 Datasheet at 2.

98. On information and belief, the 150 Patent Infringing Products comprise a fly-by bus structure for the bus signal lines of the command and address signals or the equivalent. *See* John Nieto, *The Evolution from DDR2 to DDR3 and its Impact on Signal Integrity*, *available at* https://www.inphi.com/technology-overview/Evolution%20of%20DDR2%20to%20DDR3.pdf (last visited December 21, 2015).

99. On information and belief, the clock signal regeneration circuit and the register circuit in the 150 Patent Infringing Products respectively generate two copies of the clock signal and the command signals for distribution to the memory

chips.

100. On information and belief, one or more of the 150 Patent Infringing Products further comprise an RDIMM module. *See*, *e.g.*, KVR13LR9D4/16 Datasheet at 1 ("Registered w/Parity 240-Pin DIMM").

101. The 150 Patent Infringing Products further comprise DDR-DRAM memories. *See*, *e.g.*, KVR13LR9D4/16 Datasheet at 1 ("DDR3L-1333 CL9 SDRAM").

102. On information and belief, Kingston has induced and continues to induce infringement of one or more claims of the 150 Patent, including, but not limited to, Claims 1, 2, 3, 5, 6, 8, 9, 10, and 11, pursuant to 35 U.S.C. § 271(b) by inducing its customers and other third parties to use without authorization the infringing products comprising the claimed clock signal regeneration circuit and register circuit, including but not limited to the 150 Patent Infringing Products. This use, without authorization, of the infringing products comprising the claimed arrangements and configurations of the memory chips constitutes infringement, literally or under the doctrine of equivalents, of one or more claims of the 150 Patent by such customers or third parties. Kingston's acts of inducement include: providing its customers with the 150 Patent Infringing Products and intending its customers to use the 150 Infringing Products with hardware, software and other infrastructure that enable and/or make use of these products; advertising these products through its own and third-party websites (for example, http://www.kingston.com/us/memory/search/MemoryType/Default.aspx?MemoryType=DIMM,3,,); encouraging customers and other third parties to communicate directly with Kingston representatives about these products (for example, through the "Ask an Expert" feature on its website); and providing instructions on how to use these products. For example, Kingston's documentation accompanying the representative 150 Patent Infringing Product provides the users with instructions on how to install the product in a computer system and enables the users to use the

product. *See* Ex. 7, Kingston Technology Warranty and Installation Guide, Doc. 4402092-001.D00; *see also*, KVR13LR9D4/16 Datasheet.

103. Kingston proceeded in this manner despite its actual knowledge of the 150 Patent and its knowledge that the specific actions it actively induced on the part of its customers and other third parties constitute infringement of the 150 Patent at least as of February 1, 2016, when Polaris placed Kingston on notice of infringement of the 150 Patent and identified infringing Kingston's products. At the very least, because Kingston has been and remains on notice of the 150 Patent and the accused infringement, it has been and remains willfully blind regarding the infringement it has induced and continues to induce.

104. Polaris has suffered damages as a result of Kingston's infringement of the 150 Patent.

105. Kingston's infringement of the 150 Patent has been and continues to be willful, deliberate and in disregard of Polaris's patent rights. At least as of February 1, 2016, when Polaris placed Kingston on notice of infringement of the 150 Patent and identified Kingston's infringing products, Kingston has had actual knowledge of infringement of the 150 Patent and has proceeded to infringe the 150 Patent with full and complete knowledge of that patent and its applicability to Kingston's products without taking a license under the 150 Patent. Despite knowledge of the 150 Patent, Kingston has acted and is acting despite an objectively high likelihood that its actions constitute patent infringement. This objective risk was and is known to Kingston, and is also so obvious that it should have been known to Kingston. Such willful and deliberate conduct entitles Polaris to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

PRAYER FOR RELIEF

106. Polaris respectfully prays for relief as follows:

107. A judgment that Kingston has infringed and continues to infringe one

or more claims of the Asserted Patents;

108. A judgment that Kingston has willfully infringed one or more claims of the Asserted Patents;

109. A judgment awarding Polaris all damages adequate to compensate for Kingston's infringement, and in no event less than a reasonable royalty for Kingston's acts of infringement, including all pre-judgment and post-judgment interest at the maximum rate allowed by law;

110. A judgment awarding Polaris treble damages pursuant to 35 U.S.C. § 284 as a result of Kingston's willful conduct;

111. A judgment and order finding that this is an exceptional case within the meaning of 35 U.S.C. § 285 and awarding Polaris its reasonable attorneys fees and costs; and

112. A judgment awarding Polaris such other relief as the Court may deem just and equitable.

DEMAND FOR JURY TRIAL

113. Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, Polaris demands a trial by jury in this action.

Dated: February 19, 2016

Respectfully submitted,

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EXHIBIT 1

US006157589A

United States Patent [19]

Krause

[11] **Patent Number: 6,157,589**

[45] **Date of Patent: Dec. 5, 2000**

[54] **DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR INITIALIZING A DYNAMIC SEMICONDUCTOR MEMORY DEVICE**

[75] Inventor: **Gunnar Krause**, Munich, Germany

[73] Assignee: **Siemens Aktiengesellschaft**, Munich, Germany

[21] Appl. No.: **09/343,431**

[22] Filed: **Jun. 30, 1999**

[30] **Foreign Application Priority Data**

Jun. 30, 1998 [DE] Germany 198 29 287

[51] **Int. Cl.**[7] **G11C 8/00**

[52] **U.S. Cl.** **365/226**; 365/228

[58] **Field of Search** 365/226, 227, 365/228

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Primary Examiner—Vu A. Le

Attorney, Agent, or Firm—Herbert L. Lerner; Laurence A. Greenber; Werner H. Stemer

[57] **ABSTRACT**

A dynamic semiconductor memory device of a random access type has an initialization circuit that controls the switching-on operation of the semiconductor memory device and of its circuit components. The initialization circuit supplies a supply voltage stable signal once the supply voltage has been stabilized after the switching-on of the semiconductor memory device. The initialization circuit has an enable circuit that receives the supply voltage stable signal and further command signals externally applied to the semiconductor memory device. The enable circuit supplies an enable signal after a predetermined proper initialization sequence of the command signals applied to the semiconductor memory device is identified. The enable signal effects the unlatching of a control circuit provided for the proper operation of the semiconductor memory device.

13 Claims, 3 Drawing Sheets

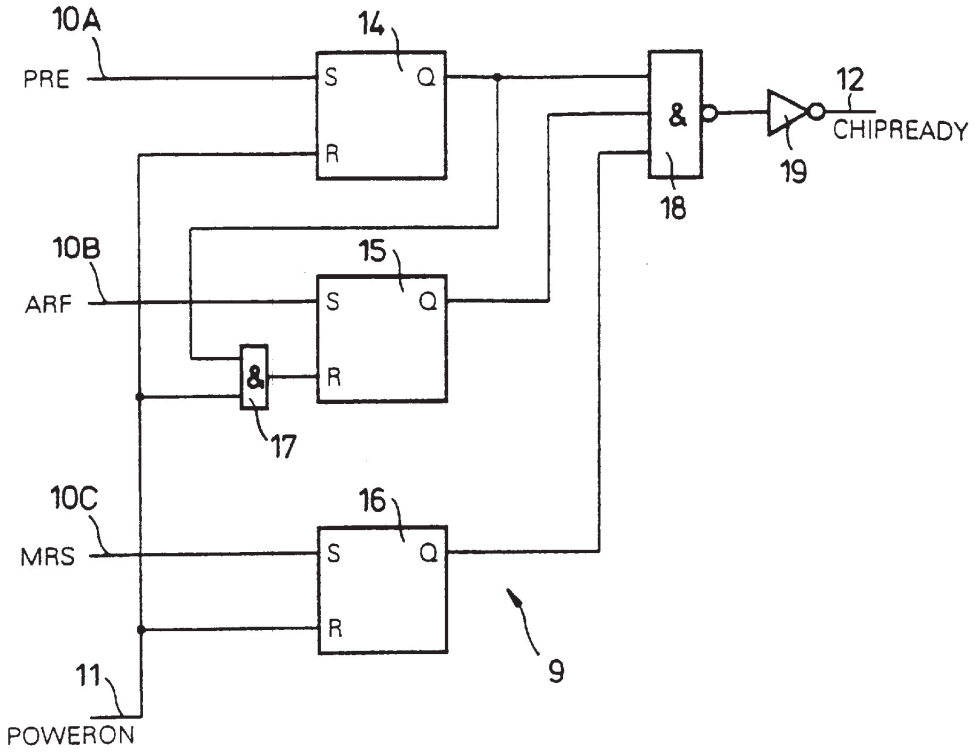
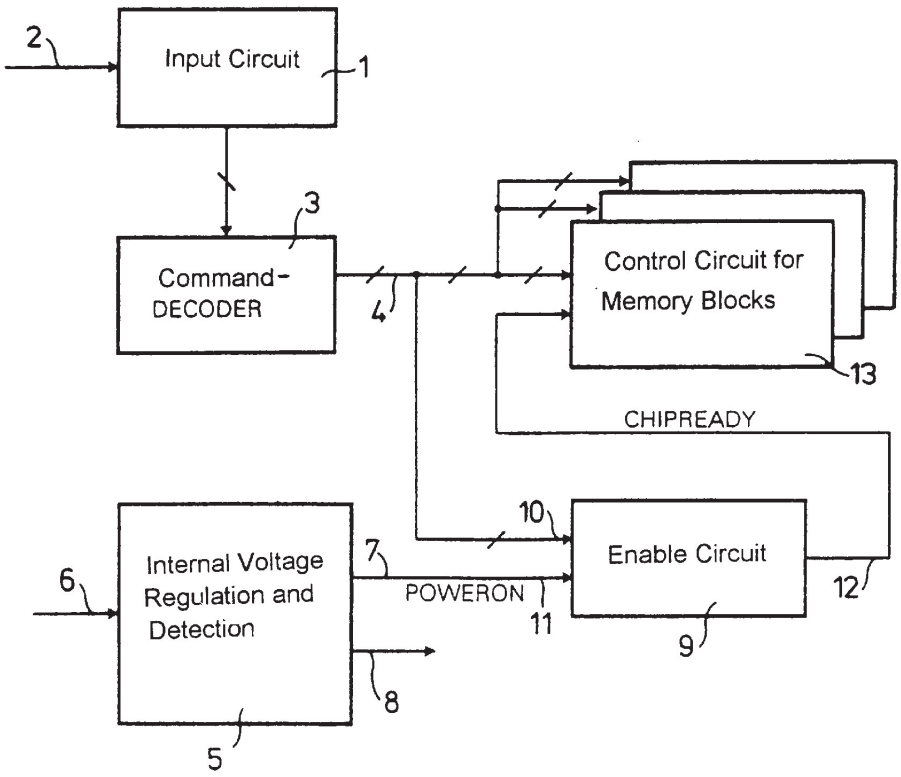


Fig 1


2
Input Circuit
1
3
Command-
DECODER
4
Control Circuit for
Memory Blocks
13
CHIPREADY
10
Enable Circuit
12
7
POWERON
11
9
6
Internal Voltage
Regulation and
Detection
8
5

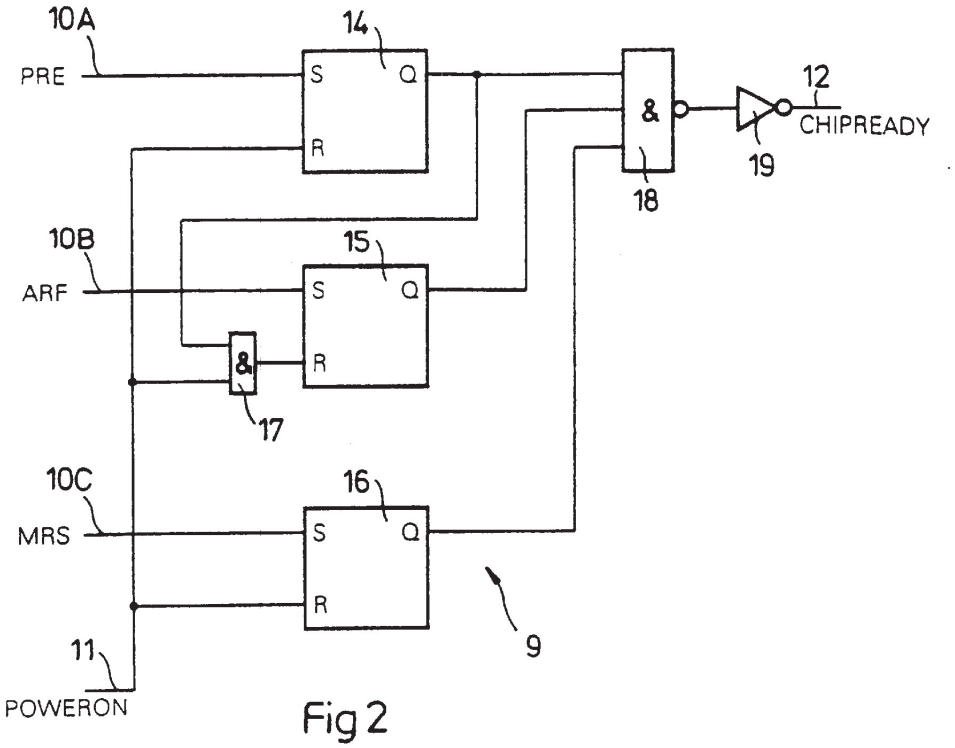

10A
PRE
14
S
Q
R
&
12
CHIPREADY
19
18
10B
ARF
15
S
Q
R
&
17
10C
MRS
16
S
Q
R
9
11
POWERON

Fig 2

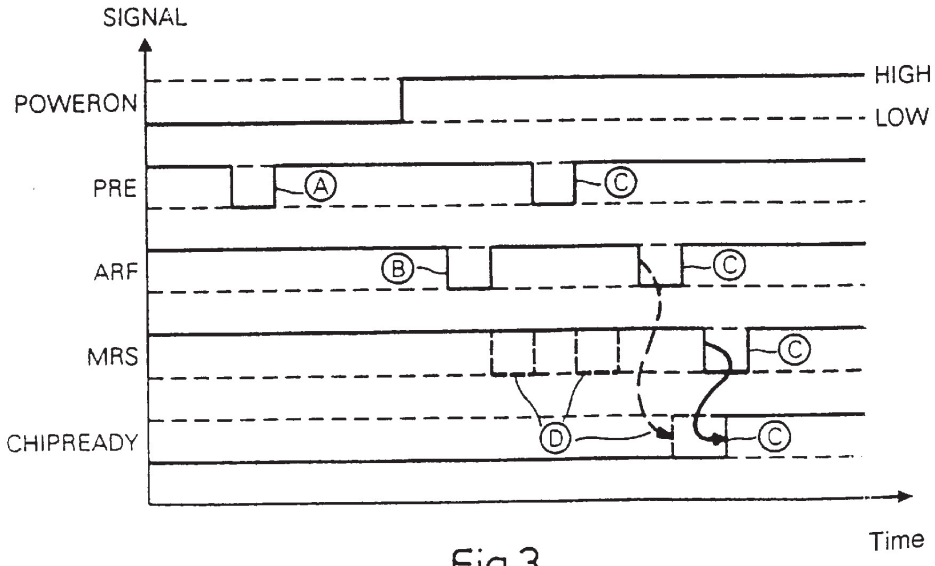

SIGNAL
POWERON
HIGH
LOW
PRE
A
C
ARF
B
C
MRS
C
CHIPREADY
D
C
Time

Fig 3

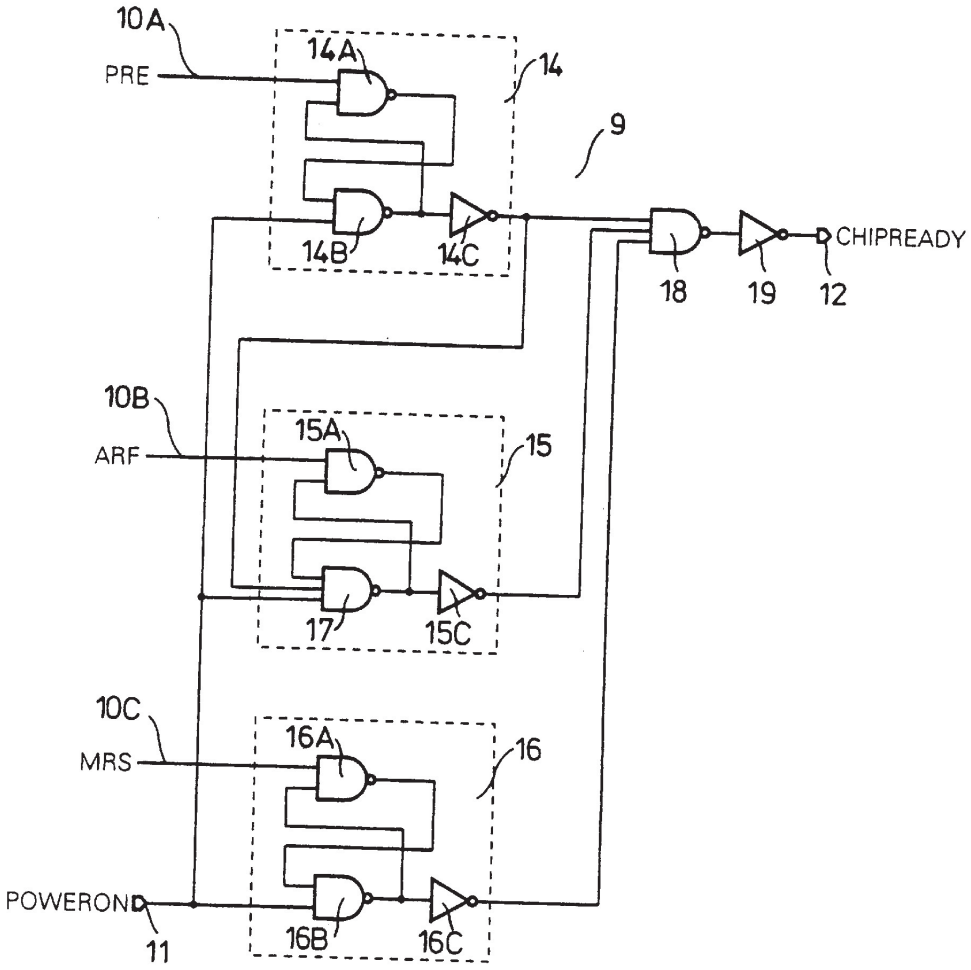

10A
PRE
14A
14
9
14B
14C
18
19
CHIPREADY
12
10B
ARF
15A
15
17
15C
10C
MRS
16A
16
POWERON
11
16B
16C

Fig 4

DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR INITIALIZING A DYNAMIC SEMICONDUCTOR MEMORY DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to a dynamic semiconductor memory device of the random access type (DRAM/SDRAM) having an initialization circuit which controls a switching-on operation of the semiconductor memory device and of its circuit components. The initialization circuit supplies a supply voltage stable signal (POWERON) once a supply voltage has been stabilized after the switching-on of the semiconductor memory device. The invention also relates to a method for initializing such a dynamic semiconductor memory device, and also to the use of an enable circuit, that supplies an enable signal, for controlling the switching-on operation of the dynamic semiconductor memory device.

In the case of SDRAM semiconductor memories according to the JEDEC standard, it is necessary to ensure during the switch-on operation ("POWERUP") that the internal control circuits provided for the proper operation of the semiconductor memory device are reliably held in a defined desired state, in order to prevent undesirable activation of output transistors that would cause, on the data lines, a short circuit (so-called "bus contention" or "data contention") or uncontrolled activation of internal current loads. The solution to the problem turns out to be difficult on account of a fundamental unpredictability of the time characteristic of the supply voltage and of the voltage level or levels at the external control inputs during the switch-on operation of the semiconductor memory. According to the specifications of the manufacturer an SDRAM component should ignore all commands which are present chronologically before a defined initialization sequence. The sequence consists of predetermined commands that must be applied in a defined chronological order. However, a series of functions and commands which are allowed during proper operation of the component are desired or allowed chronologically only after the initialization sequence. According to the JEDEC standard for SDRAM semiconductor memories, a recommended initialization sequence (so-called "POWERON-SEQUENCE") is provided as follows:

a. the application of a supply voltage and a start pulse in order to maintain an NOP condition at the inputs of the component;

b. the maintenance of a stable supply voltage of a stable clock signal, and of stable NOP input conditions for a minimum time period of 200 us;

c. the preparation command for word line activation (PRECHARGE) for all the memory banks of the device;

4. the activation of eight or more refresh commands (AUTOREFRESH); and

5. the activation of a loading configuration register command (MODE-REGISTER-SET) for initializing the mode register.

After the identification of such a defined initialization sequence, the memory module is normally in a so-called IDLE state, that is to say it is precharged and prepared for proper operation. In the case of the SDRAM semiconductor memory modules that have been disclosed to date, all the control circuits of the component have been unlatched only with the POWERON signal. The signal POWERON is active if the internal supply voltages have reached the necessary values that are necessary for the proper operation of the component. The module is then in a position to recognize and execute instructions.

SUMMARY OF THE INVENTION

It is accordingly an object of the invention to provide a dynamic semiconductor memory device and a method for initializing a dynamic semiconductor memory device which overcome the above-mentioned disadvantages of the prior art methods and devices of this general type, which is as simple as possible in structural terms and which effectively prevents the risk of a short circuit of the data lines and/or of uncontrolled activation of internal current loads.

With the foregoing and other objects in view there is provided, in accordance with the invention, a dynamic semiconductor memory device of a random access type, containing an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation. The initialization circuit has a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals. The enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals are identified and the enable signal effecting an unlatching of the control circuit.

The invention provides for the initialization circuit to have an enable circuit, which receives the supply voltage stable signal and the externally applied further command signals. The enable circuit generates the enable signal after the identification of the predetermined proper initialization sequence of the command signals is achieved. The enable signal effects the unlatching of the control circuit provided for the proper operation of the semiconductor memory device.

Following the principle of the invention, the enable signal (CHIPREADY) is generated and becomes active in dependence on further internal signals and the initialization sequence and then unlatches predetermined circuits. The predetermined circuits remain latched until the end of the predetermined initialization sequence. By way of example, commands are decoded but not executed and the output drivers are held at high impedance.

According to the preferred application in SDRAM memory devices according to the JEDEC standard, it is provided that the command signals, externally applied to the semiconductor memory device, of the initialization sequence are to be identified by the enable circuit. The command signals include a preparation command signal for word line activation (PRECHARGE), and/or a refresh command signal (AUTOREFRESH), and/or a loading configuration register command signal (MODE-REGISTER-SET).

According to an advantageous structural refinement of the initialization circuit according to the invention, it is provided that the enable circuit has at least one bistable multivibrator stage with a set input which receives the command signal (PRECHARGE, AUTOREFRESH, MODE-REGISTER-SET). The bistable multivibrator also has a reset input to which the supply voltage stable signal (POWERON), a signal derived therefrom, or a linked signal is applied. The bistable multivibrator further has an output at which the enable signal (CHIPREADY) is outputted.

In particular, the enable circuit has a plurality of bistable multivibrator stages respectively receiving the command signals.

In an expedient refinement of the invention, it is provided that the output of at least one of the bistable multivibrator stages is passed to a reset input of a further multivibrator stage. In this case, it may furthermore be provided that, in one of the bistable multivibrator stages, the supply voltage stable signal (POWERON) and the signal output from the output of the further multivibrator stage are passed, after having been logically combined by a gate, to the reset input of the multivibrator stage.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a dynamic semiconductor memory device and a method for initializing a dynamic semiconductor memory device, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagrammatic, block diagram of components of an initialization circuit which controls a switching-on operation of a semiconductor memory and its circuit components according to the invention;

FIG. **2** is circuit diagram of an enable circuit that supplies an enable signal (CHIPREADY);

FIG. **3** is a time sequence diagram for elucidating a method of operation of the circuit according to FIG. **2**; and

FIG. **4** is a circuit diagram of the enable circuit according to an exemplary embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In all the figures of the drawing, sub-features and integral parts that correspond to one another bear the same reference symbol in each case. Referring now to the figures of the drawing in detail and first, particularly, to FIG. **1** thereof, there are shown circuit components, important for understanding the invention, of an SDRAM memory device operating according to the JEDEC standard. The circuit components include an initialization circuit controlling a switching-on operation of the SDRAM memory device and its circuit components. The initialization circuit has an input circuit **1**, to whose input **2** command and clock signals that are externally applied in reference to the semiconductor memory are provided. The command and clock signals are amplified and conditioned before being received by a command decoder **3** connected downstream of the input circuit **1** and at whose output **4**, inter alia, the command signals PRE or PRECHARGE (preparation command for word line activation), ARF or AUTOREFRESH (refresh command) and MRS or MODE-REGISTER-SET (loading configuration register command) are output. The initialization circuit further has a circuit **5** for internal voltage regulation and/or detection, at whose input **6** the external supply voltages that are externally applied to the semiconductor memory externally are fed in. The circuit **5** has a first output **7** outputting a POWERON signal and a second output **8** supplying stabilized internal supply voltages. The method of operation and the structure of the circuits **1**, **3** and **5** are sufficiently known to the person skilled in the art and therefore do not need to be explained in any more detail. What is important for understanding the invention is the fact that the circuit **5** supplies an active POWERON signal if, after the POWERUP phase of the SDRAM memory, the internal supply voltages present at the output **8** have reached the values necessary for proper operation of the component.

According to the invention, the initialization circuit furthermore has an enable circuit **9** connected downstream of the circuits **3** and **5**. The command signals PRE, ARF and MRS are applied to an input **10** of the enable circuit **9** and the POWERON signal is applied to an input **11** of the enable circuit **9**. An enable signal CHIPREADY is supplied at an output **12** of the enable circuit **9** after the identification of a predetermined proper initialization sequence of the command signals applied to the semiconductor memory device is achieved. The enable signal effects unlatching of control circuits **13** provided for proper operation of the semiconductor memory device. The internal control circuits **13** serve inter alia for sequence control for one or more of the memory blocks of the SDRAM memory and are known as such.

FIG. **2** shows a preferred exemplary embodiment of the enable circuit **9** according to the invention. The enable circuit **9** contains three bistable multivibrator stages **14**, **15** and **16** each having a set input S, a reset input R, and also an output Q. An AND gate **17** connected upstream of the reset input R of the multivibrator stage **15** and an AND gate **18** connected downstream of all the outputs Q of the multivibrator stages **14**, **15**, **16** are further provided. The enable circuit further has an inverter **19** connected downstream of the AND gate **18**. The enable signal CHIPREADY being output at the output **12** of the inverter **19** and the enable signal CHIPREADY is active HIGH, that is to say activated when its voltage level is at logic HIGH. The command signals PRE, ARF, MRS applied to the respective set inputs S of the bistable multivibrator stages **14**, **15**, **16** are each active LOW, that is to say these signals are active when their voltage level is at logic LOW, while the POWERON signal is again active HIGH. The POWERON signal is applied directly to the reset inputs R in the case of the multivibrator stages **14** and **16** and is firstly applied to one input of the AND gate **17** in the case of the multivibrator stage **15**, the signal output from the output Q of the multivibrator stage **14** is applied to the other input of the AND gate **17**, the output of the AND gate **17** is connected to the reset input of the multivibrator stage **15**.

The method of operation of the enable circuit **9** illustrated in FIG. **2** is such that activation of the enable signal CHIPREADY at is the output **12** to logic HIGH is generated only when a predetermined chronological initialization sequence of the command signals PRE, ARF and MRS and activation of the POWERON signal to the logic level HIGH are detected. Only then are the control circuits **13** unlatched on account of the activation of the enable signal CHIPREADY; the control circuits **13** remaining latched prior to this.

In the schematic time sequence diagram according to FIG. **3**, exemplary command sequences during the switching-on operation of the semiconductor memory device are illustrated in order to elucidate the method of operation of the enable circuit **9**. In the case situation A, the signal PRECHARGE is activated to active LOW too early relative to the activation of the POWERON signal, with the result that, the enable signal CHIPREADY is not yet activated to logic HIGH since the proper initialization sequence requires a

waiting time before the first command. The signal swing of the command PRECHARGE according to case situation A is thus correctly ignored. In case situation B, the chronological order of the activation of the signal AUTOREFRESH to logic LOW is incorrect since the proper initialization sequence prescribes a previous PRECHARGE command before the AUTOREFRESH command. The signal swing of the AUTOREFRESH signal to logic LOW according to case situation B is therefore likewise ignored, and the enable signal does not go to logic HIGH. In case situation C, a correct chronological order of the commands PRECHARGE, AUTOREFRESH, MODE-REGISTER-SET is present conforming to the JEDEC standard, in a logically consistent manner, since the POWERON signal is also at logic HIGH, an enable signal CHIPREADY at logic HIGH is now supplied. Illustrated using dashed lines, another further conceivable initialization sequence that is allowed and therefore triggers an enable signal is represented by the symbol D; activation of the command MODE-REGISTER-SET to logic LOW is allowed at any time after the activation of the POWERON signal.

FIG. **4** shows further details of a preferred exemplary embodiment of the enable circuit **9** according to the invention. In this exemplary embodiment, each of the bistable multivibrators **14**, **15**, **16** is constructed from in each case two NAND gates **14**A, **14**B, **15**A, **17**, **16**A, **16**B and also an inverter **14**C, **15**C and **16**C, which are connected to one another in the manner illustrated. The NAND gate **17** is provided with three inputs in the bistable multivibrator **15**.

I claim:

1. A dynamic semiconductor memory device of a random access type, comprising:

an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation, said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals, said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit.

2. The semiconductor memory device according to claim **1**, wherein the externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit includes at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal.

3. The semiconductor memory device according to claim **1**, wherein said enable circuit has at least one bistable multivibrator stage having a set input receiving the externally applied further command signals, a reset input receiving one of the supply voltage stable signal, a signal derived from the supply voltage stable signal and a linked signal, and an output outputting said enable signal.

4. The semiconductor memory device according to claim **3**, wherein said at least one bistable multivibrator stage is a plurlity of bistable multivibrator stages respectively receiving one of the externally applied further command signals.

5. The semiconductor memory device according to claim **4**, wherein said output of one of said plurality of bistable multivibrator stages is passed to said reset input of another of said plurality of bistable multivibrator stages.

6. The semiconductor memory device according to claim **4**, including an AND gate receiving the supply voltage stable signal and a signal output from said output of one of said plurality of bistable multivibrator stages, said AND gate outputting an output signal received at said reset input of another of said plurality of bistable multivibrator stages.

7. The semiconductor memory device according to claim **4**, wherein said plurality of bistable multivibrator stages are each formed of an RS flip-flop constructed from one of at least two NOR and at least two NAND gates.

8. The semiconductor memory device according to claim **1**, wherein the identification of an initialization sequence that is identified as the predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard.

9. The semiconductor memory device according to claim **1**, wherein said control circuit has output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit.

10. The semiconductor memory device according to claim **1**, wherein the predetermined proper initialization sequence includes one of the following chronologically successive command sequences:

a) firstly PRE, secondly ARF, thirdly MRS;

b) firstly PRE, secondly MRS, thirdly ARF; and

c) firstly MRS, secondly PRE, or thirdly ARF;

where,

PRE=the preparation command signal for word line activation,

ARF=the refresh command signal, and

MRS=the loading configuration register command signal.

11. An improved method for initializing a dynamic semiconductor memory device of a random access type via an initialization circuit controlling a switching-on operation of the dynamic semiconductor memory device and of its circuit components, the improvement which comprises:

supplying, via the initialization circuit, a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device; and

supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device.

12. The method according to claim **11**, which comprises providing at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal as the further command signals.

13. The method according to claim **11**, which comprises maintaining a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit.

* * * * *

EXHIBIT 2

US006438057B1

(12) **United States Patent**
Ruckerbauer

(10) **Patent No.: US 6,438,057 B1**
(45) **Date of Patent: Aug. 20, 2002**

(54) **DRAM REFRESH TIMING ADJUSTMENT DEVICE, SYSTEM AND METHOD**

(75) Inventor: **Hermann Ruckerbauer**, Moos (DE)

(73) Assignee: **Infineon Technologies AG** (DE)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/900,626**

(22) Filed: **Jul. 6, 2001**

(51) **Int. Cl.**[7] **G11C 7/00**
(52) **U.S. Cl.** **365/222**; 365/211
(58) **Field of Search** 365/222, 211, 365/228

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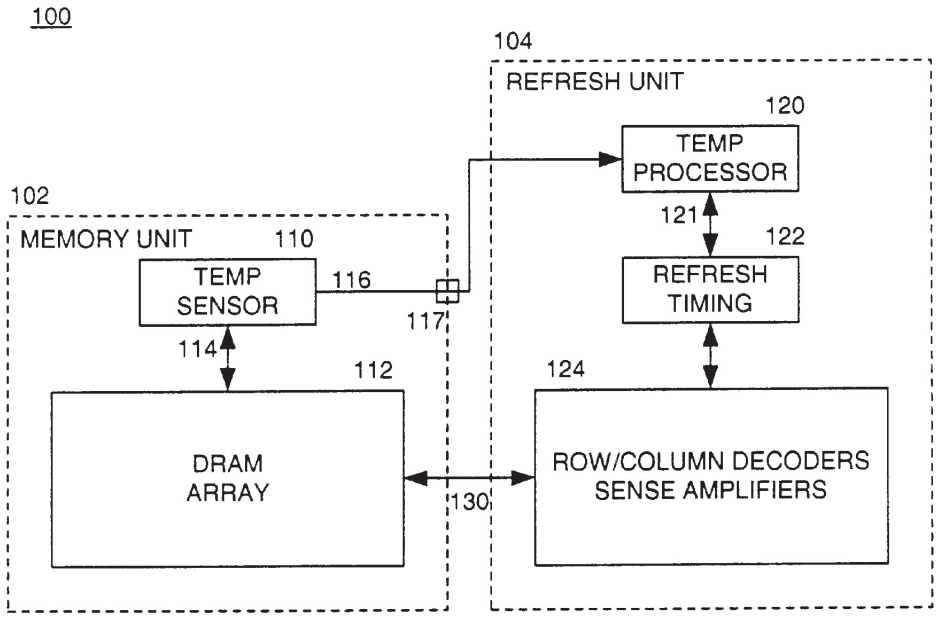
Primary Examiner—Vu A. Le
(74) *Attorney, Agent, or Firm*—Lerner, David, Littenberg, Krumholz & Mentlik, LLP

(57) **ABSTRACT**

An apparatus includes at least one dynamic random access memory (DRAM) array; and at least one temperature sensor in thermal communication with the DRAM array and operable to produce a signal indicative of a temperature of the DRAM array.

17 Claims, 5 Drawing Sheets



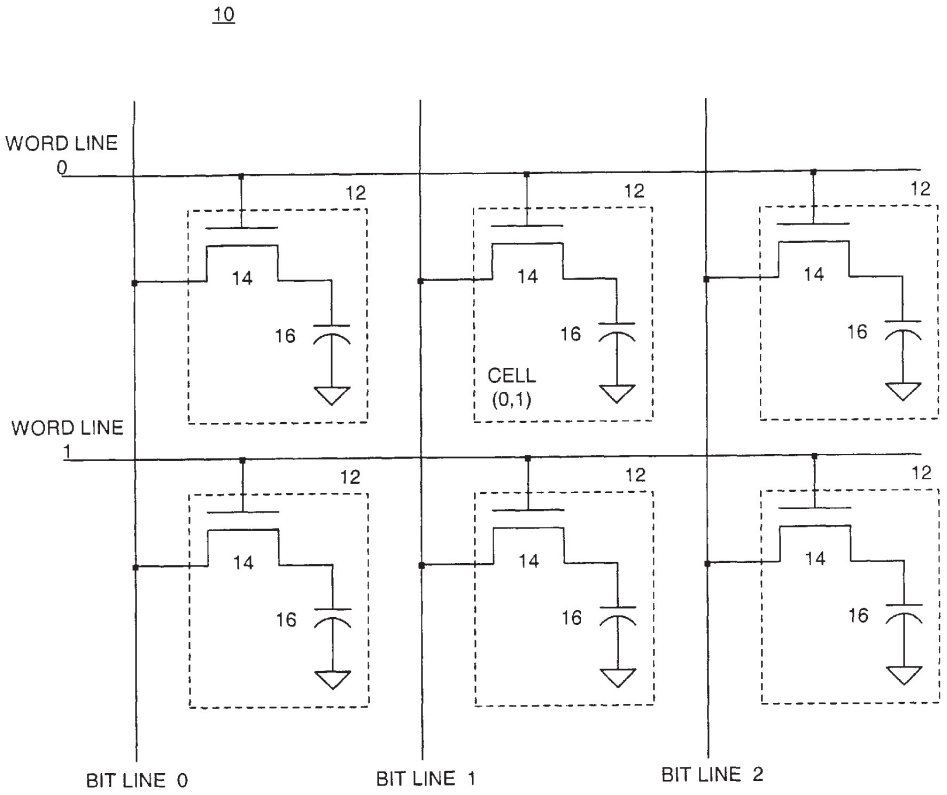

10
WORD LINE 0
WORD LINE 1
12
14
16
CELL (0,1)
BIT LINE 0
BIT LINE 1
BIT LINE 2

FIG. 1

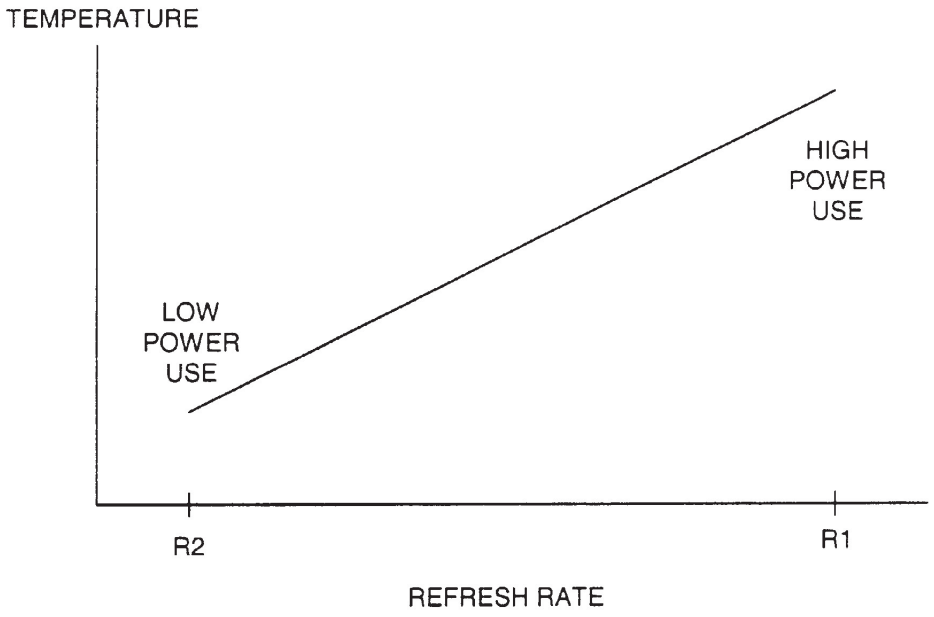


FIG. 2

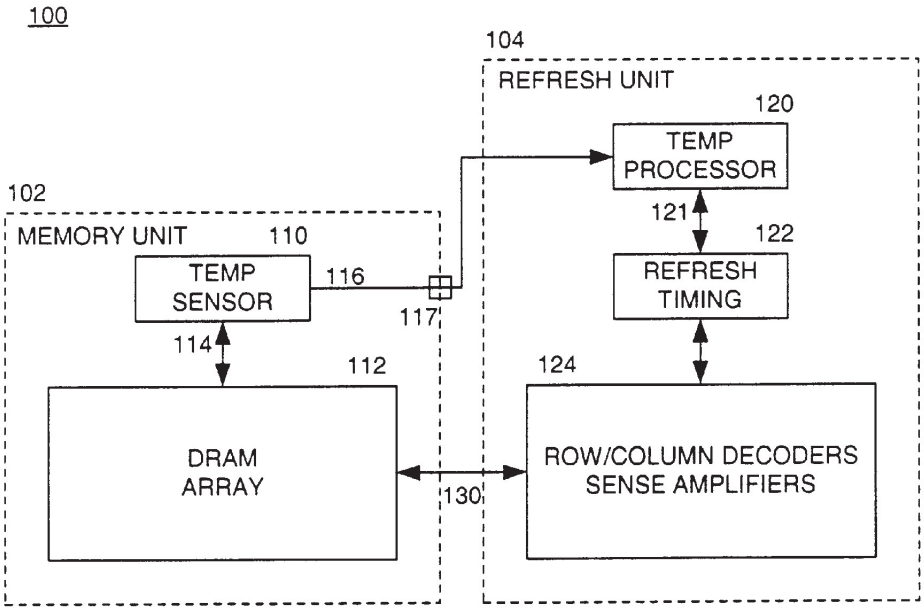

100
104
REFRESH UNIT
120
TEMP PROCESSOR
121
122
REFRESH TIMING
102
MEMORY UNIT
110
TEMP SENSOR
116
117
114
112
124
DRAM ARRAY
130
ROW/COLUMN DECODERS SENSE AMPLIFIERS

FIG. 3

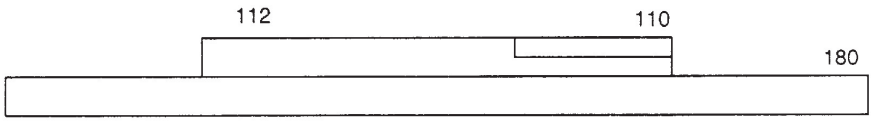


FIG. 4A

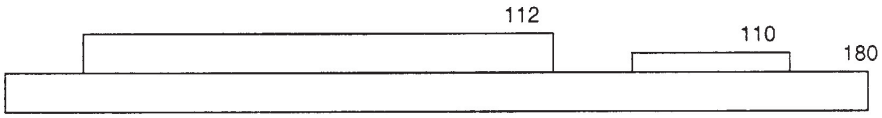


FIG. 4B

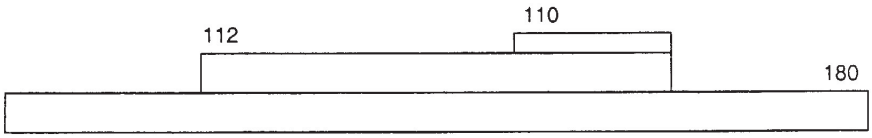


FIG. 4C

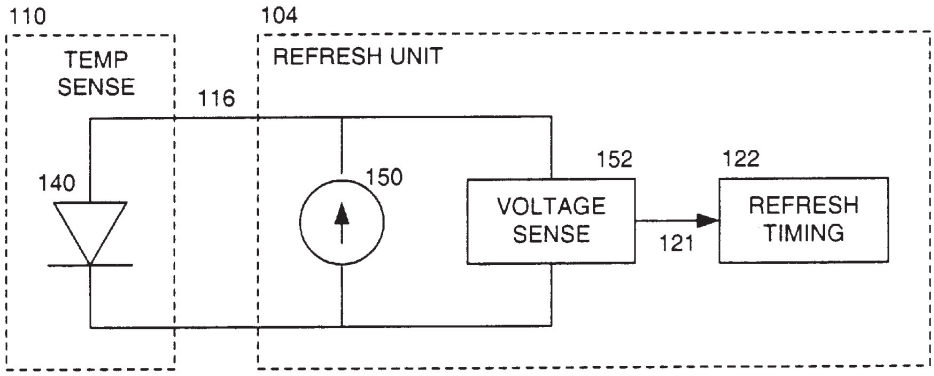

110
104
TEMP SENSE
REFRESH UNIT
116
140
150
152
122
VOLTAGE SENSE
121
REFRESH TIMING

FIG. 5

DRAM REFRESH TIMING ADJUSTMENT DEVICE, SYSTEM AND METHOD

BACKGROUND OF THE INVENTION

The present invention relates to devices, systems, and/or methods for refreshing the contents of a dynamic random access memory (DRAM) array and, more particularly, to devices, systems, and/or methods for utilizing a temperature of the DRAM array to adjust a refresh rate at which the contents of the DRAM array are updated.

A common form of random access memory (RAM) is dynamic random access memory (DRAM). With reference to the equivalent circuit shown in FIG. **1**, DRAMs employ a semiconductor technology called complementary metal-oxide-semiconductor CMOS to implement a memory array **10** including a plurality of memory cells **12**, each cell **12** consisting of a single transistor **14** and a single capacitor **16**. A given cell **12** of the DRAM array **10** may be accessed by activating a particular bit line and word line. As the cells **12** of the DRAM array are arranged in a grid, only one cell **12** will be accessed for each combination of word line and bit line.

For example, in order to write a data bit into cell **(0,1)**, word line **0** is activated by applying an appropriate voltage to that line, e.g., a logic high (such as 3.3V, 5V, 15V, etc.) or a logic low (such as 0V). The appropriate voltage on word line **0** will turn on each of the transistors **14** connected to that line including the transistor **14** of cell **(0,1)**. A voltage may then be presented on bit line **1**, which will charge the capacitor **16** of cell **(0,1)** to a desired level, e.g., a logic high or logic low consistent with the data bit. The voltage may be presented on bit line **1** (and/or any of the other bit lines) by way of a suitably connected data bus. When the voltage on word line **0** is removed, the transistor **14** of cell **(0,1)** is biased off and the charge on the capacitor **16** of cell **(0,1)** is stored.

Reading a data bit from a particular cell **12**, such as cell **(0,1)**, is substantially similar to writing a data bit except that the voltage on bit line **1** is imposed by the capacitor **16** of the cell **12** rather than by the data bus. Typically, a single cell **12** is not written to or read from; rather, an entire word (series of data bits) is written into the DRAM array **10** or read from the DRAM array **10** by applying the appropriate voltage on a particular word line and either imposing or sensing voltage on each of the bit lines **0,1,2**, etc.

Once data bits (i.e., voltages) have been stored on the capacitors **16** of the DRAM array **10**, the data are not permanent. Indeed, various leakage paths exist around the capacitors **16** and, therefore, failure to read the date may corrupt the stored voltages. In order to avoid the loss of data stored in the DRAM array **10**, the data are refreshed on a periodic basis. In particular, an external sense amplifier is employed to sense the data stored in the DRAM array **10** and rewrite (i.e., refresh) the data onto the capacitors **16**. Typically, the data associated with a particular word line (i.e., one data word) are refreshed every 7.8 microseconds (e.g., for 256 Mbit DRAM arrays) or every 15.6 microseconds (e.g., for 64 Mbit DRAM arrays). The refresh rate for a particular DRAM array **10** is established by the manufacturer and is based on a worst-case high temperature condition.

The refresh process may be implemented in either of two ways, namely, internally (self refresh) or externally (CBR or Ras only refresh). The internal refresh process requires that the DRAM itself set the refresh timing. The external refresh process requires an external chip (chipset) that issues a refresh command. The DRAM receives the refresh command from the external chip through a dedicated pin.

Unfortunately, the refresh process has a deleterious effect on overall system performance. Among these deleterious effects are: (i) an increase in power consumed by the DRAM array **10** and any external circuitry involved in the refresh process; and (ii) a decrease in overall system bandwidth. As to the former, the external sense amplifiers and other associated circuitry (e.g., row decoders, column decoders, etc.) involved in the refresh process, not to mention the DRAM array **10** itself, draw power in order to rewrite the data into the DRAM array **10**. In certain applications, such as in the automotive industry, power efficiency is desirable and increases in power consumption due to DRAM array **10** refresh cycles may be problematic. As to the latter, the refresh cycles of the DRAM array **10** take priority over routine reading and writing cycles and, therefore, the rate at which the DRAM array **10** is refreshed has a corresponding impact on the bandwidth (e.g., data throughput) of the overall system in which the DRAM array **10** is utilized.

Accordingly, there is a need in the art for a new device, system, and/or method for refreshing the data of a DRAM array such that power consumption is reduced and system bandwidth is increased.

SUMMARY OF THE INVENTION

In accordance with at least one aspect of the present invention, an apparatus includes: at least one DRAM array; and at least one temperature sensor in thermal communication with the DRAM array and operable to produce a signal indicative of a temperature of the DRAM array.

Preferably, the DRAM array is refreshed at a rate that varies in response to the signal. For example, the rate at which the DRAM array is refreshed may decrease as the temperature of the DRAM array decreases. Further, the rate at which the DRAM array is refreshed may increase as the temperature of the DRAM array increases.

Preferably, the at least one temperature sensor includes at least one diode having a forward voltage drop that varies as a function of the temperature of the DRAM array, and the signal corresponds to the forward voltage drop of the at least one diode. Alternatively, the at least one temperature sensor may be taken from the group consisting of thermocouples, thermistors, or any other device that provides an output signal that varies as a function of temperature.

In accordance with one or more further aspects of the invention, the apparatus may further include a refresh unit operable to refresh the DRAM array at a rate that varies in response to the signal. Preferably, the refresh unit includes a refresh timing unit operable to establish the rate at which the DRAM array is refreshed in response to the signal. It is preferred that the refresh timing unit is operable to decrease the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array decreases. It is also preferable that the refresh timing unit is operable to increase the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array increases.

When the at least one temperature sensor is a diode, it is preferable that the refresh unit is operable to sense the forward voltage drop of the diode to determine the temperature of the DRAM array.

In accordance with one or more further aspects of the present invention, the DRAM array and the at least one temperature sensor are disposed in a semiconductor package, the package including at least one connection pin operable to provide the signal to external circuitry.

In accordance with one or more further aspects of the invention, the DRAM array, the at least one temperature sensor, and the refresh unit are integrated in a semiconductor package.

In accordance with at least one further aspect of the present invention, the apparatus includes: at least one DRAM chip including the DRAM array and the at least one temperature sensor; at least one refresh chip operable to refresh the DRAM array at a rate that varies in response to the signal. Preferably, the refresh chip includes the refresh timing unit.

In accordance with one or more further aspects of the present invention, a method includes: sensing a temperature of a DRAM array; and refreshing contents of the DRAM array at a rate that varies in response to the temperature thereof.

The method preferably further includes decreasing the rate at which the DRAM array is refreshed as the temperature of the DRAM array decreases. The method may also include increasing the rate at which the DRAM array is refreshed as the temperature of the DRAM array increases. It is most preferred that the step of sensing the temperature of the DRAM array includes sensing a forward voltage drop of a diode that is in thermal communication with the DRAM array.

Other aspects, features, advantages, etc. will become apparent to one skilled in the art in view of the description herein taken in combination with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

For the purposes of illustrating the invention, there are shown in the drawings forms which are presently preferred, it being understood, however, that the invention is not limited to the precise arrangements and/or instrumentalities shown.

FIG. **1** is a DRAM array in accordance with the prior art;

FIG. **2** is a graph illustrating the relationship between a temperature of the DRAM array and a desirable refresh rate of the DRAM array;

FIG. **3** is a block diagram of a DRAM apparatus in accordance with one or more aspects of the present invention; and

FIGS. **4**A–**4**C are structural views of alternative DRAM configurations in accordance with the present invention; and

FIG. **5** is a block diagram showing additional details of certain components of FIG. **3**.

DETAILED DESCRIPTION

With reference to FIG. **2**, it has been found that the refresh rate established by DRAM array manufacturers may be altered when the temperature of the DRAM array is lower than a worst-case value. For example, when the temperature of the DRAM array is relatively high, a correspondingly high refresh rate **R1** may be required to ensure integrity of the data stored in the DRAM array. The relatively high refresh rate **R1** unfortunately results in a correspondingly high power use and a low system bandwidth. Conversely, when the temperature of the DRAM array is relatively low, it has been found that a correspondingly lower refresh rate **R2** may be utilized to ensure the integrity of the data stored in the DRAM array. Advantageously, the relatively lower refresh rate **R2** results in a lower power usage and higher overall system bandwidth. Although the relationship between the temperature and the refresh rate of the DRAM array is illustrated as being a linear function in FIG. **2**, it is noted that the relationship may not be linear and may vary depending on the specific implementation of the DRAM array. It is believed, however, that the overall relationship between temperature and refresh rate for DRAM arrays will exhibit a positive slope. In accordance with one or more aspects of the present invention, this relationship is exploited to reduce power consumption of the DRAM array (and any associated circuitry) and improve overall system bandwidth.

FIG. **3**, is a block diagram of a system **100** for storing data in a DRAM array. The system **100** includes a memory unit **102** and a refresh unit **104**. The memory unit **102** preferably includes at least one temperature sensor **110** and at least one DRAM array **112**. The DRAM array **112** may be configured in a substantially similar way as shown in FIG. **1** and/or may be configured in accordance with any of the known technologies. Preferably, the temperature sensor **110** is in thermal communication with the DRAM array **112** (schematically illustrated by way of line **114**) and is operable to produce a signal on line **116** that is indicative of a temperature of the DRAM array **112**. By way of example, the DRAM array **112** may be implemented on a semiconductor chip and the temperature sensor **110** may be thermally coupled to the same semiconductor chip or to an intermediate member that is in thermal communication with the semiconductor chip.

The refresh unit **104** preferably includes a temperature processor **120**, a refresh timing unit **122**, and a decoder/amplifier unit **124**. The refresh unit **104** is preferably operable to refresh the DRAM array **112** (by way of connection **130**) at a rate that varies in response to the signal on line **116**. More particularly, the DRAM array **112** is preferably refreshed at a rate that decreases as the temperature of the DRAM array **112** decreases and/or refreshed at a rate that increases as the temperature of the DRAM array **112** increases. The temperature processor **120** is preferably operable to detect a level of the signal on line **116** and to provide an indication of the temperature (by way of line **121**) of the DRAM array **112** to the refresh timing unit **122**. The refresh timing unit **122** is preferably operable to establish the rate at which the DRAM array **112** is refreshed in response to the temperature indication from the temperature processor **120**. The row/column decoders and sense amplifiers **124** are preferably operable to perform the refresh function on the DRAM array **112** in accordance with known techniques at intervals dictated by the refresh timing unit **122**.

In accordance with at least one aspect of the present invention, the temperature sensor **110** and the DRAM array **112** are preferably disposed in a semiconductor package where the package includes at least one connection pin **117** operable to provide the signal on line **116** to external circuitry, such as the refresh unit **104**. In accordance with a further aspect of the present invention, the DRAM array **112**, temperature sensor **110**, and the refresh unit **104** are integrated in the same semiconductor package such that external circuitry is not required to perform the refresh function. In accordance with a further aspect of the present invention, the refresh unit **104** is implemented by way of one or more semiconductor packages so as to form a chipset with the package containing the temperature sensor **110** and the DRAM array **112**.

Reference is now make to FIGS. **4**A–**4**C, which are structural views of alternative configurations of the DRAM array **112** and temperature sensor **110**. In FIG. **4**A, the DRAM array **112** is disposed on an intermediate member **180**, such as a substrate, a heatsink, etc. The temperature

sensor **110** is integrated with the DRAM array structure **112**, such as by implementing the temperature sensor **110** into the semiconductor material of the DRAM array **112**. As shown in FIG. **4**B, an alternative structural configuration is contemplated where the DRAM array **112** and the temperature sensor **110** are disposed on the intermediate member **180**, where the intermediate member **180** exhibits desirable thermal conductivity properties. Indeed, in this configuration it is preferred that the intermediate member **180** exhibits a low thermal resistance between the DRAM array **112** and the temperature sensor **110** such that an accurate measurement of the temperature of the DRAM array **112** may be obtained. The structural configuration shown in FIG. **4**C shows that the temperature sensor **110** may be coupled to the semiconductor device **112**, such as by bonding it to the semiconductor material of the DRAM array **112**.

With reference to FIG. **5**, the temperature sensor **110** preferably includes at least one diode **140** having a forward voltage drop that varies as a function of the temperature of the DRAM array **112**. The signal on line **116** preferably corresponds to the forward voltage drop of the diode **140**. By way of example, the refresh unit **104** may include a current source **150** operatively coupled to the diode **140** such that the diode **140** is forward biased. The refresh unit **104** may also include a voltage sensor **152** operatively coupled across the diode **140** such that the forward voltage drop across the diode **140** may be measured. The voltage sensor **152** preferably produces a value on line **121** indicative of the temperature of the DRAM array **112** vis-a-vis the forward voltage drop of the diode **140**.

Although the use of diode **140** is preferred, various other temperature sensing devices and techniques may be employed, such as the use of one or more thermocouples, thermistors, etc.

In accordance with at least one further aspect of the present invention, a method of refreshing the contents of a DRAM array may be achieved utilizing suitable hardware, such as that illustrated in FIGS. **3–5** and/or utilizing a manual or automatic process. An automatic process may be implemented using any of the known processors that are operable to execute instructions of a software program. In either case, the steps and/or actions of the method preferably correspond to the functions described hereinabove with respect to at least portions of the hardware shown in FIGS. **3–5**.

Although the invention herein has been described with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present invention. It is therefore to be understood that numerous modifications may be made to the illustrative embodiments and that other arrangements may be devised without departing from the spirit and scope of the present invention as defined by the appended claims.

What is claimed is:

1. An apparatus, comprising:

a semiconductor package including at least one connection pin;

at least one dynamic random access memory (DRAM) array disposed within the package; and

at least one temperature sensor in thermal communication with the DRAM array, operable to produce a signal indicative of a temperature of the DRAM array, and coupled to the at least one connection pin such that the signal may be provided to external circuitry,

wherein the DRAM array is refreshed at a rate that decreases as the temperature of the DRAM array decreases and that increases as the temperature of the DRAM array increases.

2. The apparatus of claim **1**, wherein the at least one temperature sensor includes at least one diode having a forward voltage drop that varies as a function of the temperature of the DRAM array, and the signal corresponds to the forward voltage drop of the at least one diode.

3. The apparatus of claim **1**, wherein the at least one temperature sensor is taken from the group consisting of thermocouples and thermistors.

4. The apparatus of claim **1**, wherein the at least one temperature sensor includes a diode having a forward voltage drop that varies as a function of the temperature of the DRAM array; the at least one connection pin includes a first pin coupled to an anode of the diode and a second pin coupled to a cathode of the diode; and the signal corresponds to a potential voltage between the first and second pins.

5. The apparatus of claim **1**, wherein the at least one temperature sensor is taken from the group consisting of thermocouples and thermistors.

6. The apparatus of claim **1**, further comprising a refresh unit operable to refresh the DRAM array at a rate that varies in response to the signal.

7. The apparatus of claim **6**, wherein the refresh unit includes a refresh timing unit operable to establish the rate at which the DRAM array is refreshed in response to the signal.

8. The apparatus of claim **7**, wherein the refresh timing unit is operable to decrease the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array decreases.

9. The apparatus of claim **7**, wherein the refresh timing unit is operable to increase the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array increases.

10. The apparatus of claim **7**, wherein the at least one temperature sensor includes at least one diode having a forward voltage drop that varies as a function of the temperature of the DRAM array, and the signal corresponds to the forward voltage drop of the at least one diode.

11. The apparatus of claim **10**, wherein the refresh unit is operable to sense the forward voltage drop of the diode to determine the temperature of the DRAM array.

12. The apparatus of claim **6**, wherein the DRAM array, the at least one temperature sensor, and the refresh unit are integrated in a semiconductor package.

13. A dynamic random access memory (DRAM) chipset, comprising:

at least one DRAM chip including a DRAM array and at least one temperature sensor in thermal communication with the DRAM array, the at least one temperature sensor being operable to produce a signal indicative of a temperature of the DRAM array, the DRAM chip including at least one connection pin operable to provide the signal to external circuitry; and

at least one refresh chip operable to refresh the DRAM array at a rate that varies in response to the signal,

wherein the refresh chip is operable to (i) decrease the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array decreases; and (ii) increase the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array increases.

14. The apparatus of claim **13**, wherein the at least one temperature sensor includes at least one diode having a forward voltage drop that varies as a function of the temperature of the DRAM array, and the signal corresponds to the forward voltage drop of the at least one diode.

15. The apparatus of claim **14**, wherein the refresh chip is operable to sense the forward voltage drop of the diode to determine the temperature of the DRAM array.

16. A method, comprising:

sensing a temperature of a dynamic random access memory (DRAM) array;

outputting a signal indicative of the temperature of the DRAM array to external circuitry; and

refreshing contents of the DRAM array at a rate that (i) decreases as the temperature of the DRAM array decreases; and (ii) increases as the temperature of the DRAM array increase.

17. The method of claim **16**, wherein the step of sensing the temperature of the DRAM array includes sensing a forward voltage drop of a diode that is in thermal communication with the DRAM array.

* * * * *

EXHIBIT 3

US006850414B2

(12) **United States Patent**
Benisek et al.

(10) **Patent No.: US 6,850,414 B2**
(45) **Date of Patent: Feb. 1, 2005**

(54) **ELECTRONIC PRINTED CIRCUIT BOARD HAVING A PLURALITY OF IDENTICALLY DESIGNED, HOUSING-ENCAPSULATED SEMICONDUCTOR MEMORIES**

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(73) Assignee: **Infineon Technologies AG**, Munich (DE)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 374 days.

(21) Appl. No.: **10/187,763**

(22) Filed: **Jul. 2, 2002**

(65) **Prior Publication Data**

US 2003/0002262 A1 Jan. 2, 2003

(30) **Foreign Application Priority Data**

Jul. 2, 2001 (DE) 101 31 939

(51) **Int. Cl.**[7] **H05K 1/00**; H05K 1/18; H05K 1/16; H05K 7/02; H05K 7/06

(52) **U.S. Cl.** **361/748**; 361/760; 174/260

(58) **Field of Search** 361/728–730, 361/735, 736–737, 748, 749, 760, 763, 767, 768, 807, 808, 785, 788, 790, 791, 803; 257/693, 684, 679, 678; 711/301; 714/773; 365/51–52, 63; 174/250, 253, 255–256, 260

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Primary Examiner—Phuong T. Vu
(74) *Attorney, Agent, or Firm*—Laurence A. Greenberg; Werner H. Stemer; Ralph E. Locher

(57) **ABSTRACT**

An electronic printed circuit board has a memory module and a contact strip for insertion into another electronic unit. The memory module has at least nine identically designed housing-encapsulated integrated semiconductor memories configured on the printed circuit board. The longer dimension of the housing of one of the semiconductor memories, which is connected as an error correction chip, is oriented perpendicular to the contact strip. The longer dimension of the housings of the other semiconductor memories are oriented parallel to the contact strip. The different orientation of the semiconductor memories makes it possible to reduce the height of the printed circuit board while enabling the rectangular housings to keep the same physical form.

8 Claims, 3 Drawing Sheets