



US005539229A

United States Patent [19]

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Noble, Jr et al.

[45] **Date of Patent:** Jul. 23, 1996

[54] **MOSFET WITH RAISED STI ISOLATION SELF-ALIGNED TO THE GATE STACK**

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[75] Inventors: **Wendell P. Noble, Jr**, Milton, Vt.;
Ashwin K. Ghatalia; **Badih El-Kareh**,
both of Hopewell Junction, N.Y.

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T. Furukawa et al., "Process and Device Simulation of Trench Isolation Corner Parasitic Device", Proceedings of the Electrochemical Society Meeting, Oct. 9-14, 1988.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

A. Bryant et al., "The Current-Carrying Corner Inherent to Trench Isolation", IEEE Electron Device Letters, vol. 14, No. 8, Aug. 1993.

[21] Appl. No.: **365,729**

D. Foty et al., "Behavior of an NMOS Trench-Isolated Corner Parasitic Device at Low Temperature", Proceedings of the Electrochemical Society Meeting, Oct. 1989.

[22] Filed: **Dec. 28, 1994**

T. Ishijima et al., "A Deep-Submicron Isolation Technology with T-shaped Oxide (TSO) Structure", Proceedings of the IEDM, 1990, p. 257.

[51] **Int. Cl.**⁶ **H01L 27/08**; H01L 29/76;
H01L 29/00

[52] **U.S. Cl.** **257/301**; 257/305; 257/397;
257/623

[58] **Field of Search** 257/301, 304,
257/305, 395, 396, 397, 398, 383, 385,
586, 587, 619, 623, 384

Primary Examiner—Donald L. Monin, Jr.
Attorney, Agent, or Firm—James M. Leas

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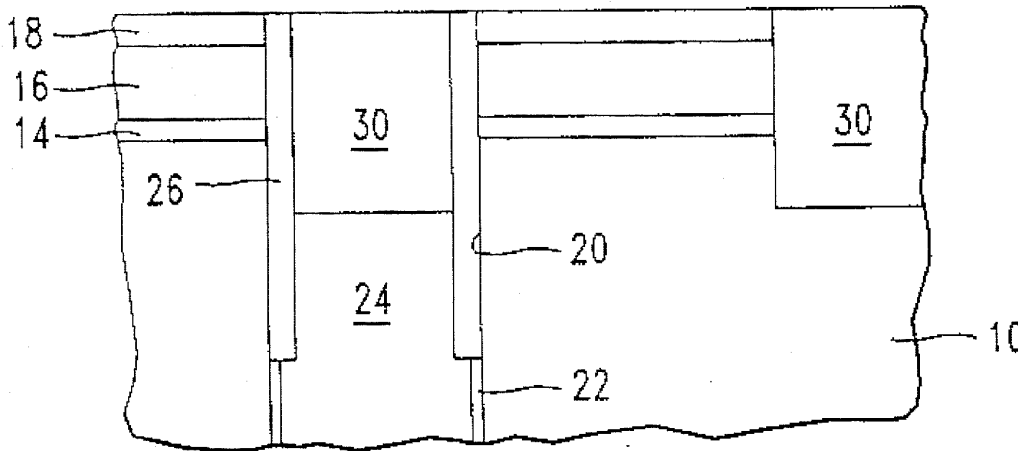
[57] **ABSTRACT**

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A semiconductor structure comprising a transistor having a gate conductor that has first and second edges bounded by raised isolation structures (e.g. STI). A source diffusion is self-aligned to the third edge and a drain diffusion is self-aligned to the fourth edge of the gate electrode.

19 Claims, 5 Drawing Sheets



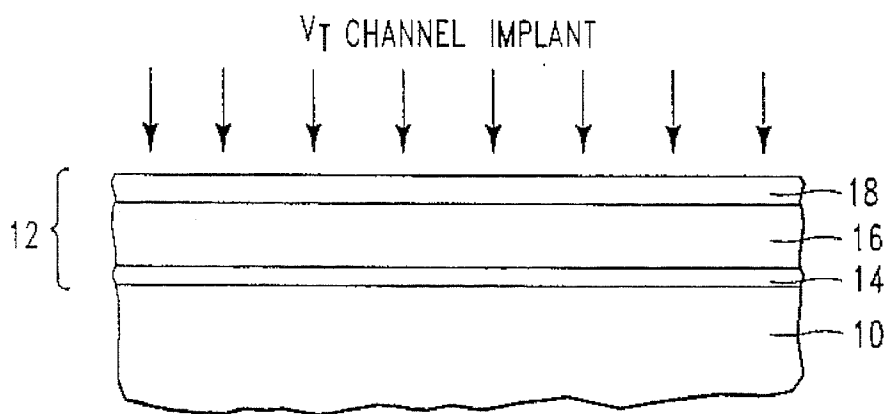


FIG. 1

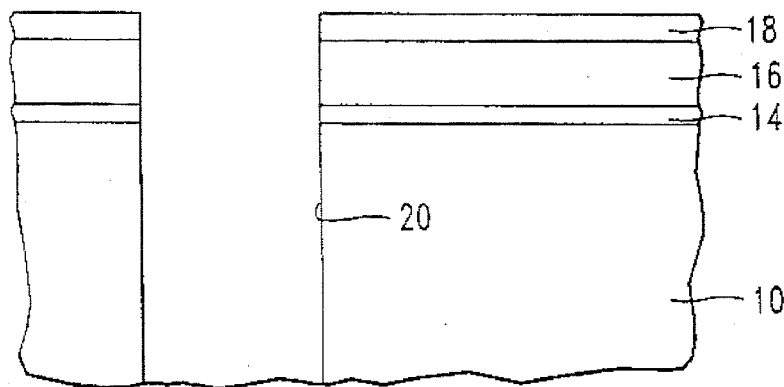


FIG. 2

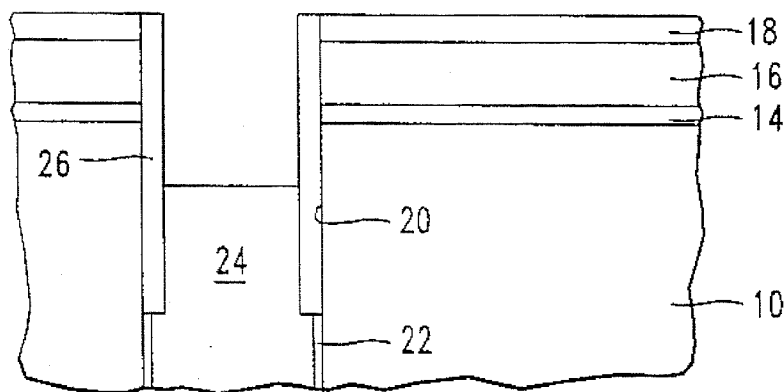


FIG. 3

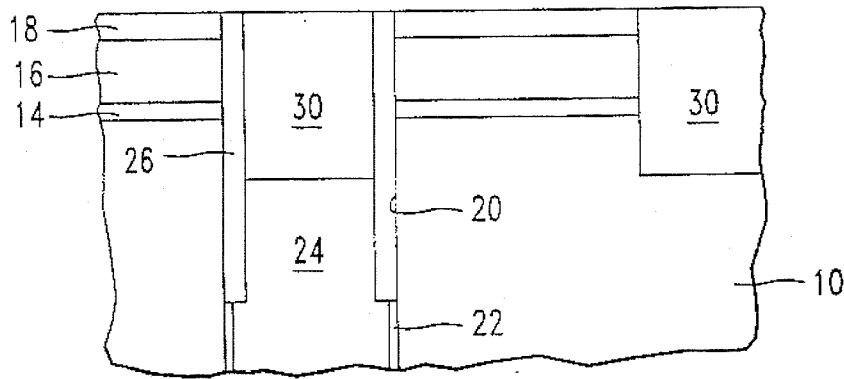


FIG. 4

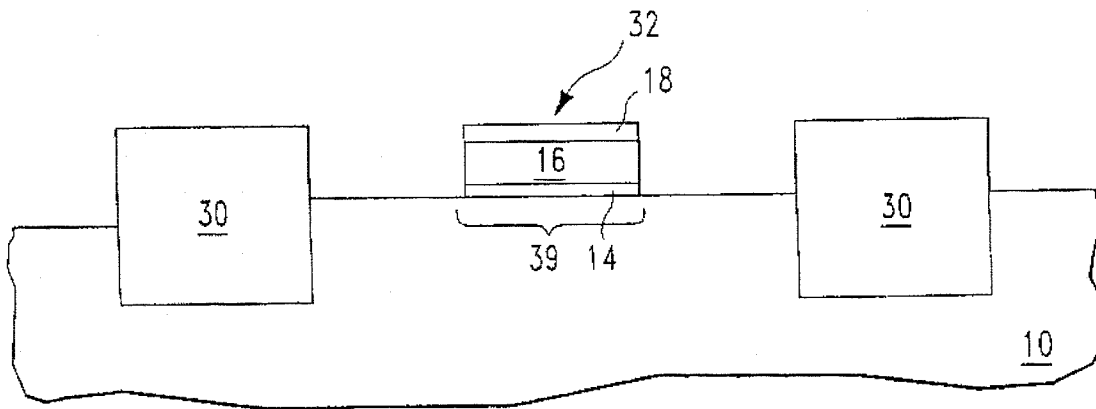


FIG. 5

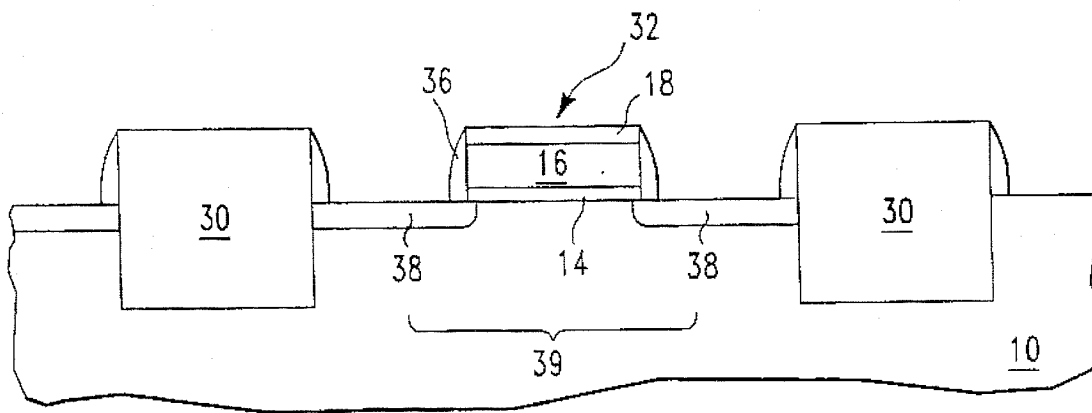


FIG. 6

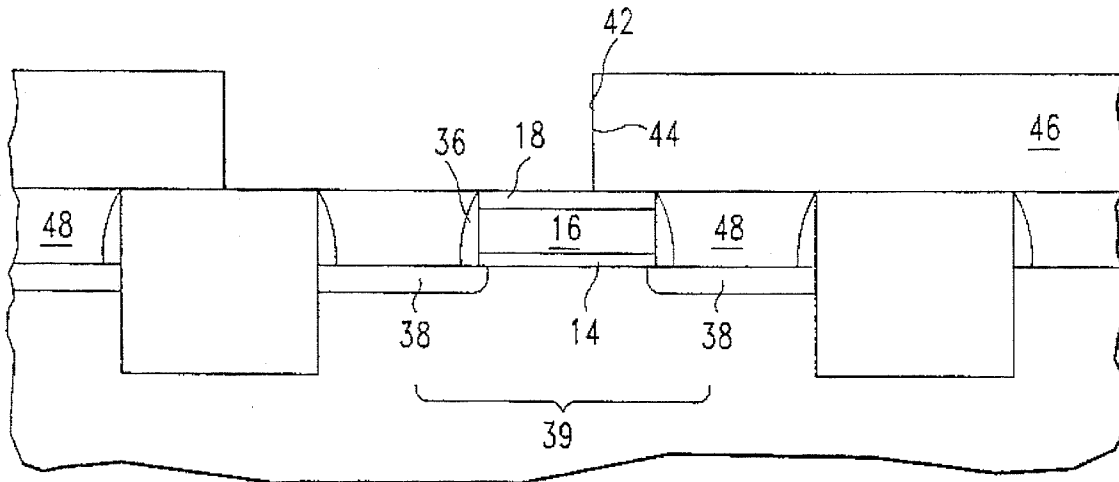


FIG. 7

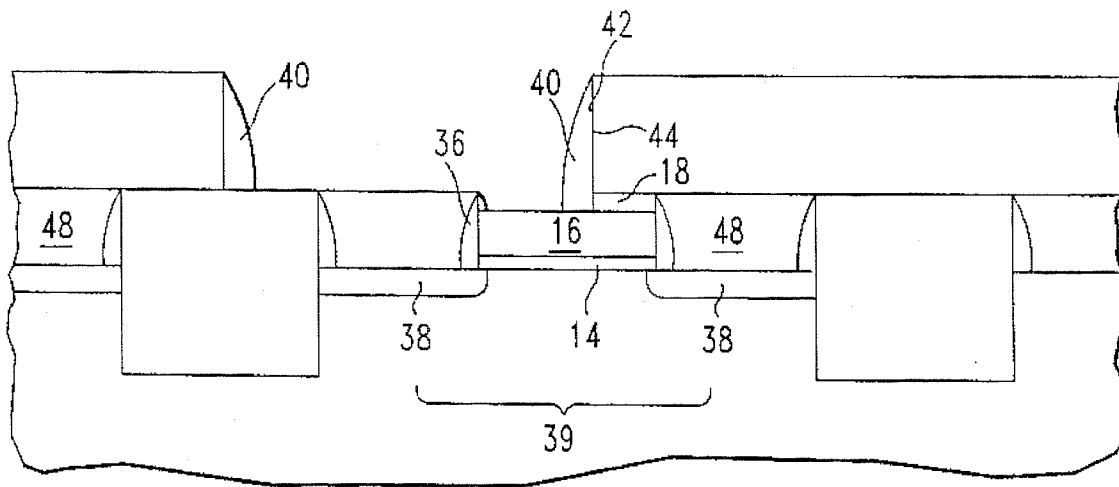


FIG. 8

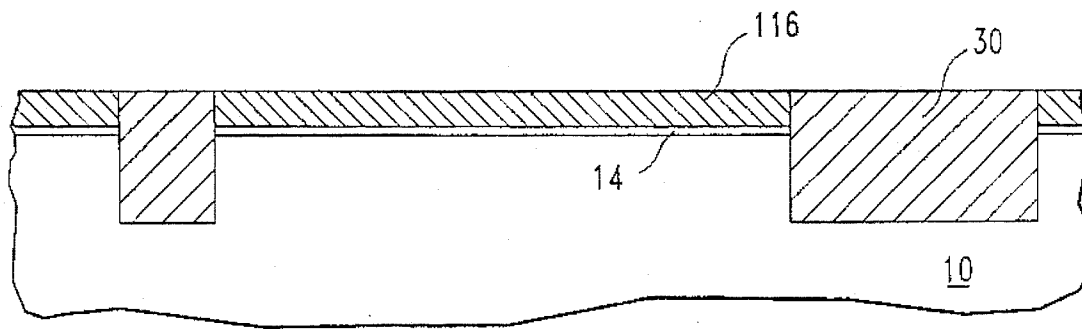


FIG. 9

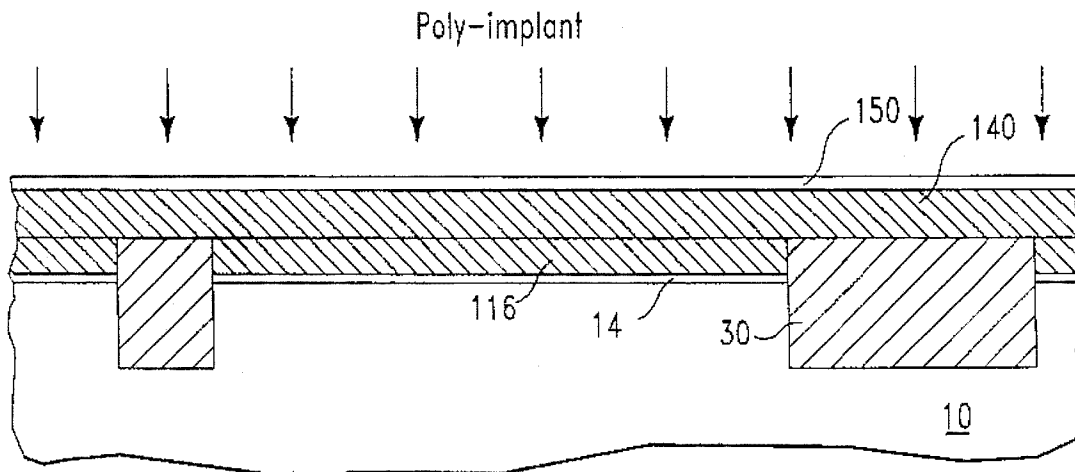


FIG. 10

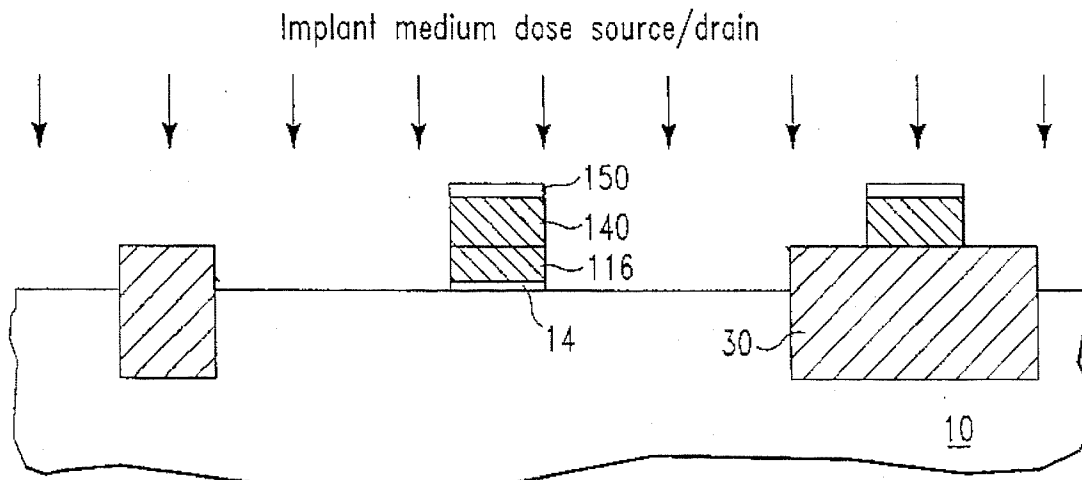


FIG. 11

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