United States Patent [19]

Nagasawa et al.

[11] **4,110,899**

[45] **Sep. 5, 1978**

[54] **METHOD FOR MANUFACTURING COMPLEMENTARY INSULATED GATE FIELD EFFECT TRANSISTORS**

[75] Inventors: **Kouichi Nagasawa**, Kunitachi; **Yasunobu Kosa; Satoshi Meguro**, both of Kodaira, all of Japan

[73] Assignee: **Hitachi, Ltd.**, Japan

[21] Appl. No.: **756,711**

[22] Filed: **Jan. 4, 1977**

[30] **Foreign Application Priority Data**

Jan. 12, 1976 [JP] Japan 51-2057

[51] **Int. Cl.**[2] **B01J 17/00**

[52] **U.S. Cl.** **29/571**

[58] **Field of Search** 29/571; 357/23, 41, 357/42, 50

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,913,211	10/1975	Seeds et al.	29/571
3,983,620	10/1976	Spadea	29/571
4,027,380	6/1977	Deal et al.	29/571

Primary Examiner—Gerald A. Dost

Attorney, Agent, or Firm—Craig & Antonelli

[57] **ABSTRACT**

Method for manufacturing complementary insulated gate field effect transistors of LOCOS (local oxidation of silicon) structure wherein after the formation of a well layer, an impurity having higher doping level than and the same conductivity type as a semiconductor substrate (well layer) is ion implanted at an area in the semiconductor substrate on which a field oxide layer is to be formed using a silicon nitride layer as a mask, and the semiconductor substrate surface is selectively thermally oxidized using the silicon nitride layer as a mask.

8 Claims, 6 Drawing Figures

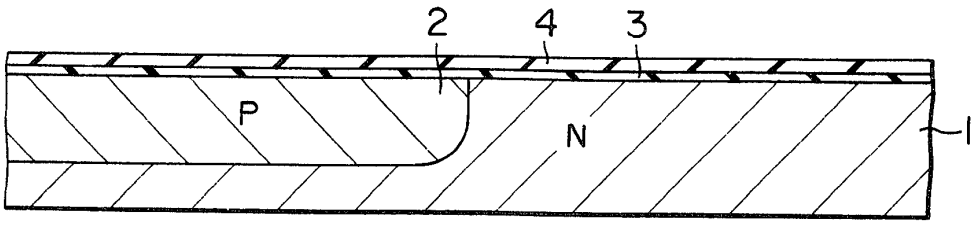


FIG. 1

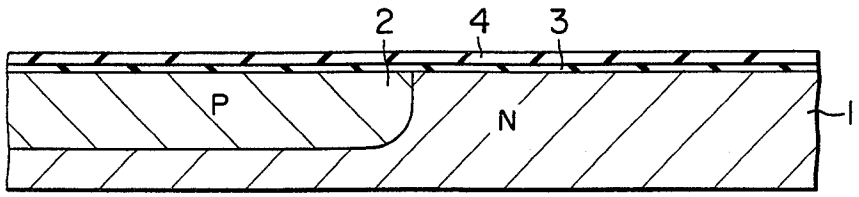


FIG. 2

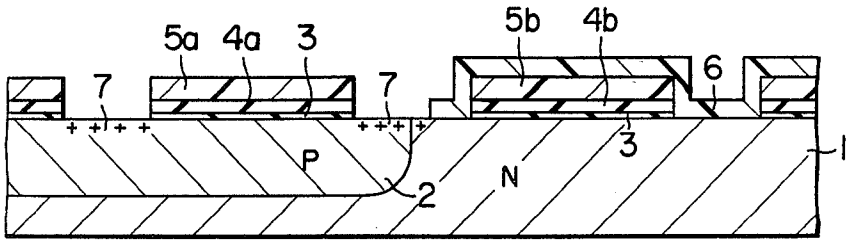


FIG. 3

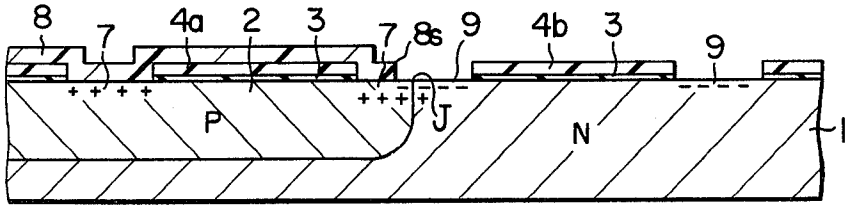


FIG. 4

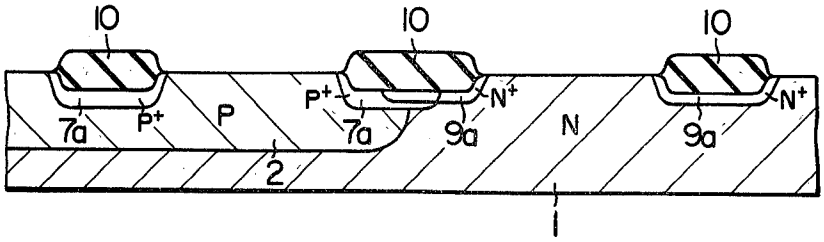


FIG. 5

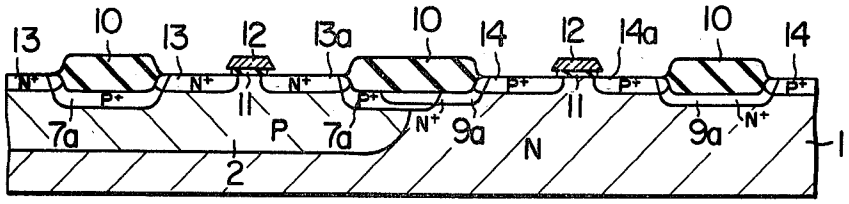
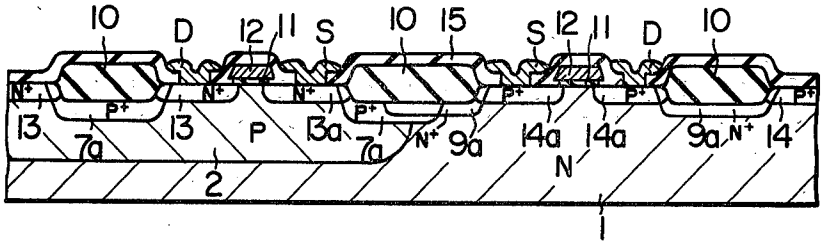


FIG. 6



METHOD FOR MANUFACTURING COMPLEMENTARY INSULATED GATE FIELD EFFECT TRANSISTORS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method for manufacturing complementary insulated gate field effect transistors (hereinafter referred to as CMIS FET's) having a field oxide layer of LOCOS (local oxidation of silicon) structure, and more particularly to a method for manufacturing a semiconductor integrated circuit device comprising such transistors.

2. Description of the Prior Art

In prior art CMIS FET's of the LOCOS structure, a power supply voltage therefor is determined by a threshold voltage V_{th} of an active region which is a channel region immediately beneath a gate electrode and a threshold voltage V_{th} of a parastic MOS FET in a field oxide layer region. Accordingly, when it is desired to raise the power supply voltage for the CMIS FET's, it is necessary to change the impurity concentration of a substrate and the impurity concentration of a well layer which is of opposite conductivity type to that of the substrate. Namely, the threshold voltage V_{th} is defined by

$$V_{th} = \frac{Q_{ss} + Q_b}{C_g} \quad (1)$$

where Q_b is a charge in a bulk, Q_{ss} is surface state and oxide charge, and C_g is the capacitance of the gate. A simple way to control the threshold voltage V_{th} defined by the equation (1) is to control Q_b. That is, Q_b is related to the impurity concentration of the substrate and it increases as the impurity concentration of the substrate increases. Accordingly, V_{th} can be increased by increasing the impurity concentration of the substrate.

Thus, when it is desired to raise the operation voltage, a voltage applied to a wiring layer extending over the field oxidation region also rises, resulting in a parastic channel immediately beneath the field oxide layer region. That is, a parastic MOS FET is formed. In order to avoid the formation of such a parastic MOS FET, it is necessary to increase the impurity concentration of the substrate or the impurity concentration of the well layer as seen from the above equation to raise the threshold voltage V_{th} of the parastic MOS FET. However, since the impurity concentrations of the substrate and the well layer are determined by electrical characteristics of the CMIS FET's such as the threshold voltage V_{th} and mutual conductance gm, the range of the operating voltage for the CMIS FET's is limited and the magnitude thereof is very small. For example, when the threshold voltage V_{th} of an N-channel MOS FET formed in a P-type well layer is 0.45 volts, a parastic channel is formed at about 4 volts because an N-type inversion layer is readily formed because of many sodium (+) ions present in the field oxide layer. As a result, the operating voltage should be up to about 3 volts.

As a commonly used method for manufacturing the CMIS FET's of the LOCOS structure which avoids the formation of the parastic channel in the P-type well layer and which can be practiced in a simple way, a technique disclosed in the Philips Technical Review, Vol. 34, No. 1, 1974, pp. 19-23, is known. According to the technique disclosed therein, particularly in the right column on page 20 and FIG. 2 on page 21, the P-type well layer is formed by ion implantation technology after the formation of the LOCOS oxide (field oxide) layer. Therefore, while the parastic channel is not readily formed, a complex design of layout for the MOS FET's and the wiring layers therefor is required when a plurality of MOS FET's are to be incorporated in the P-type well layer because LOCOS oxides cannot be formed in the P-type well layer. The operating voltage is also limited. That is, according to the disclosed technique, the operating supply voltage should be up to about 10 volts because as the operating voltage rises, the area immediately beneath the LOCOS oxide formed in the semiconductor body is more apt to form a parastic channel by a wiring layer extending over the LOCOS oxide layer although the above area is made more N-type conductive by sodium (+) ions present in the LOCOS oxide. Furthermore, due to the threshold voltage V_{th} of the active region in the P-type well layer, it becomes impossible to prevent the formation of the parastic channel in the P-type well as the operating voltage rises. Accordingly, the field of application of the semiconductor integrated circuit device manufactured by the disclosed technique is limited.

On the other hand, the field of application of the semiconductor integrated circuit device comprising CMIS FET's is wide in these days and, actually, the operating voltage therefor varies widely depending on the specification of a particular product. It is, therefor, required to manufacture CMIS FET's applicable to a variety of products of various specifications in a common process and provide CMIS FET's which are satisfactorily operable with a wide range of operating voltages. To this end, a method for manufacturing CMIS FET's which can control the threshold voltage V_{th} of the active region of the CMIS FET's and the threshold voltage V_{th} of the parastic MOS FET to predetermined voltages is required.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a method for manufacturing CMIS FET's of LOCOS structure which allows the establishment of the threshold voltage V_{th} of the parastic MOS FET in the field oxide layer region independently of the threshold voltage V_{th} of the active region whereby the operating voltage can be raised and the range thereof can be widened.

It is another object of the present invention to provide a method for manufacturing CMIS FET's of LOCOS structure suited for a semiconductor integrated circuit device comprising a number of CMIS FET's of LOCOS structure.

It is another object of the present invention to provide a method for manufacturing CMIS FET's of LOCOS structure suited for a semiconductor integrated circuit device operating at a high supply voltage.

It is another object of the present invention to provide a method for manufacturing CMIS FET's of LOCOS structure having less crystal defects.

It is another object of the present invention to provide a method for manufacturing CMIS FET's of LOCOS structure which allows a high integration density.

It is another object of the present invention to provide a method for manufacturing CMIS FET's of

LOCOS structure which is less influenced by contamination.

In order to achieve the above objects, the method of manufacturing the CMIS FET's of the LOCOS structure according to the present invention comprises the following steps of;

(1) forming a P(or N)-type well layer in a portion of an N(or P)-type semiconductor substrate surface and then forming a thin thermal oxidation layer over the entire surface and then forming a silicon nitride layer over the entire surface thereof,

(2) etching away the silicon nitride layer at areas on which field oxide layers are to be formed,

(3) ion implanting donor (or acceptor) and acceptor (or donor) impurities at those areas in the N(or P)-type semiconductor substrate and the P(or N)-type well layer on which the field oxide layers are to be formed,

(4) heat treating the substrate to selectively thermally oxidize the areas on which the field oxide layers are to be formed, using said silicon nitride layer as a mask, and

(5) removing the silicon nitride layer formed in the step (1) and the thin thermal oxidation film beneath the silicon nitride layer and then forming a gate insulation layer, a source region and a drain region of a MIS device in the N(or P)-type semiconductor substrate and the P(or N)-type well layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1** through **6** show one embodiment of the present invention illustrating a sequence of steps, in partial sectional views, of manufacturing a semiconductor integrated circuit device comprising a plurality of CMIS FET's of LOCOS structure.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The method for manufacturing a CMIS FET IC of LOCOS structure of the present invention is now explained in the order of manufacturing steps.

(a) A portion of a surface of an N-type silicon substrate is delimited, in which a P-type well layer **2** of a thickness of about 6-8 μm is formed by ion implantation technique. Thereafter, the surface of the substrate is thermally oxidized in a dry O_2 atmosphere at about 1000° C. to form a silicon oxide (SiO_2) layer **3** of the thickness of about 700 Å. Then, a silicon nitride (Si_3N_4) layer **4** of the thickness of about 1000 Å - 1400 Å is formed by vapor reaction on the layer **3**. (FIG. **1**)

(b) The Si_3N_4 layer **4** and the SiO_2 layer **3** therebeneath are etched away except at areas **4***a* and **4***b* on which field oxide layers are to be formed, using a photoresist layer **5** (**5***a* and **5***b*) as a mask. Then, that portion of the surface of the substrate **1** on which a P-channel MOS device is to be formed is covered with a photoresist layer **6**, and then boron (B) impurity **7** is ion implanted at 75KeV at that area of the surface of the substrate **1** on which the field oxide layer of the N-channel MOS device is to be formed, using, as a mask, a photoresist layer **6** and the photoresist layer **5***a* which has been used in etching the Si_3N_4 layer **4** and the underlying SiO_2 layer **3** so that a surface impurity concentration of about 2×10^{13} atoms/cm^2 to 5×10^{13} atoms/cm^2 is obtained at the said area. (FIG. **2**)

(c) After removing the photoresist layers **5** and **6**, a new photoresists layer **8** is selectively formed on that portion of the surface of the substrate **1** in which the N-channel MOS device is to be formed. Then, using the selectively formed photoresist layer **8** and the silicon nitride (Si_3N_4) layer under which the P-channel MOS device is to be formed as a mask, phosphorus (P) impurity **9** is ion implanted at 45KeV in that portion of the surface of the substrate **1** on which the field oxide layer of the P-channel MOS device is to be formed. (FIG. **3**) The ion implantation energy of 45KeV for the phosphorus impurity is enough to obtain an area of a sufficiently high surface impurity concentration. On the other hand, with the acceleration energy of below 60KeV, phosphorus ions can be masked only by the Si_3N_4 layer or the SiO_2 layer. Accordingly, the photoresist layer need not be maintained on the Si_3N_4 layer **4***b*. This means that the alignment of the mask used in exposing step for the photoresist layer **8** need not be highly accurate. That is, an edge **8S** of the photoresist layer **8** may extend beyond a PN junction J between the P-type well layer **2** and the N-type substrate **1**.

(d) After removing the photoresist layer **8**, the substrate **1** is oxidized in a wet oxygen atmosphere at 1000° C. for about 7.5 hours to form selective silicon oxide (SiO_2) layers **10** of a thickness of about 1.4 μm of LOCOS structure (FIG. **4**). In this case, because of the masking action of the Si_3N_4 layer **4** to the oxygen, silicon oxide (SiO_4) layer is not formed on the areas covered with the Si_3N_4 layer **4**. Then, the selective oxidation mask of the Si_3N_4 layer **4** and the underlying thin SiO_2 layer **3** are removed (FIG. **4**).

Through the heat treatment for forming the thick SiO_2 layers **10** of the LOCOS structure, the impurities which have been ion implanted in the previous step are activated and diffused so that P^+-type field diffusion layers **7***a* and N^+-type field diffusion layers **9***a*, which act as parastic channel stopper layers, are formed (FIG. **4**).

(e) On the surface of the substrate **1**, gate oxide layers **11** of a thickness of about 1000 Å are formed in a dry O_2 atmosphere at 1000° C. Then, on the surfaces of the gate oxide layers **11**, polycrystalline silicon layers **12** are deposited to a thickness of about 3500 Å. the polycrystalline silicon layers are then etched away by photoetching except those areas which are to act as gate electrodes. Etching is again carried out using the remaining polycrystalline silicon layers **12** as a mask to remove the gate oxide layers **11** on the source and drain regions. The drain regions **13**, **14** and the source regions **13***a*, **14***a* of the MOS devices are then formed using the thick field oxide layers **10** and the polycrystalline silicon layers **12** as a mask (FIG. **5**).

The formation of the drain regions **13**, **14***a* and the source regions **13***a*, **14** of the P-channel and N-channel MOS devices, respectively, is explained in more detail. A photoresist layer is formed on an area in which the N-channel MOS device is to be formed. Those portions of the gate oxide layer **11** which correspond to the source and drain regions of the P-channel MOS device are removed. Then, phosphorus impurity is diffused in the exposed surface of the substrate **1** using the polycrystalline silicon layer **12** for the gate electrode G_1 and portions of the field oxide layers **10** as a diffusion mask, to form the source region **14** and the drain region **14***a*. In this manner, the P-channel MOS device is formed. Then, the photoresist layer is removed and new photoresist layers are formed on the source region **14** and the drain region **14***a*, and the portions of the gate oxide layer **11** which correspond to the source and drain regions of the N-channel MOS device are removed. Thereafter, using the polycrystalline silicon layer **12** for the gate electrode G_2 of the P-channel MOS device and

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.