



US005153145A

United States Patent [19]

[11] Patent Number: **5,153,145**

Lee et al.

[45] Date of Patent: **Oct. 6, 1992**

- [54] FET WITH GATE SPACER 0101077 5/1986 Japan .
- [75] Inventors: **Kuo-Hua Lee; Chih-Yuan Lu; Janmye Sung**, all of Lower Macungie Township, Lehigh County, Pa.
- [73] Assignee: **AT&T Bell Laboratories**, Murray Hill, N.J.
- [21] Appl. No.: **422,834**
- [22] Filed: **Oct. 17, 1989**
- [51] Int. Cl.⁵ **H01L 21/24; H01L 21/265; H01L 21/336**
- [52] U.S. Cl. **437/44; 437/41; 437/200**
- [58] Field of Search **437/34, 27, 28, 29, 437/30, 40, 41, 44, 56, 67, 235, 238, 239, 241, 186, 196, 200; 357/23.3, 23.4; 148/DIG. 147**

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Primary Examiner—Olik Chaudhuri
Assistant Examiner—M. Wilczewski
Attorney, Agent, or Firm—John T. Rehberg

[57] **ABSTRACT**

A semiconductor integrated circuit structure and method of fabrication is disclosed. The structure includes a FET gate with adjacent double or triple-layered gate spacers. The spacers permit precise tailoring of lightly doped drain junction profiles having deep and shallow junction portions. In addition, a self-aligned silicide may be formed solely over the deep junction portion thus producing a reliable low contact resistance connection to source and drain.

5 Claims, 5 Drawing Sheets

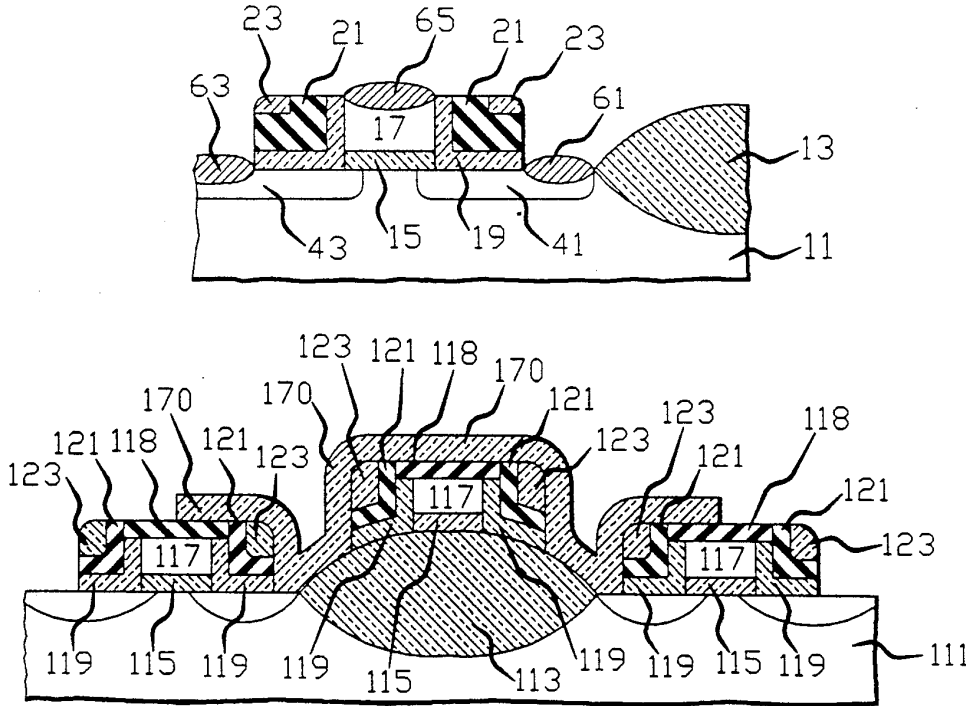


FIG. 1

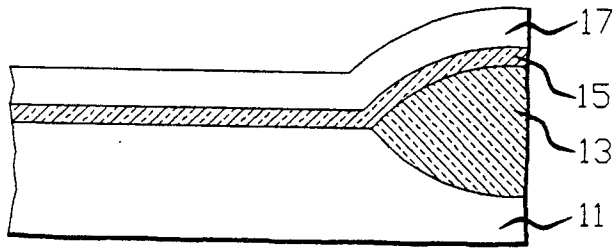


FIG. 2

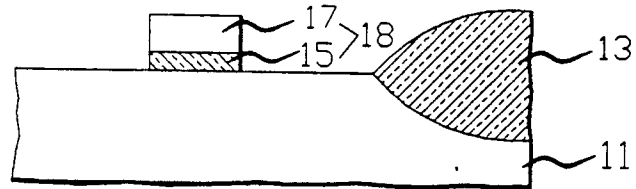


FIG. 3

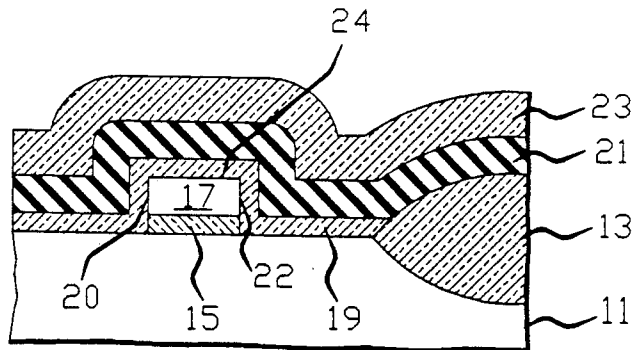


FIG. 4

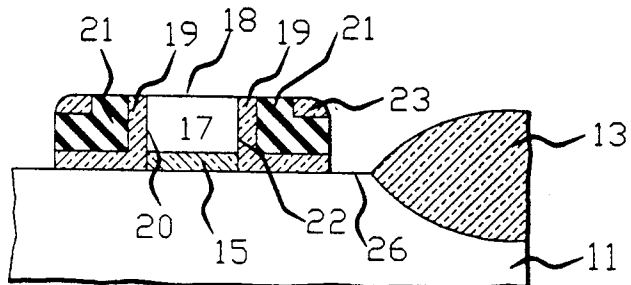


FIG. 5

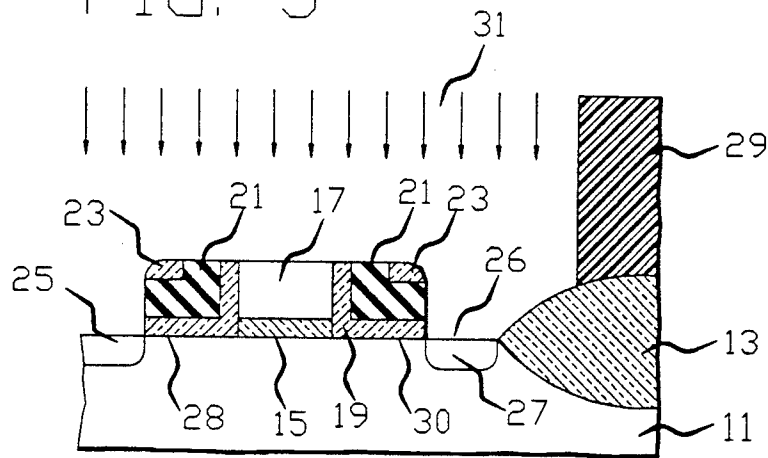


FIG. 6

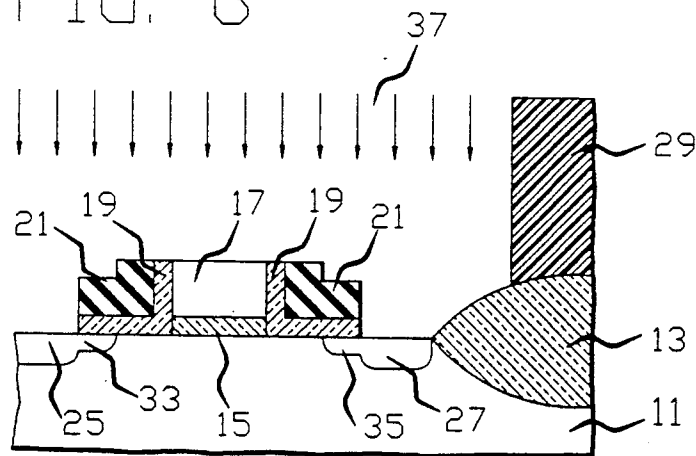


FIG. 7

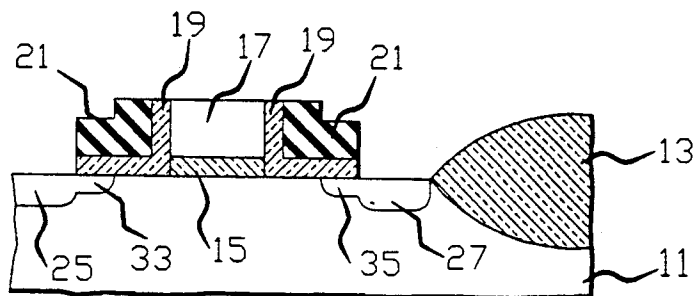


FIG. 8

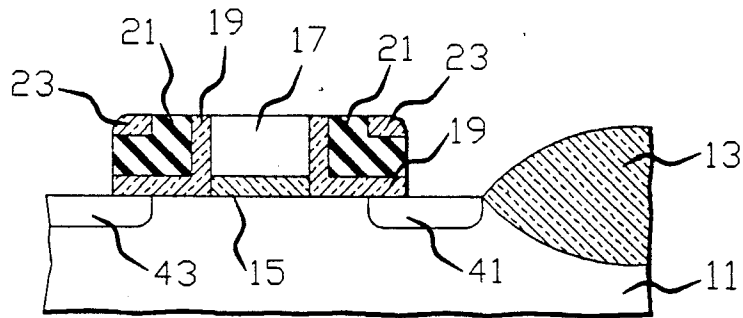


FIG. 9

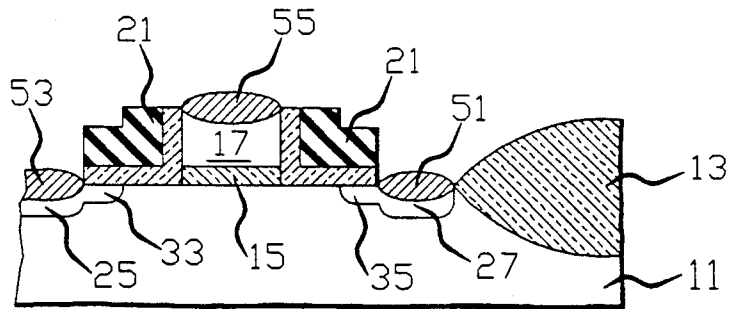


FIG. 10

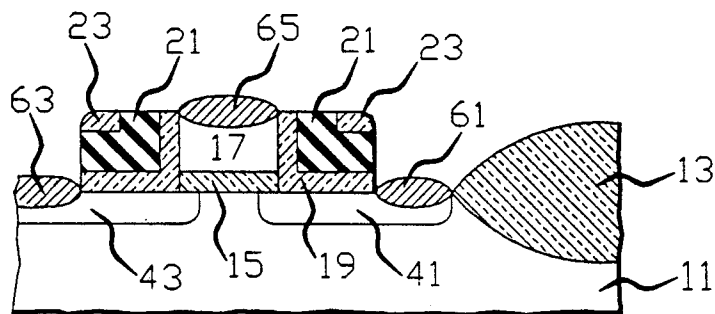


FIG. 11

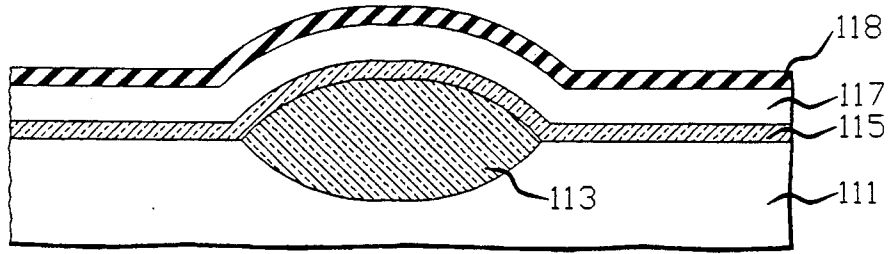


FIG. 12

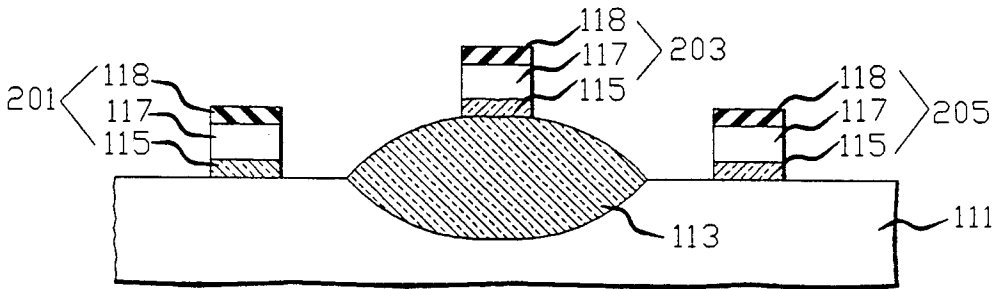
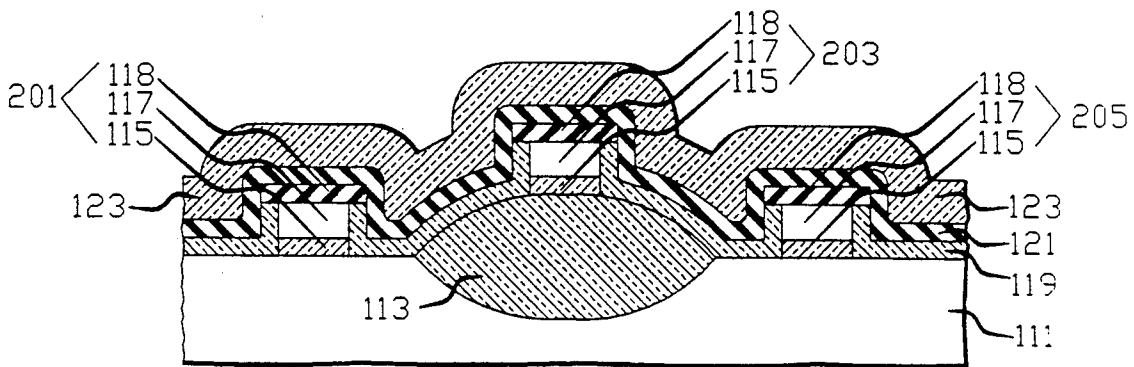


FIG. 13



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