United States Patent [19]

Iyer

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[54] **GATE ELECTRODE SIDEWALL ISOLATION SPACER FOR FIELD EFFECT TRANSISTORS**

[75] Inventor: **Subramanian S. Iyer**, Mt. Kisco, N.Y.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **763,897**

[22] Filed: **Aug. 9, 1985**

Related U.S. Application Data

[63] Continuation of Ser. No. 447,543, Dec. 7, 1982, abandoned.

[51] **Int. Cl.**[4] **H01L 29/94**; H01L 29/78

[52] **U.S. Cl.** **357/54**; 357/23.3; 357/23.9; 357/59; 357/23.1

[58] **Field of Search** 357/54, 59, 23.3, 23.9, 357/23.1

[56] **References Cited**

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Primary Examiner—Martin H. Edlow
Assistant Examiner—Charles S. Small, Jr.
Attorney, Agent, or Firm—Pollock, Vande Sande & Priddy

[57] **ABSTRACT**

A sidewall isolation structure for field effect transistor which includes a first electrical insulating layer and a second electrical insulating layer contiguous with the first layer. The second electrical insulating material is etched above or below the surface level of the first insulating layer to provide recesses in the sidewall isolation structure, and method for the preparation thereof.

11 Claims, 8 Drawing Figures

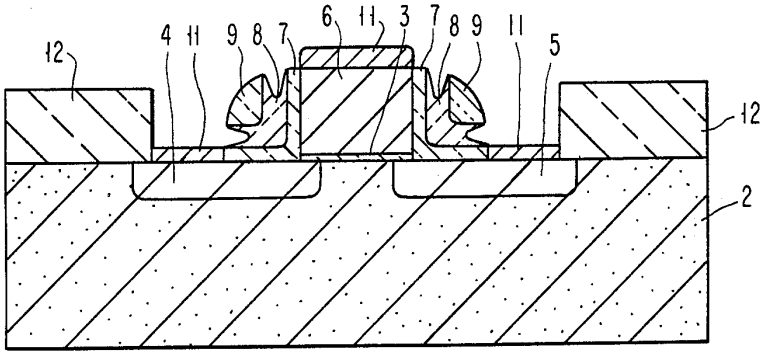


FIG. 1

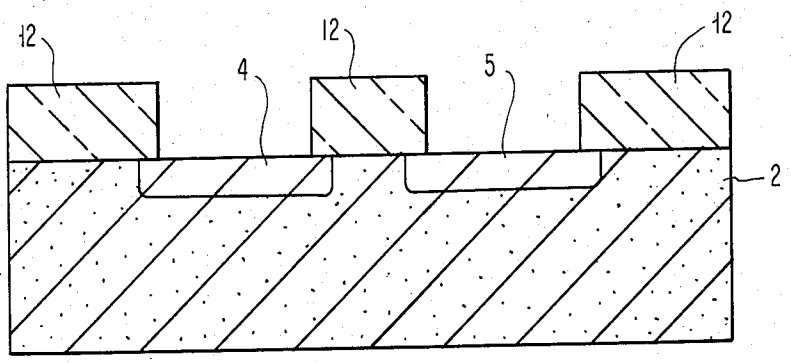


FIG. 2

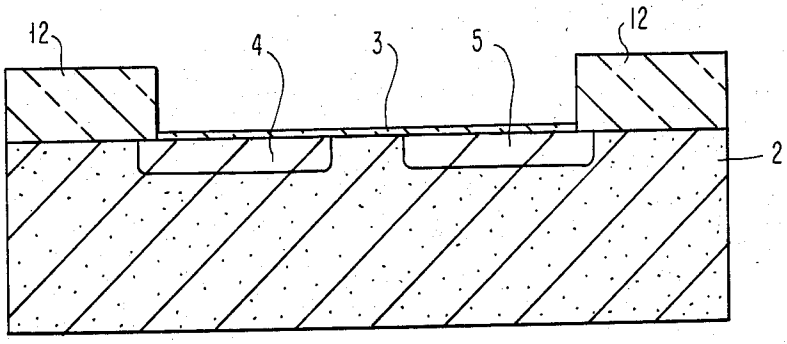


FIG. 3

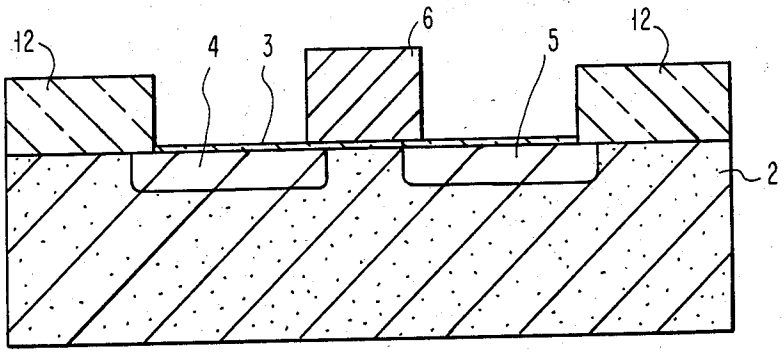


FIG. 4

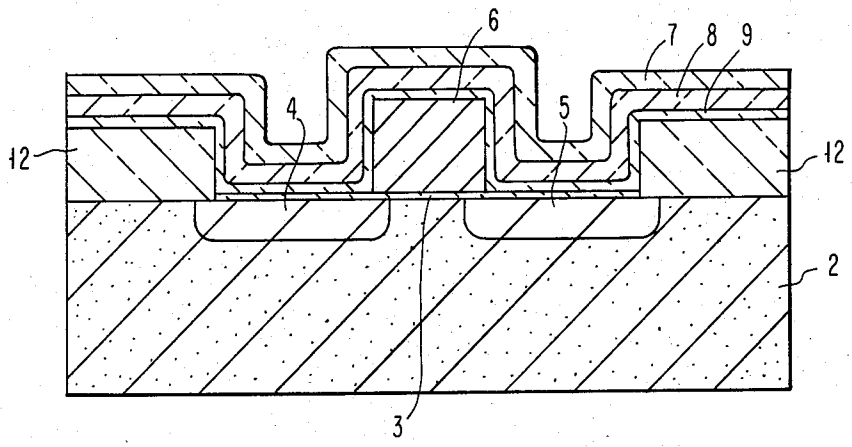


FIG. 5

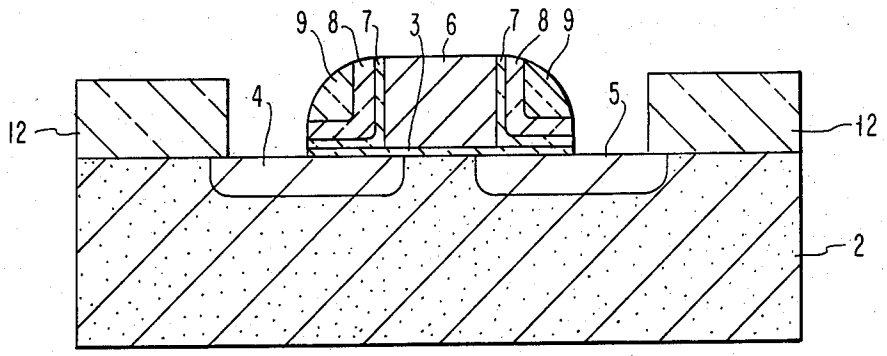


FIG. 6

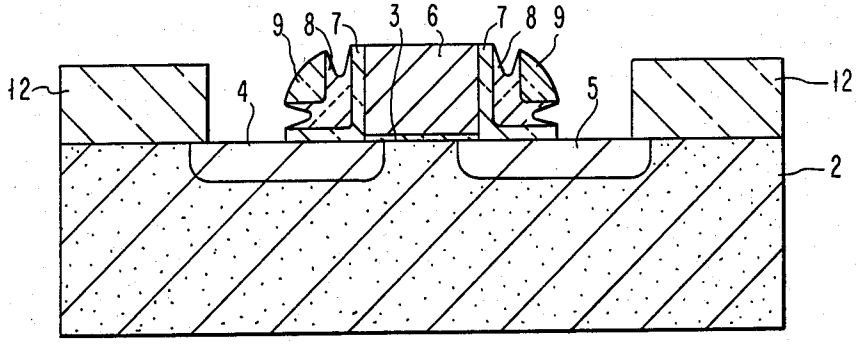


FIG. 7

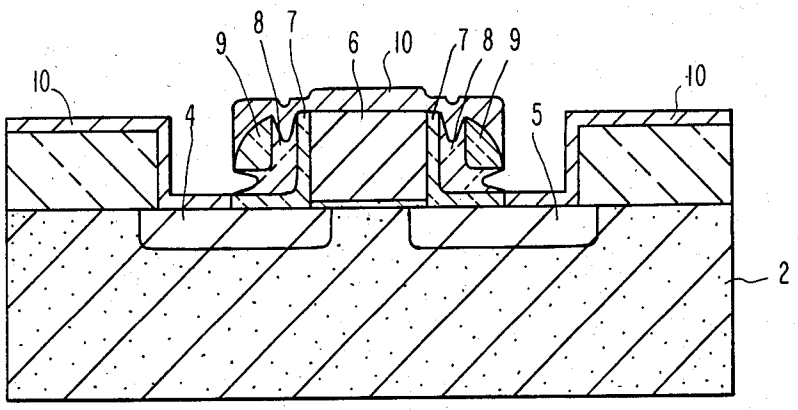
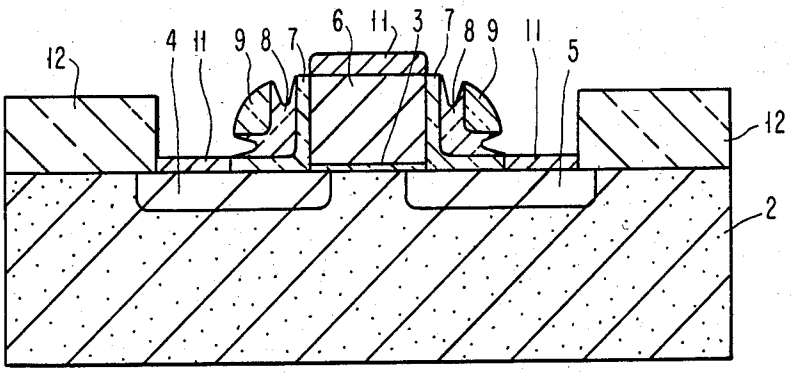


FIG. 8



GATE ELECTRODE SIDEWALL ISOLATION SPACER FOR FIELD EFFECT TRANSISTORS

This application is a continuation of application Ser. No. 447,543, filed Dec. 7, 1982, now abandoned.

DESCRIPTION

1. Technical Field

The present invention is concerned with certain sidewall isolation structures for field effect transistors. In particular, the present invention is concerned with a sidewall isolation structure for field effect transistors which structure contains a plurality of electrical insulating materials. The present invention is also concerned with a process for fabricating the sidewall isolation structure and, particularly, for fabricating a sidewall isolation structure having a plurality of insulating materials.

2. Background Art

The metallic type electrical connections to the source, drain, and gate regions of a field effect transistor can be achieved by various processes. One such procedure involves the selective reaction of a metal such as titanium, cobalt, palladium, or nickel with exposed silicon to obtain self-aligned contacts to the source, drain, and gate regions of the device. Achieving self-alignment is significant in the fabrication of field effect transistors since one of the most crucial steps in preparing FET devices is a lithographic masking step which requires high precision in registration (i.e., relative mask-to-mask alignment) and extreme care in execution.

With respect to the above procedure for achieving self-alignment of metallic type contacts to the source, drain, and gate regions of a FET device, it is important to maintain the electrical isolation of the gate from the source and drain regions. This is accomplished by providing an isolation or electrical insulation layer on the sidewalls of the gate (which can be referred to as "spacer") and between the gate and semiconductor substrate. To obtain self-aligned contacts, a metal is deposited over the entire region (the source, drain, gate, and over the sidewall isolation between the gate and the source and drain regions). Subsequent to this, the metal is reacted with the available exposed silicon which it contacts to form a metallic silicide. Since the sidewalls are of an isolation material such as an oxide or nitride, reaction between the metal and the sidewall should not occur to form silicide. Subsequent to this, the unreacted metal on the sidewall isolation can then be selectively etched away.

However, it has been observed in attempting to prepare devices by the procedure discussed above, that although free silicon is not present on the sidewalls, nonetheless, metallic silicides have formed thereon. This, in turn, causes electrical leakage between the source, drain, and gate areas across the spacer paths. It is not entirely understood as to what causes the silicide formation on the sidewalls, but it is believed that possibly silicon is diffused through the metal on the sidewall due to the temperature of the silicide formation and this leads to silicide formation there. This is particularly noticeable when employing metals such as cobalt and titanium to form the silicide.

DISCLOSURE OF INVENTION

In order to prevent possible diffusion paths on the silicon over the spacer and thereby eliminating electrical leakage across the spacer, the present invention provides a discontinuous metal film over the sidewall isolation layer rather than a continuous metal film as obtained in accordance with the above discussed technique.

Providing a discontinuous film over the sidewall isolation spacer prevents the formation of a continuous silicon diffusion path over the spacer. This prevents the formation of a continuous silicide film over the spacer and thereby precludes electrical leakage across the spacer after the unreacted metal has been selectively etched away.

This discontinuous path is created by recessing the sidewall isolation layer so that metal deposited thereon would be discontinuous over the isolation region. In particular, the sidewall isolation is fabricated of at least two different materials and the composite isolation region is then selectively etched in order to create a recess therein.

In particular, the present invention is concerned with a sidewall isolation structure for field effect transistors which structure comprises a first electrical insulating material and a second and different electrical insulating material. The second electrical insulating material is contiguous with and preferably embedded in the first electrical insulating material. Moreover, the second electrical insulating material is etched above or preferably below the surface level of the first electrical insulating material to provide a recess in the sidewall isolation structure. This, in turn, prevents the formation of a continuous metal film over the sidewall isolation structure.

Another aspect of the present invention is a process for preparing sidewall isolation for field effect transistors. The process comprises providing a first electrical insulating layer over at least the sidewalls of an electrically conductive region. A second and different electrical insulating layer is provided adjacent the first electrical insulating layer on at least the sidewalls of the conductive region.

Although the present invention can be practiced with only two layers, it is preferred to provide a third electrical insulating layer adjacent the second and different insulating layer on at least the sidewalls. The third electrical insulating layer, if provided, can have substantially the same or a different etch rate as does the second insulating layer or the first insulating layer. However, it is preferred that such a third layer have an etch rate substantially the same as that of the first electrical insulating layer. The layers are then etched whereby the second layer is etched at a rate different than the first layer to thereby provide recesses in the sidewall isolation. Preferably the second layer is etched at a rate faster than the first layer and third layer, if present, resulting in a recess below the surface level of the first and third layers.

BRIEF DESCRIPTION OF DRAWINGS

FIGS. **1–8** are cross-sectional views of a simplified field effect transistor in various stages of fabrication according to the present invention.

BEST AND VARIOUS MODES FOR CARRYING OUT INVENTION

For convenience, the discussion of the fabrication steps is directed to the preferred aspect of employing a p-type silicon substrate as the semiconductive substrate and n-type impurities. This leads to the n-channel FET

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