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United States Patent [19]

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Mandelman et al.

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[54] **CORNER PROTECTED SHALLOW TRENCH ISOLATION DEVICE**

4-56279 2/1992 Japan 257/622

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[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **348,709**

[22] Filed: **Dec. 2, 1994**

[51] Int. Cl.⁶ **H01L 29/00**

[52] U.S. Cl. **257/510; 257/513; 257/622; 257/623; 257/626**

[58] Field of Search **257/301, 302, 257/303, 304, 305, 905, 510, 513, 524, 622, 623, 626, 647**

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Attorney, Agent, or Firm—James M. Leas

[57] ABSTRACT

A semiconductor structure to prevent gate wrap-around and corner parasitic leakage comprising a semiconductor substrate having a planar surface. A trench is located in the substrate, the trench having a sidewall. An intersection of the trench and the surface forms a corner. A dielectric lines the sidewall of the trench. And, a corner dielectric co-aligned with the corner extends a subminimum dimension distance over the substrate from the corner.

10 Claims, 5 Drawing Sheets

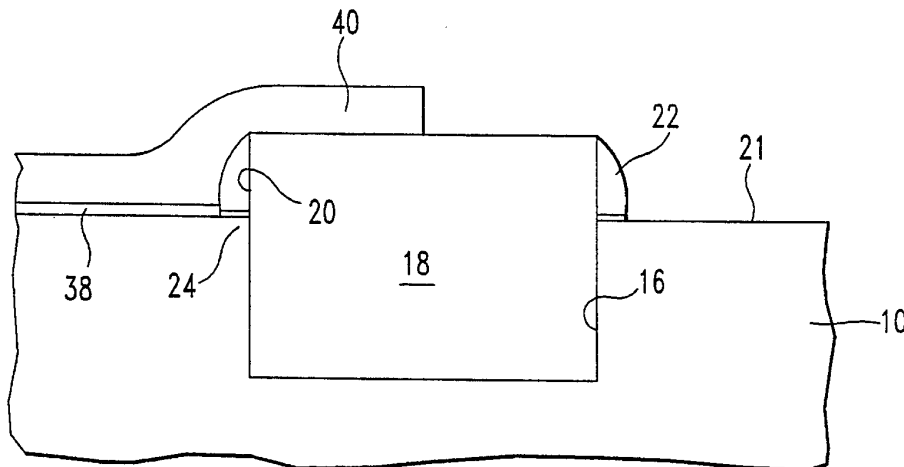


FIG. 1a

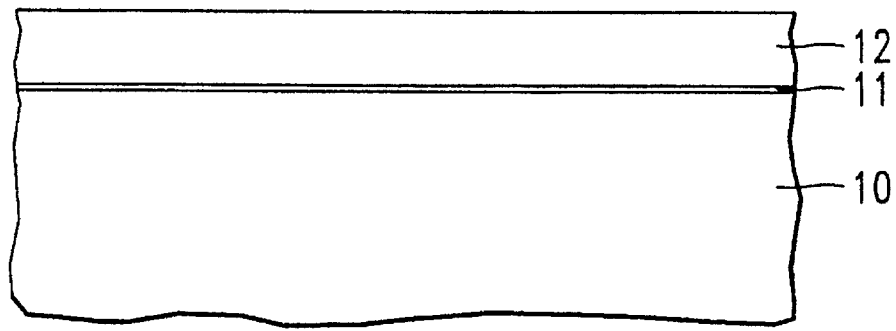


FIG. 1b

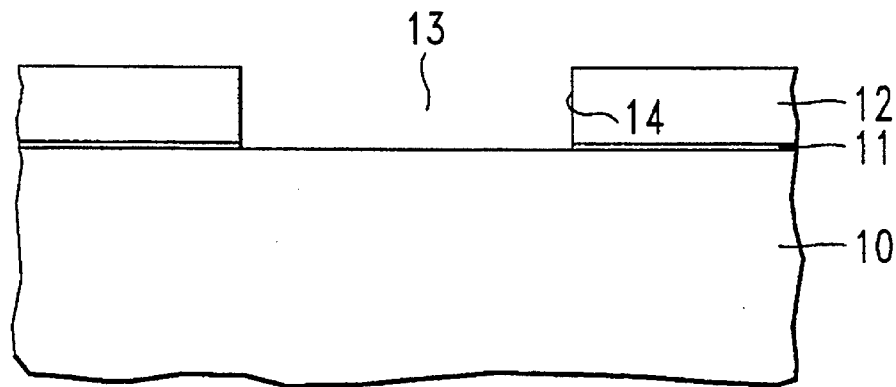
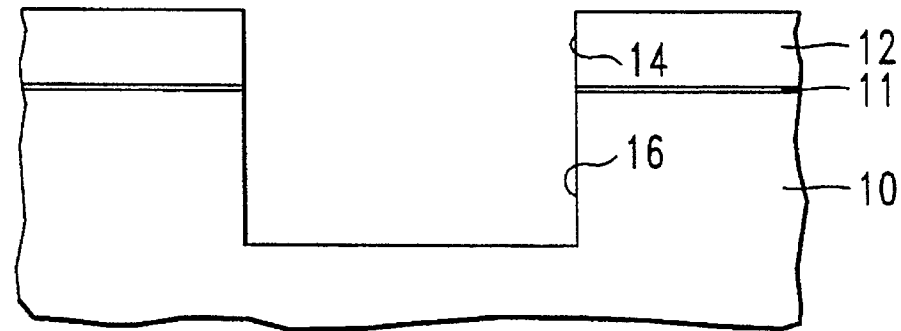


FIG. 1c



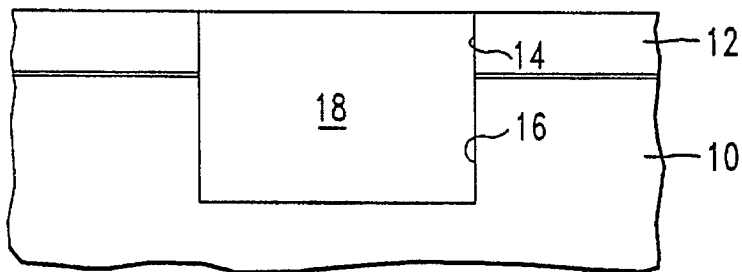


FIG. 1d

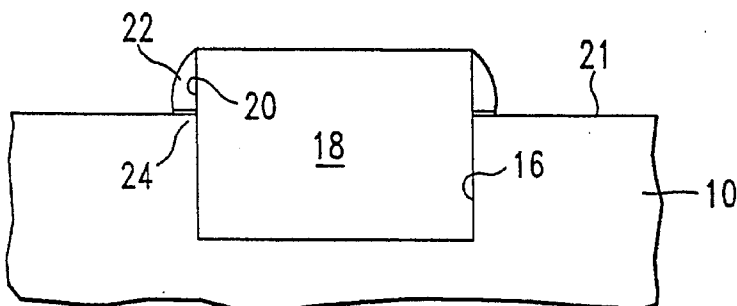


FIG. 1e

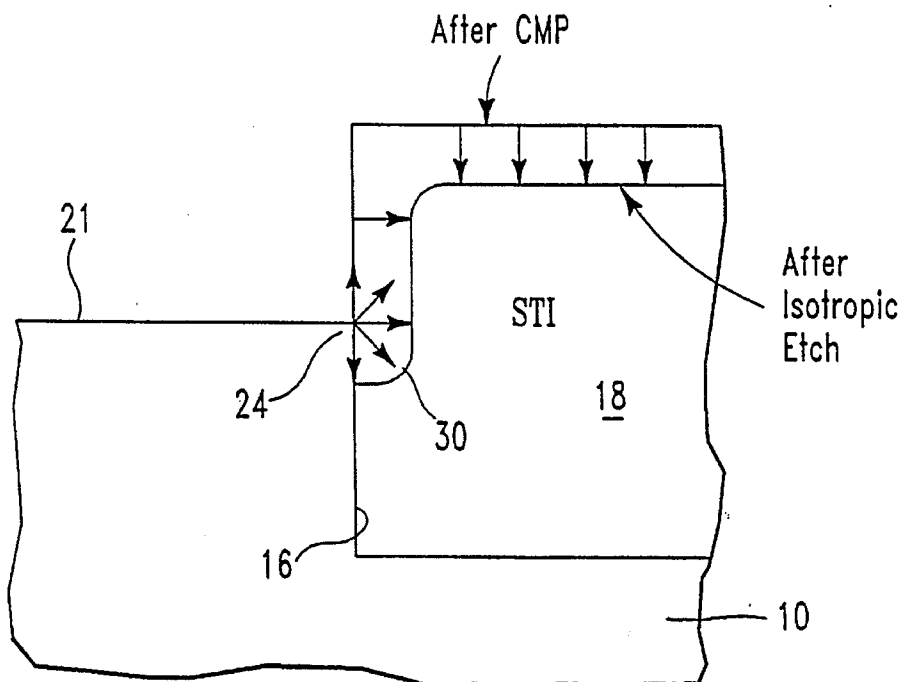
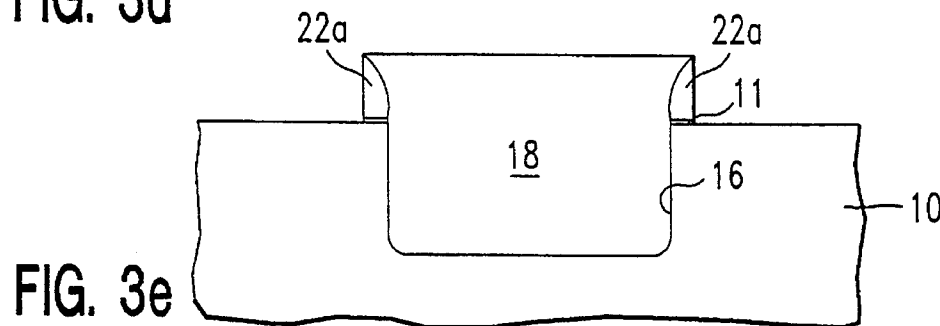
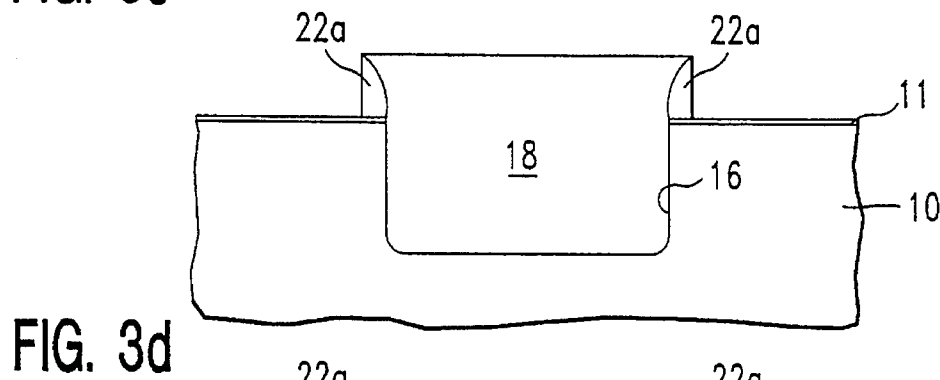
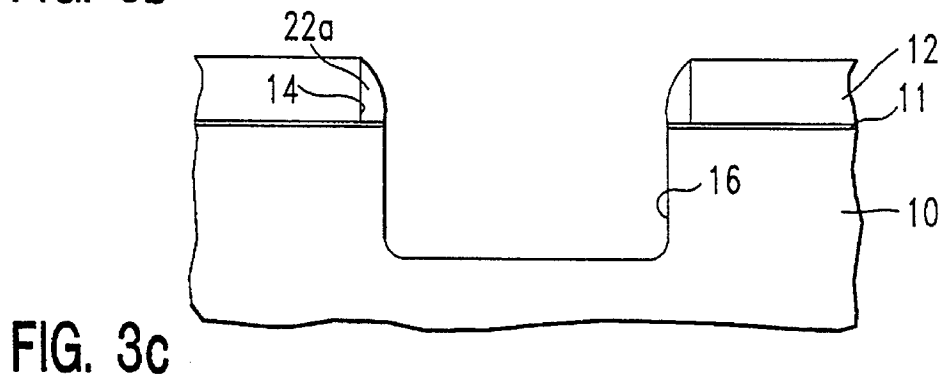
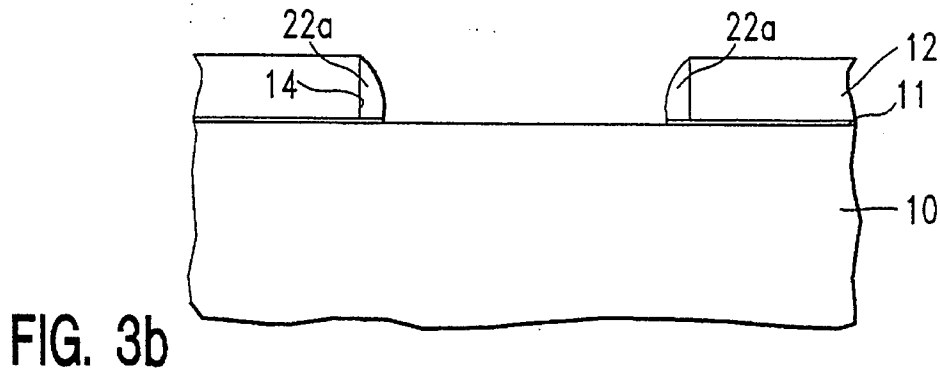
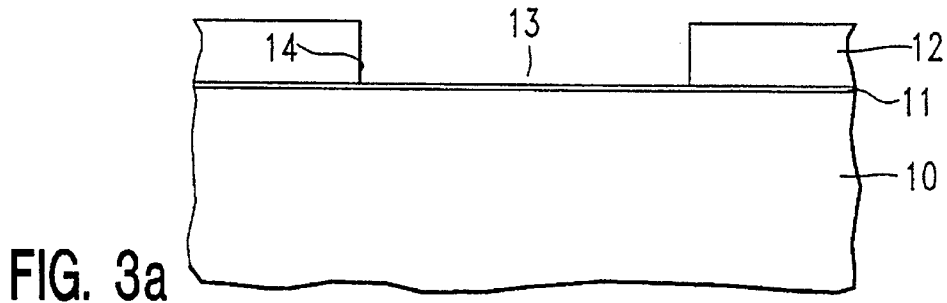


FIG. 2
PRIOR ART



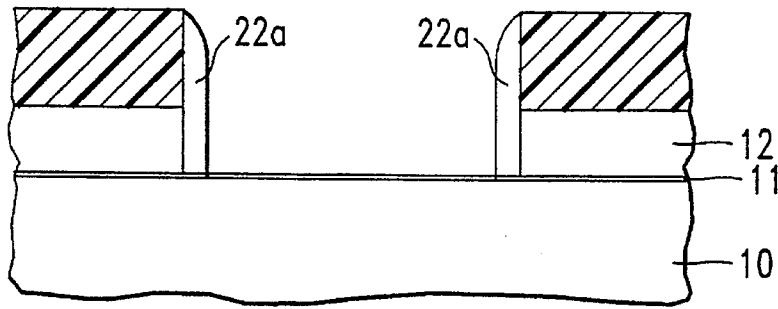


FIG. 4a

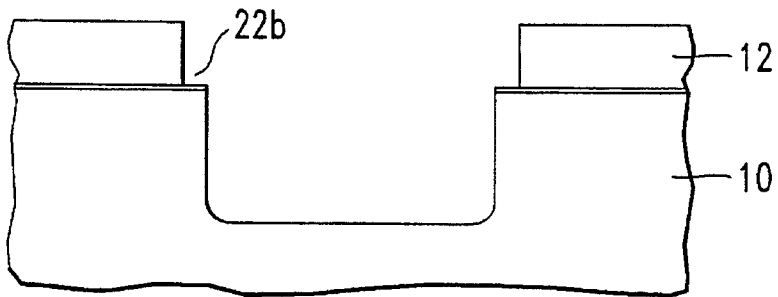


FIG. 4b

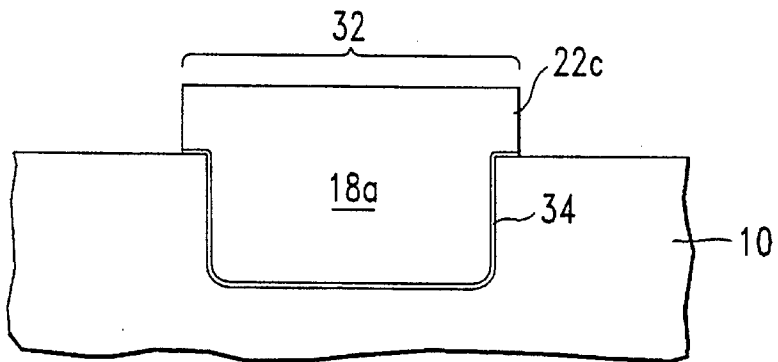


FIG. 4c

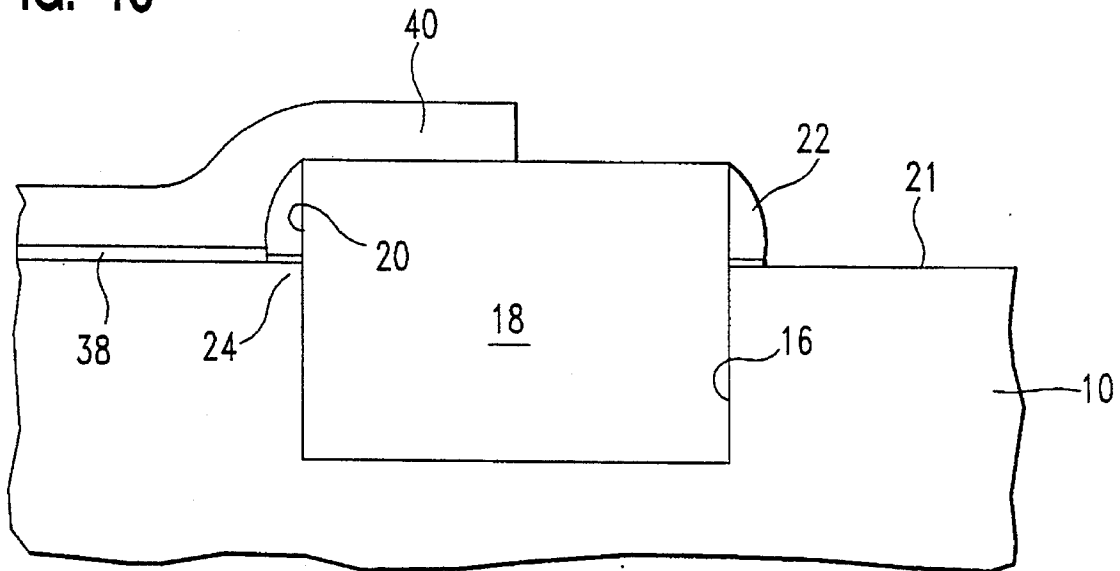


FIG. 5

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