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United States Patent [19]

[11] **Patent Number:** **5,539,229**

Noble, Jr et al.

[45] **Date of Patent:** **Jul. 23, 1996**

[54] **MOSFET WITH RAISED STI ISOLATION SELF-ALIGNED TO THE GATE STACK**

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Ashwin K. Ghatalia; **Badih El-Kareh**,
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[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

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Attorney, Agent, or Firm—James M. Leas

[21] Appl. No.: **365,729**

[22] Filed: **Dec. 28, 1994**

[51] **Int. Cl.**⁶ **H01L 27/08**; H01L 29/76;
H01L 29/00

[52] **U.S. Cl.** **257/301**; 257/305; 257/397;
257/623

[58] **Field of Search** 257/301, 304,
257/305, 395, 396, 397, 398, 383, 385,
586, 587, 619, 623, 384

[57] ABSTRACT

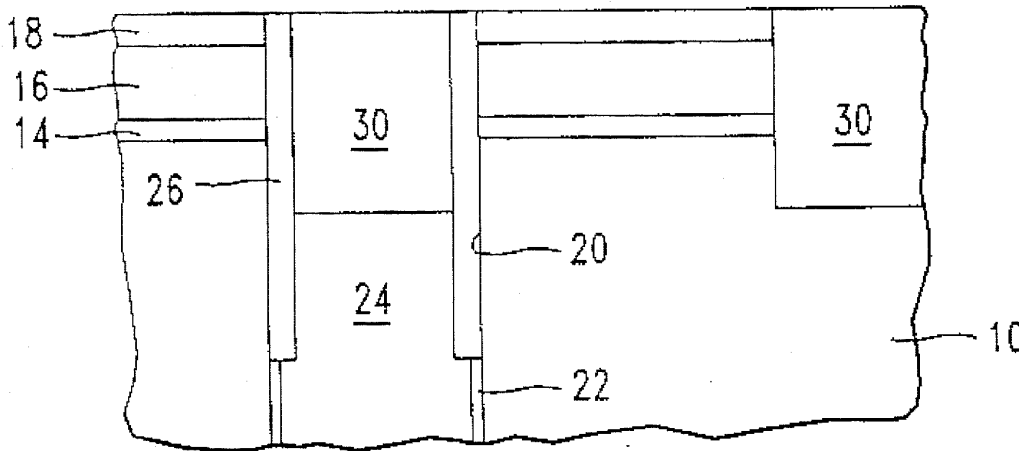
A semiconductor structure comprising a transistor having a gate conductor that has first and second edges bounded by raised isolation structures (e.g. STI). A source diffusion is self-aligned to the third edge and a drain diffusion is self-aligned to the fourth edge of the gate electrode.

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19 Claims, 5 Drawing Sheets



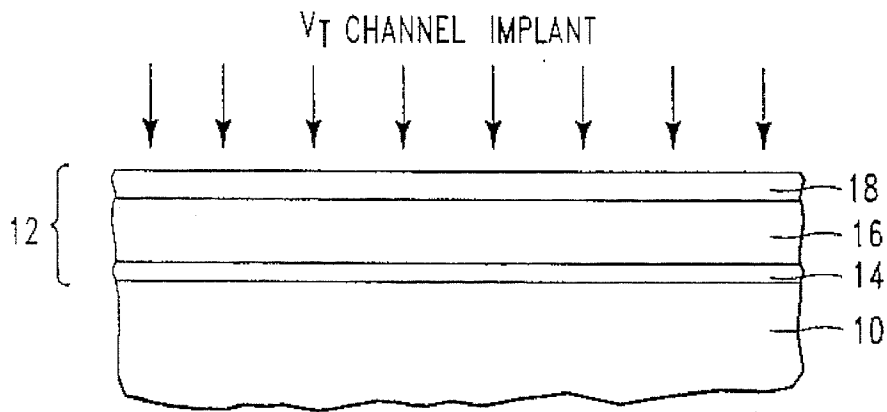


FIG. 1

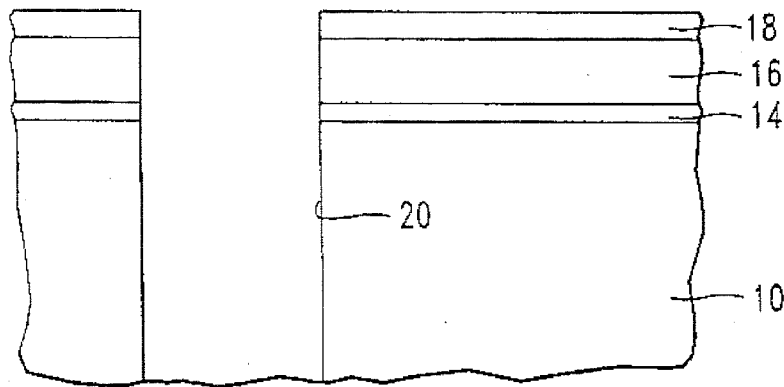


FIG. 2

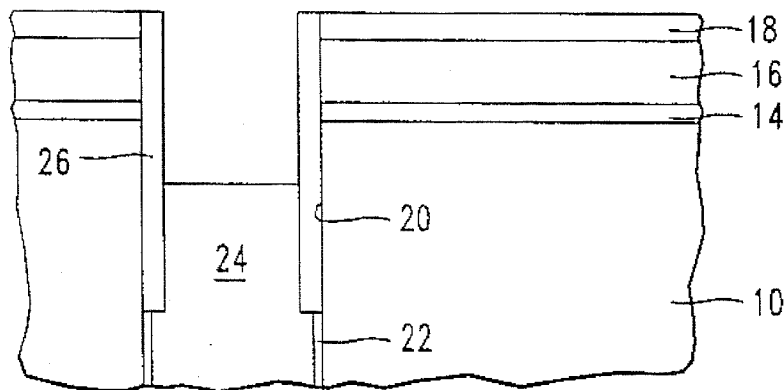


FIG. 3

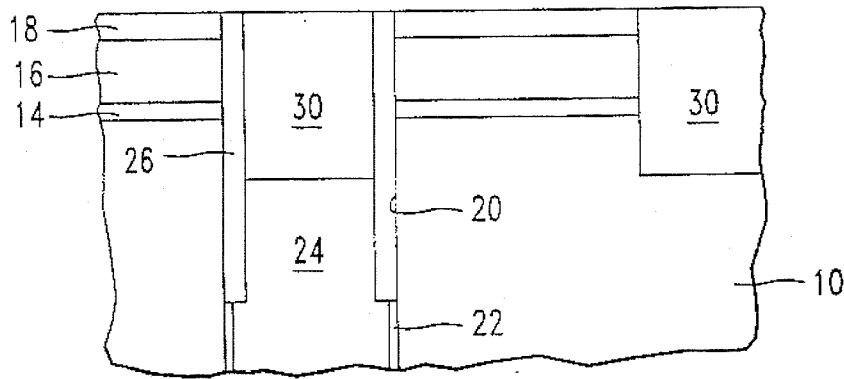


FIG. 4

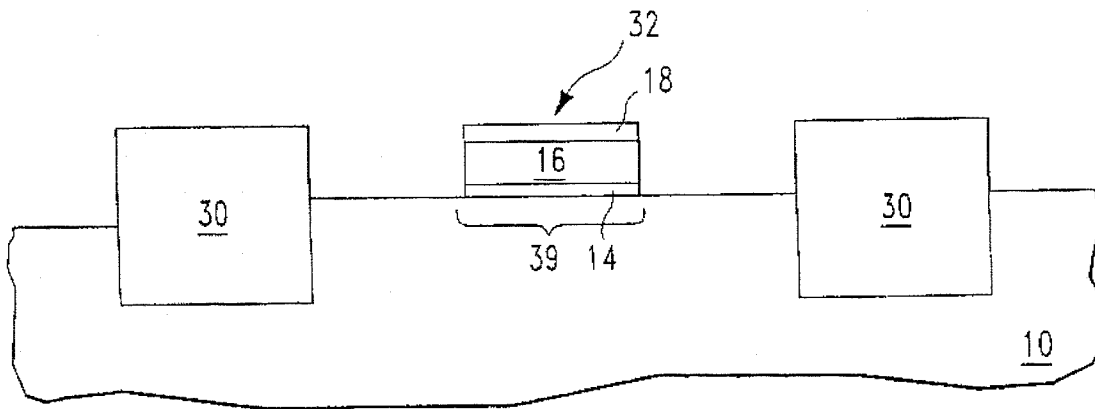


FIG. 5

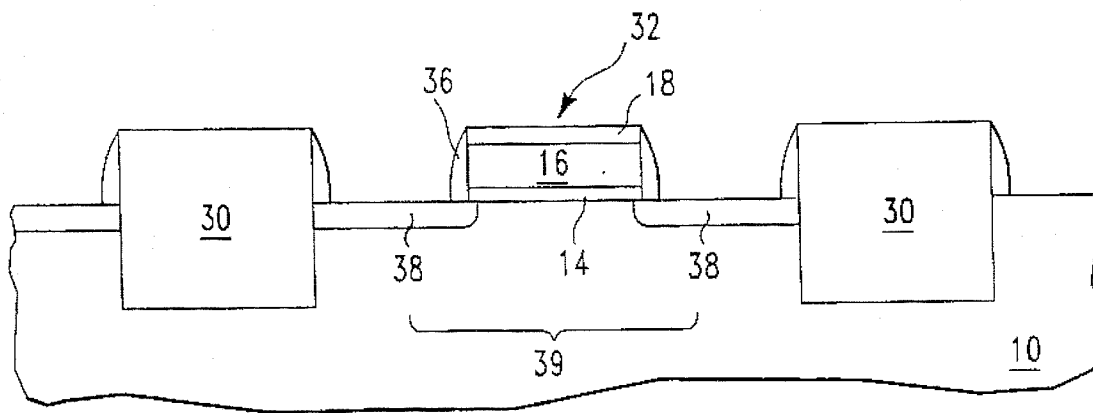


FIG. 6

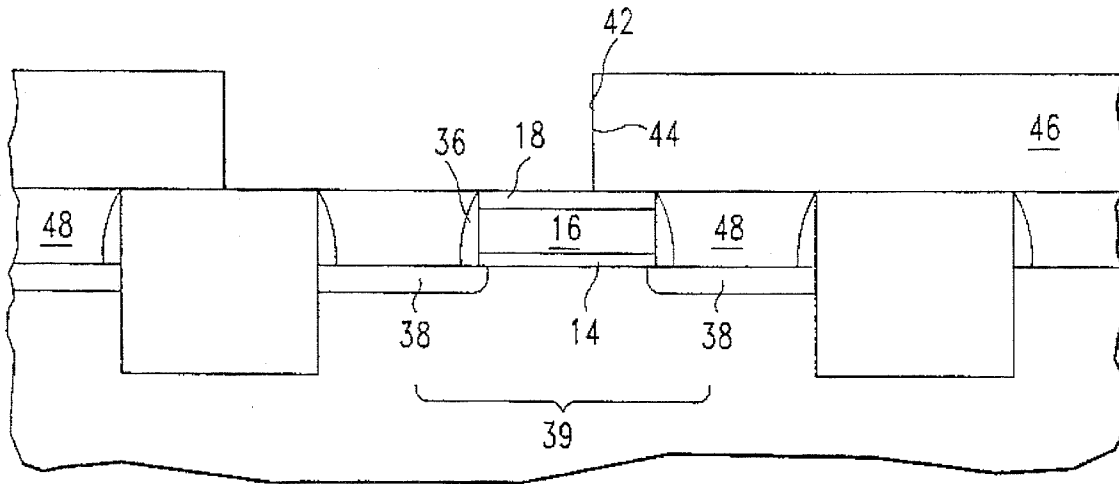


FIG. 7

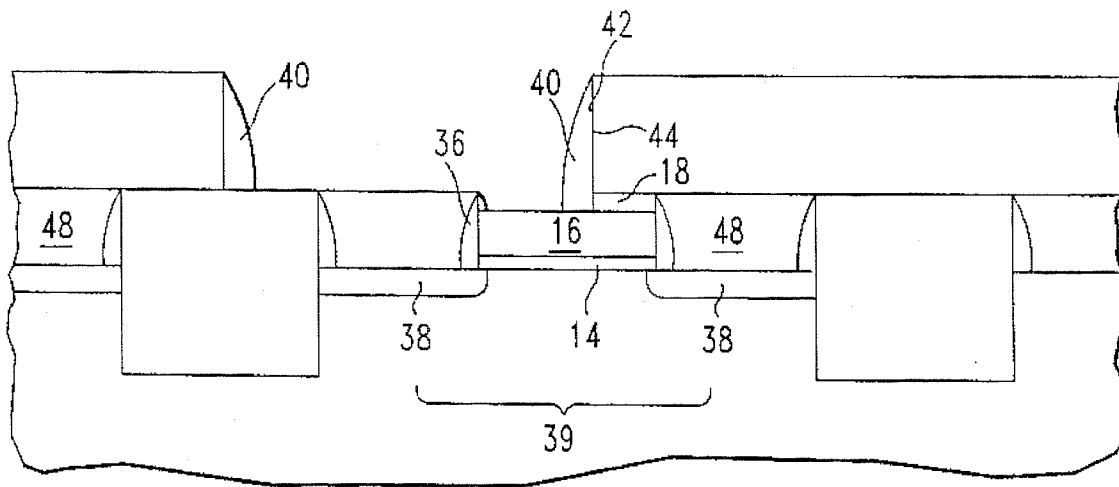


FIG. 8

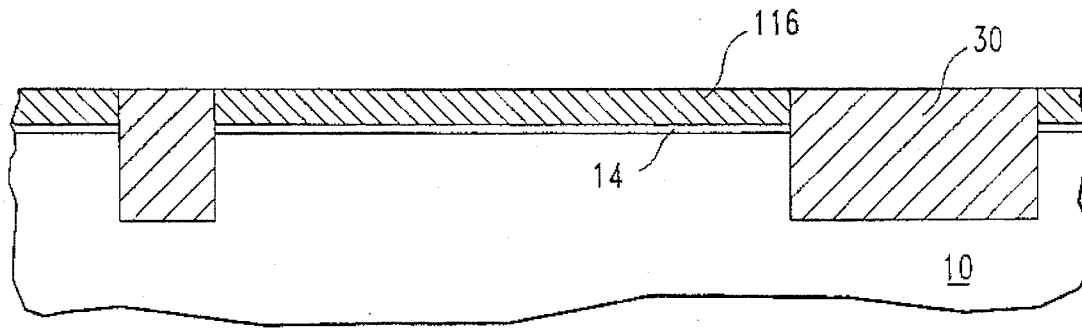


FIG. 9

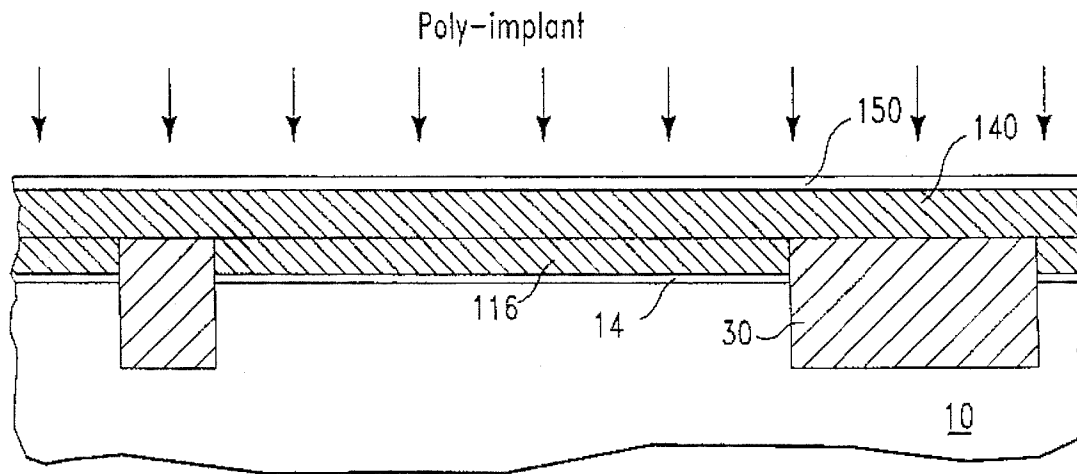


FIG. 10

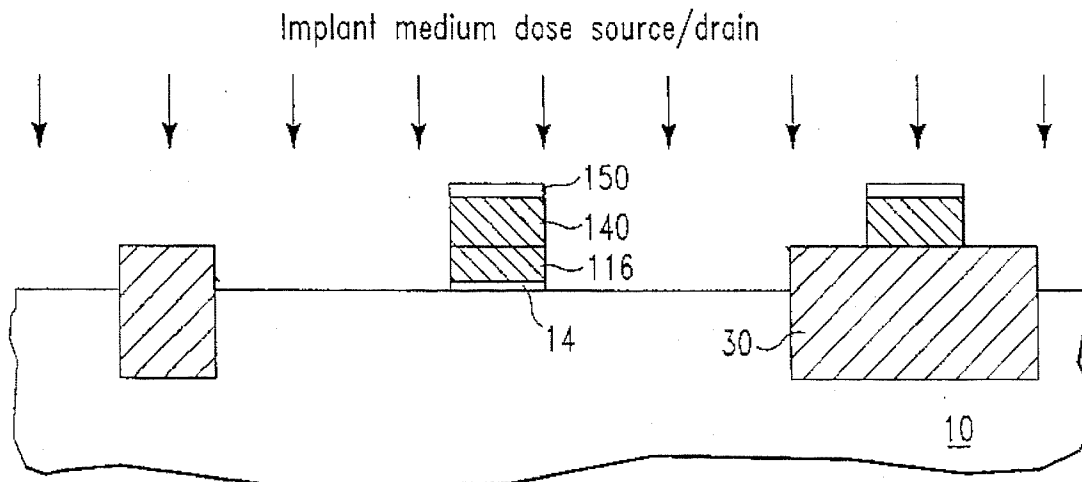


FIG. 11

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