United States Patent [19]

Ogawa et al.

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[54] **METHOD FOR PRODUCTION OF SEMICONDUCTOR DEVICES**

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[73] Assignee: **Fujitsu Limited**, Kawasaki, Japan

[21] Appl. No.: **414,803**

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[30] **Foreign Application Priority Data**

Sep. 10, 1981 [JP] Japan 56-142911

[51] Int. Cl.³ H01L 21/76; H01L 21/302; H01L 21/20

[52] U.S. Cl. .... **29/571**; 29/578; 29/576 W; 148/1.5; 148/175; 148/187; 156/643; 156/648; 156/662; 357/49

[58] Field of Search .... 29/571, 576 R, 576 B, 29/576 W, 578; 148/174, 175, 187, 1.5; 357/47, 48, 49, 50; 156/643, 648, 653, 661.1, 662

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[57] **ABSTRACT**

A method for producing semiconductor devices having a substrate, element fabrication areas formed in the substrate and isolation areas surrounding the element fabrication areas. The method comprises forming a thermal strain absorbing layer on the top surface of the element fabrication areas, forming at least one groove in an area which is to become the isolation areas, inlaying an insulator in the at least one groove, and annealing the insulator to make the density thereof uniform.
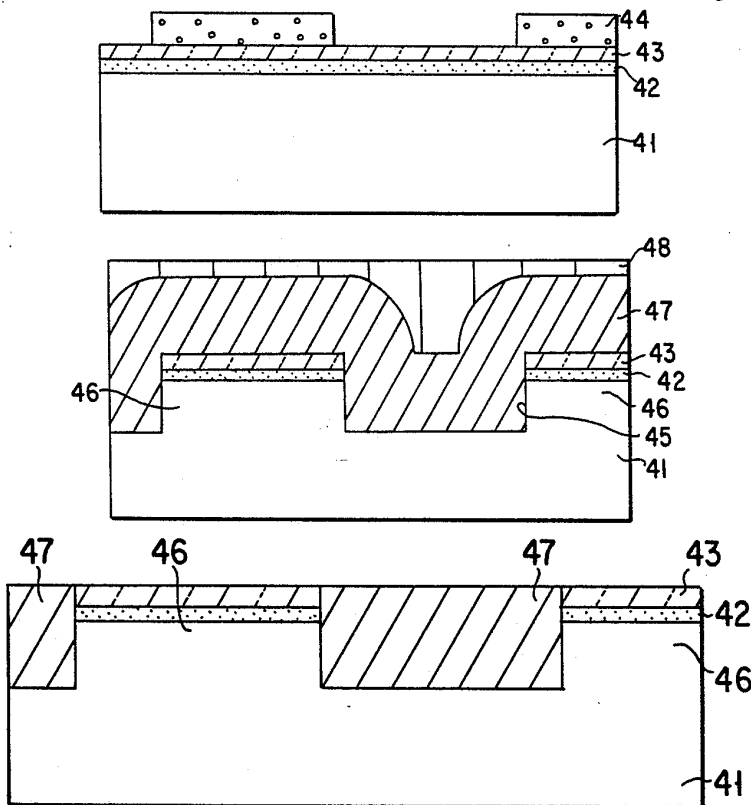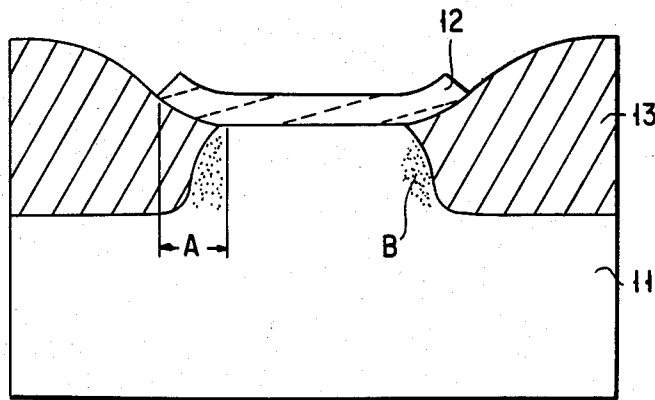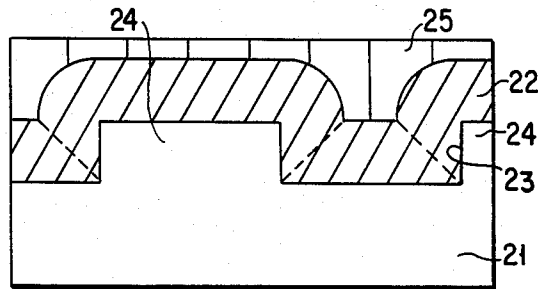
9 Claims, 21 Drawing Figures
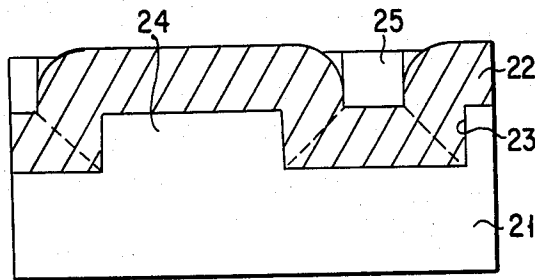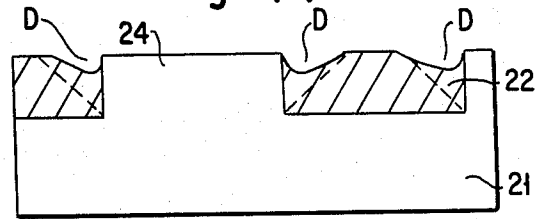
Fig. 1

Fig.2(a)
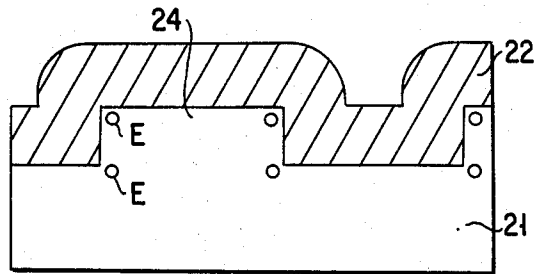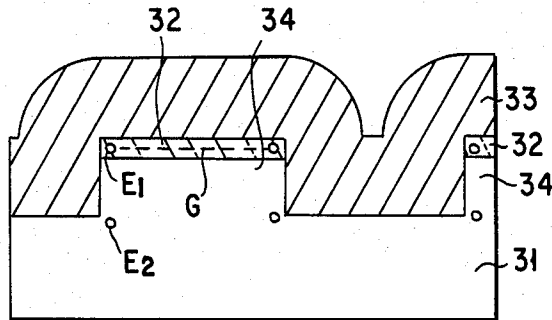

Fig.2(b)
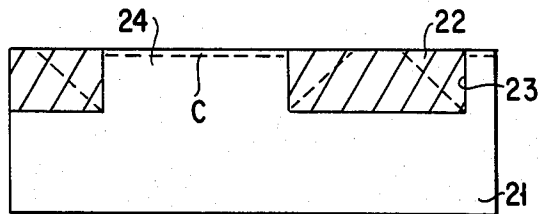
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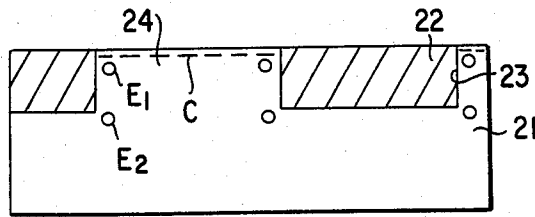
Fig.2(d)

Fig.2(e)

Fig.2(f)

Fig.3

Fig.4(a)
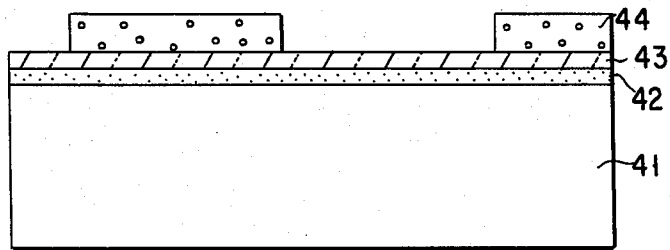
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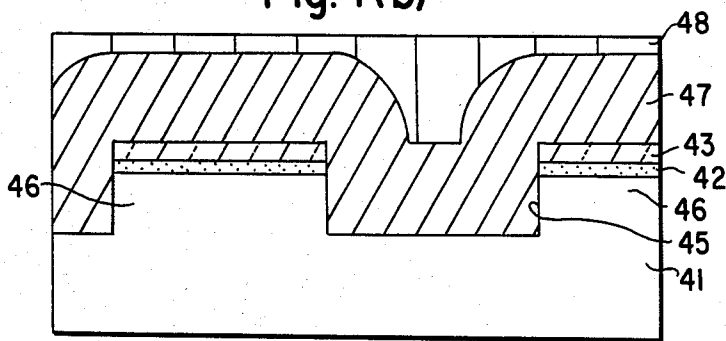
Fig. 4(c)

Fig.(d)

Fig.(e)

DOCKET ALARM
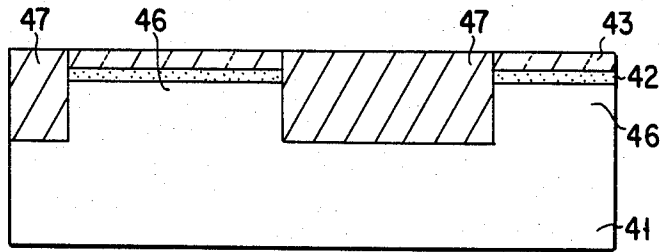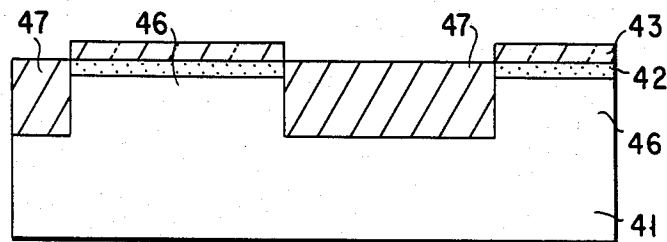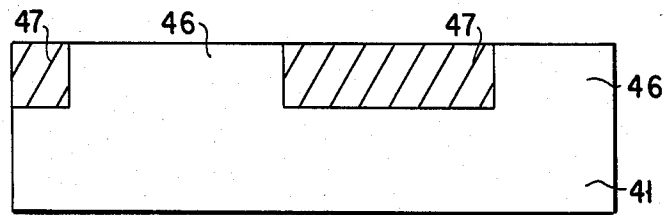
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