



US005733812A

United States Patent [19]

Ueda et al.

[11] Patent Number: **5,733,812**

[45] Date of Patent: **Mar. 31, 1998**

[54] **SEMICONDUCTOR DEVICE WITH A FIELD-EFFECT TRANSISTOR HAVING A LOWER RESISTANCE IMPURITY DIFFUSION LAYER, AND METHOD OF MANUFACTURING THE SAME**

[75] Inventors: **Tetsuya Ueda; Takashi Uehara; Kousaku Yano; Satoshi Ueda**, all of Osaka, Japan

[73] Assignee: **Matsushita Electric Industrial Co., Ltd.**, Osaka, Japan

[21] Appl. No.: **571,131**

[22] Filed: **Dec. 12, 1995**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 340,341, Nov. 14, 1994, abandoned.

[30] Foreign Application Priority Data

Nov. 15, 1993 [JP] Japan 5-284820
Oct. 26, 1995 [JP] Japan 7-278546

[51] Int. Cl.⁶ **H01L 21/265**

[52] U.S. Cl. **438/289; 438/297; 438/301; 438/586; 438/691**

[58] Field of Search 437/40 R, 40 GS, 437/40 RG, 41 R, 41 GS, 44, 45, 187, 979, 228 POL. 29, 228 PL; 156/636.1, 645.1; 216/52; 148/DIG. 163; 438/289, 297, 301, 586, 691

[56] References Cited

U.S. PATENT DOCUMENTS

4,287,660 9/1981 Nicholas 437/41 GS
4,330,931 5/1982 Liu 29/571
4,584,761 4/1986 Wu 437/41 R

4,713,356	12/1987	Hiruta	437/41
4,727,043	2/1988	Matsumoto et al.	437/29
4,780,429	10/1988	Roche et al.	437/41
5,209,816	5/1993	Yu et al.	156/636
5,245,210	9/1993	Nishigoori	257/382
5,289,443	2/1994	Jang	437/40 GS
5,340,370	8/1994	Cadien et al.	51/308
5,346,584	9/1994	Nasr et al.	156/636
5,422,289	6/1995	Pierce et al.	437/32
5,447,874	9/1995	Grivna et al.	437/40 GS

FOREIGN PATENT DOCUMENTS

5-13432 1/1993 Japan .

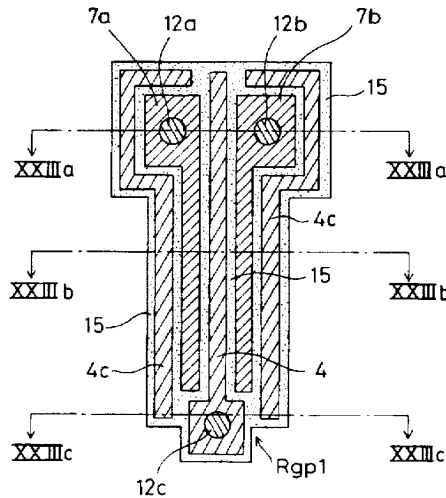
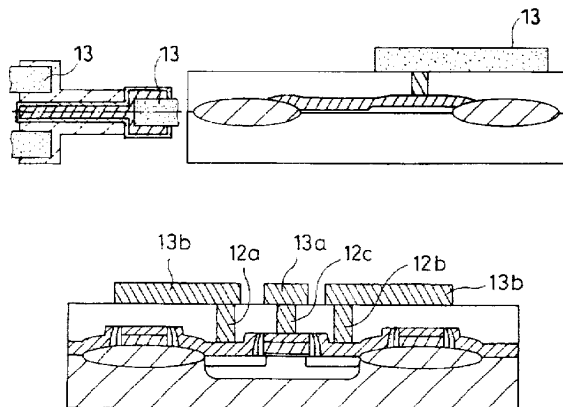
Primary Examiner—Brian Dutton

Attorney, Agent, or Firm—McDermott, Will & Emery

[57] ABSTRACT

There is formed an isolation which surrounds an active region of a semiconductor substrate. Formed over the active region and on the isolation, respectively, are a gate electrode and two gate interconnections on both sides thereof. Between the gate electrode and the gate interconnections are located two first interspaces each of which is smaller in width than a specified value and a second interspace which is larger in width than the specified value and interposed between the two first interspaces. In forming side walls on both side faces of the gate electrode and gate interconnections by depositing an insulating film on the substrate, the first interspaces are buried with the insulating film. Thereafter, a metal film is deposited on the substrate, followed by chemical mechanical polishing till the gate electrode, gate interconnections, and side walls become exposed. By the process, withdrawn electrodes from a source/drain region for contact with the active region is formed by self alignment, while the withdrawn electrodes are insulated from the gate electrode and gate interconnections by the side walls.

11 Claims, 27 Drawing Sheets



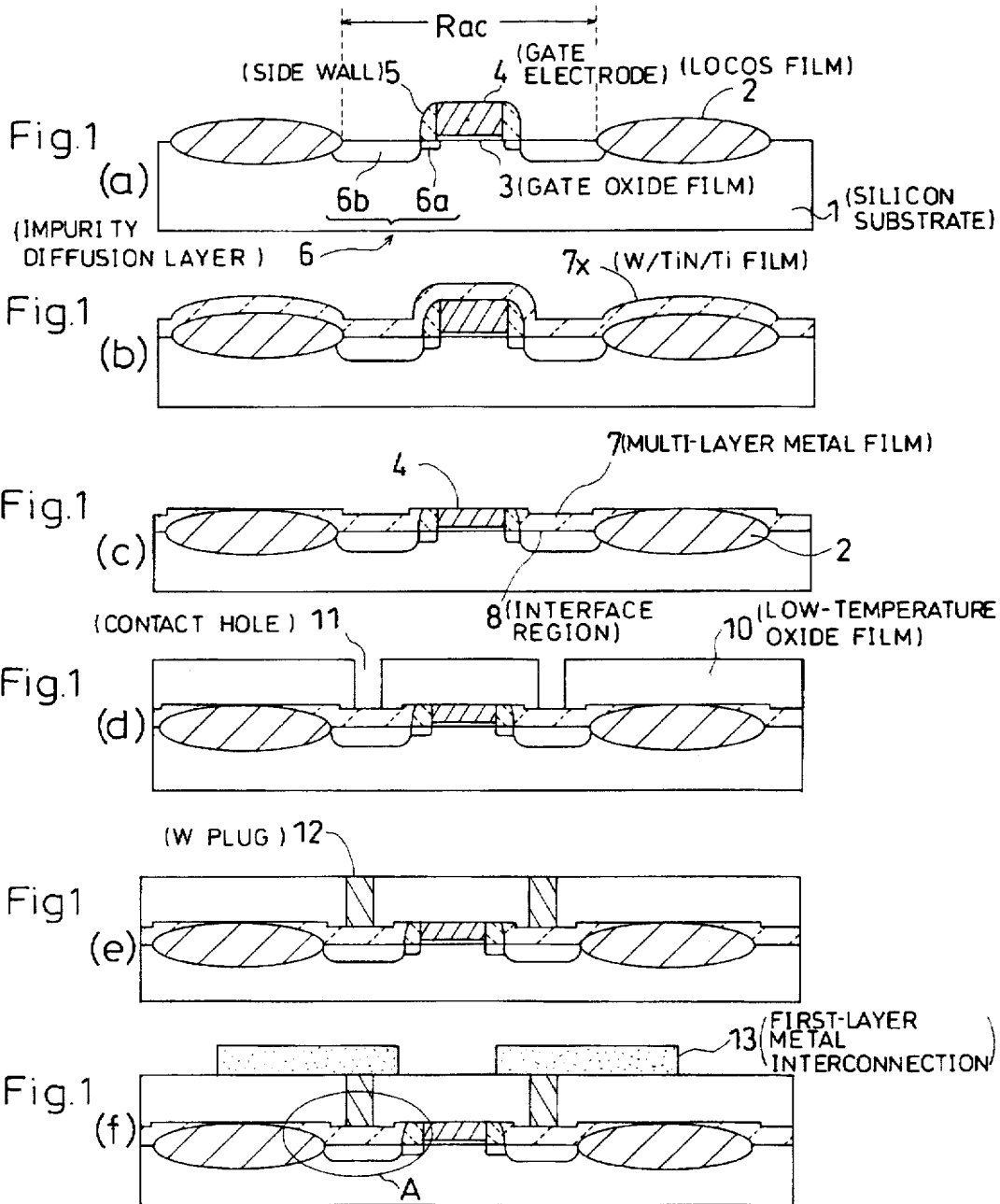


Fig.2

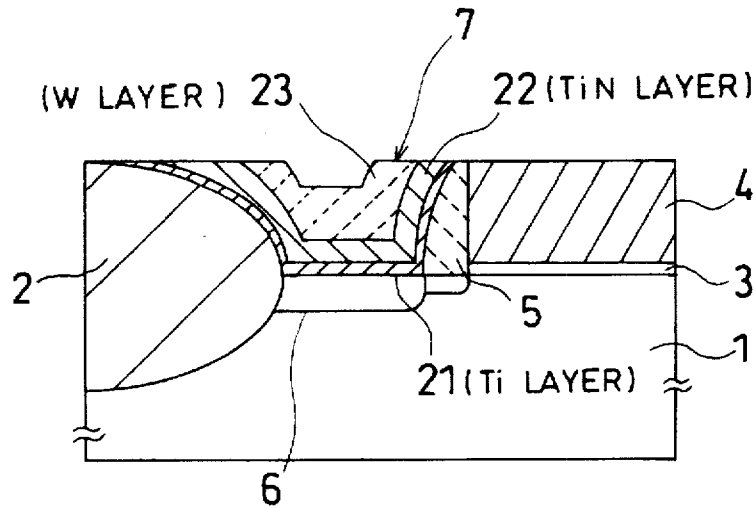


Fig.3

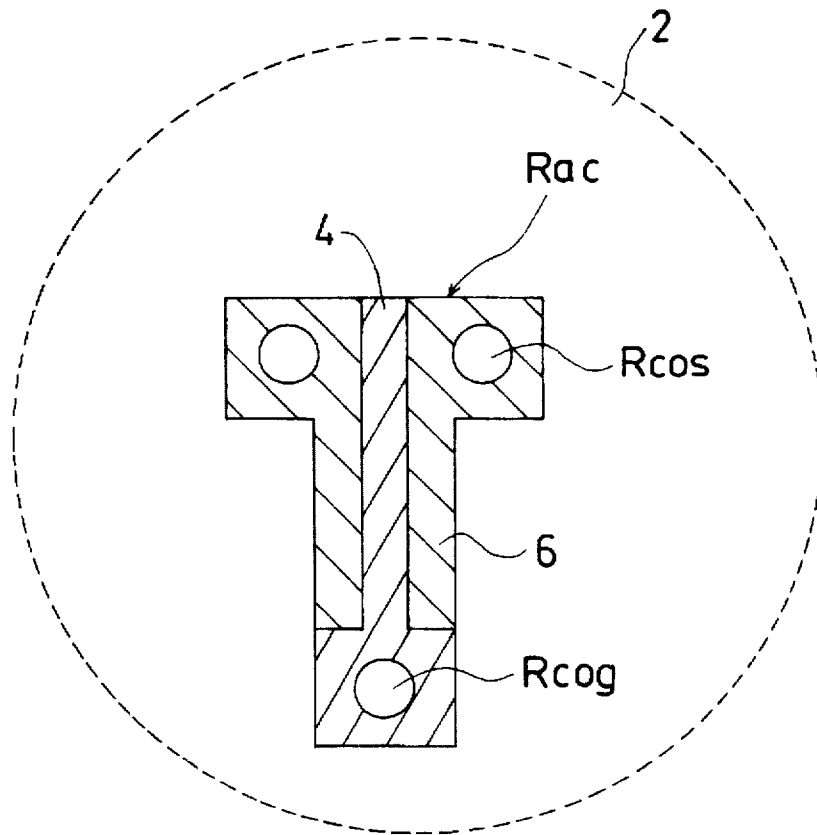


Fig.4

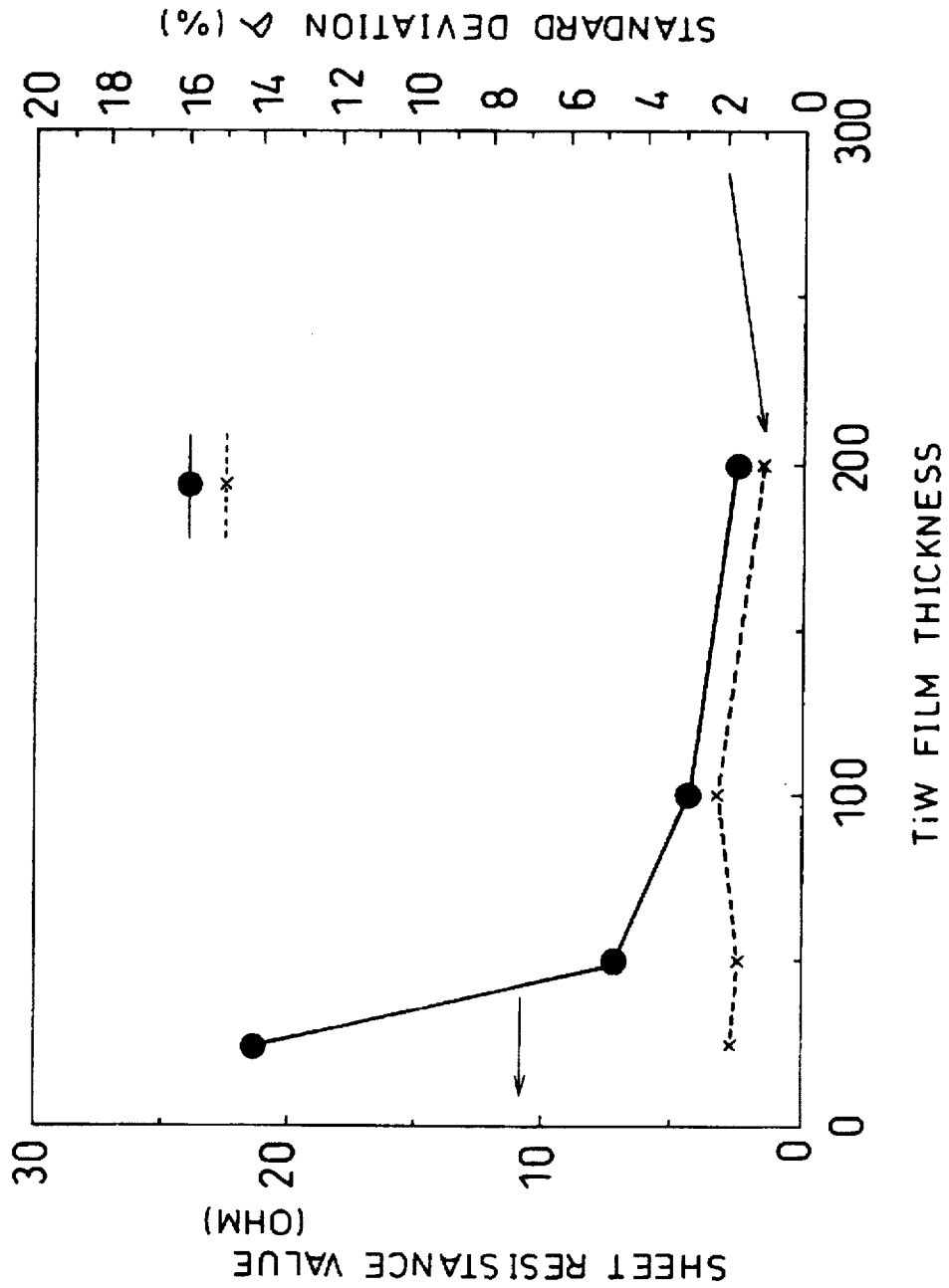
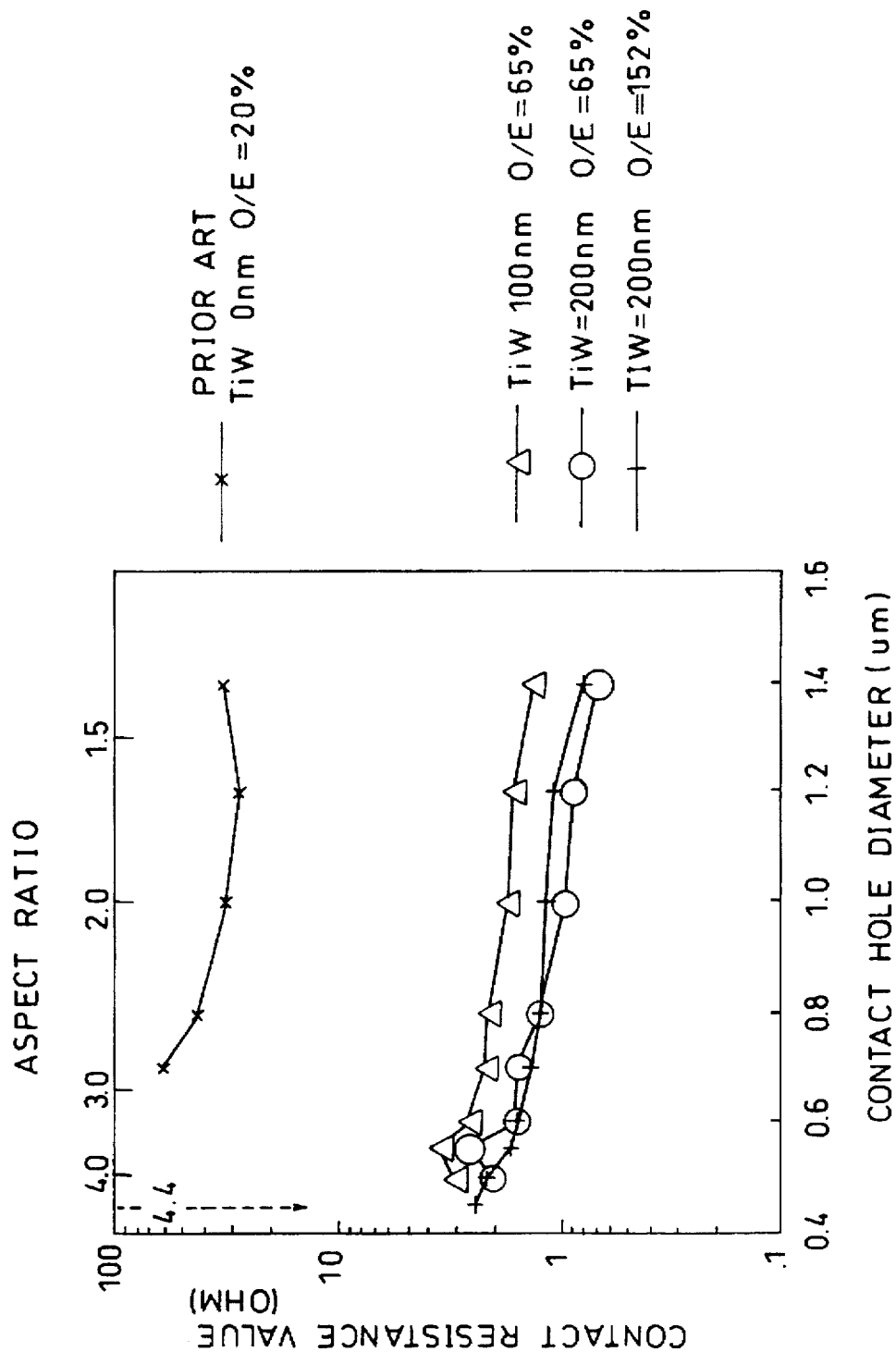


Fig.5



Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.