

## CERTIFICATE OF TRANSLATION

I Roger P. Lewis, whose address is 42 Bird Street North, Martinsburg WV 25401, declare and state the following:

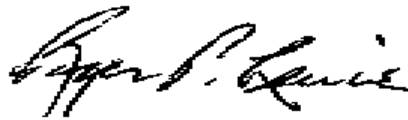
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I hereby certify that the Japanese translation of the attached document identified as:

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SINCERELY,



ROGER P. LEWIS

Date: June 30, 2016

【Document Name】 Patent Application  
【Docket Number】 2926400241  
【Submission Date】 11<sup>th</sup> Year of Heisei, 3<sup>rd</sup> Month, 19<sup>th</sup> Day  
[March 19, 1999]  
【Submitted To】 Director General of the Patent Office  
【International Classification】 H01L 21/3205  
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【Assertion of Priority Rights Based on Earlier Application】  
    【Application Number】 10<sup>th</sup> Year of Heisei Pat. App. Number 79371  
    【Application Date】 10<sup>th</sup> Year of Heisei, 3<sup>rd</sup> Month, 26<sup>th</sup> Day  
    [March 26, 1998]  
【Indication of Fee】  
    【Deposit Account Number】 014409  
    【Monetary Amount Paid】 ¥21,000  
Index of Submitted Items】  
    【Name of Item】 Specifications 1  
    【Name of Item】 Figures 1

[Document Name] Patent Application [Receipt Date] Hei.11. 3. 9 [March 9, 1999]  
[Patent] Hei. 11 [1999] – 075519 (11. 3. 19) Page:2/2

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【Name of Item】 Abstract 1

【General Power of Attorney Number】  
9601026

【Proofing – Required/Not Required】  
Required

【Document Name】 Specifications  
【Name of Invention】 Formation Method of Wiring Structure  
【Scope of the Patent Claims】

【Claim 1】 A formation method of wiring structure that is characterized by the following:

Process 1, by which a 1<sup>st</sup> insulating film is formed over the lower layer of metal wiring, and Process 2, by which a 2<sup>nd</sup> insulating film that differs in composition from the afore described 1<sup>st</sup> insulating film is formed over this 1<sup>st</sup> insulating film, and

Process 3, by which a 3<sup>rd</sup> insulating film that differs in composition from the afore described 2<sup>nd</sup> insulating film is formed over this 2<sup>nd</sup> insulating film, and

Process 4, by which a thin film is formed over the afore described 3<sup>rd</sup> insulating film, and

Process 5, by which a 1<sup>st</sup> resist pattern that has opening(s) for forming wiring is formed over the afore described thin film, and

Process 6, by which etching is performed vis-à-vis the afore described thin film whilst using the afore described 1<sup>st</sup> register pattern as a mask, thus forming from the afore described thin film a mask pattern that has opening(s) for forming wiring, and

Process 7, by which a 2<sup>nd</sup> resist pattern that has opening(s) for contact hole formation is formed over the afore described 3<sup>rd</sup> insulating film, and

Process 8, by which dry etching is performed vis-à-vis the afore described 3<sup>rd</sup> insulating film so that the etching conditions for the etching rate for the afore described 3<sup>rd</sup> insulating film vis-à-vis the 1<sup>st</sup> resist pattern and the 2<sup>nd</sup> resist pattern is high whilst the etching rate vis-à-vis the afore described 2<sup>nd</sup> insulating film is low, so that together with pattern formation on the afore described 3<sup>rd</sup> insulating film of opening(s) for contact hole formation on this 3<sup>rd</sup> insulating film, and the total or partial removal of the afore described 1<sup>st</sup> resist pattern and the 2<sup>nd</sup> resist pattern, and

Process 9, by which the etching conditions are such that the etching rate vis-à-vis the afore described 2<sup>nd</sup> insulating film is high, the etching rate vis-à-vis the 3<sup>rd</sup> insulating film is low, the patterning is in such a way as to form on the afore described 2<sup>nd</sup> insulating film contact hole formation opening(s) on this 2<sup>nd</sup> insulating film, with, as a mask, the afore described 3<sup>rd</sup> insulating film that has been patterned vis-à-vis the afore described 2<sup>nd</sup> insulating, and

Process 11, by which, under etching [...]

[...] conditions such that the etching rate vis-à-vis the afore described 1<sup>st</sup> insulating film and 3<sup>rd</sup> insulating film is high whilst the etching rate vis-à-vis the afore described mask pattern and 2<sup>nd</sup> insulating pattern is low, are conducted dry etching vis-à-vis the afore described 3<sup>rd</sup> insulating film as the afore described mask pattern and also conducting dry etching vis-à-vis the afore described 1<sup>st</sup> insulating pattern as the patterned afore described 2<sup>nd</sup> insulating film, resulting in the formation of the wiring groove(s) in the afore described 3<sup>rd</sup> insulating film together with the contact hole(s) in the afore described 1<sup>st</sup> insulating film, and

Process 11, by which the filling of the afore described wiring groove(s) and contact hole(s) with a metal film so as to form the contact that connects the upper level metal wiring & the afore described lower level metal wiring and the afore described lower level metal wiring & the afore described upper level metal wiring.

【Claim 2】 The formation method of wiring structure of Claim 1 that is characterized by the fact that it is further equipped with a process between the afore described Process 10 and Process 11 of the formation of an adhesive layer consisting of a metal film that is formed in the exposed portion(s) of the afore described wiring groove(s) in the afore describe 3<sup>rd</sup> insulating film and the exposed portion(s) of the afore described contact hole(s) of the afore described 1<sup>st</sup> insulating film.

【Claim 3】 The formation method of wiring structure described in Claim 1 that is characterized by the fact that the afore described 3<sup>rd</sup> insulating film is mainly composed of organic component(s).

【Claim 4】 The formation method of wiring structure described in Claim 3 that is characterized by the fact it includes the formation of the afore described 3<sup>rd</sup> insulating film by means of the CVD method wherein a perfluorodecalin containing reactive gas is used.

【Claim 5】 The formation method of wiring structure described in Claim 3 that is characterized by the fact that the afore described 1<sup>st</sup> insulating film is mainly composed of organic component(s).

【Claim 6】 The formation method of wiring structure of Claim 5 that is characterized by the fact that it is further equipped with a process between the afore described Process 10 and Process 11 of the formation of an adhesive layer by the plasma processing wherein nitrogen-containing reactive gas(es) is/are used on the exposed portion(s) of the afore described wiring groove(s) in the afore describe 3<sup>rd</sup> insulating film and the exposed portion(s) of the afore described contact hole(s) of the afore described 1<sup>st</sup> insulating film.

【Claim 7】 The formation method of wiring structure described in Claim 3 that is characterized by the fact it includes the formation of the afore described 1<sup>st</sup> insulating film by means of the CVD method wherein a perfluorodecalin containing reactive gas is used.

【Claim 8】 A formation method of wiring structure that is characterized by the following:  
Process 1, by which a 1st insulating film is formed over the lower layer of metal wiring, and [...]

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