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United States Patent [19]

Yu et al.

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[45] Date of Patent: **Aug. 15, 2000**

[54] **METHOD TO MANUFACTURE DUAL DAMASCENE STRUCTURES BY UTILIZING SHORT RESIST SPACERS**

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[57] ABSTRACT

[21] Appl. No.: **09/136,867**

A method of manufacturing semiconductor devices wherein a partially completed semiconductor device having a first and second layer of interlayer dielectric and a first and second etch stop layer has the second etch stop layer masked and etched with an etch pattern having dimensions of the trench structure to be formed in the second interlayer dielectric. The second layer dielectric and first etch stop layer are then masked and etched with an etch pattern having dimensions of the via structure to be formed in the first interlayer dielectric. The remaining portions of the photo-resist is removed and exposed portions of the second layer of interlayer dielectric and the first layer of interlayer dielectric are then etched simultaneously. The via structure and trench structure are then simultaneously filled with a conductive material.

[22] Filed: **Aug. 19, 1998**

[51] Int. Cl.⁷ **H01L 21/4763**

[52] U.S. Cl. **438/622**; 438/618; 438/634; 438/638

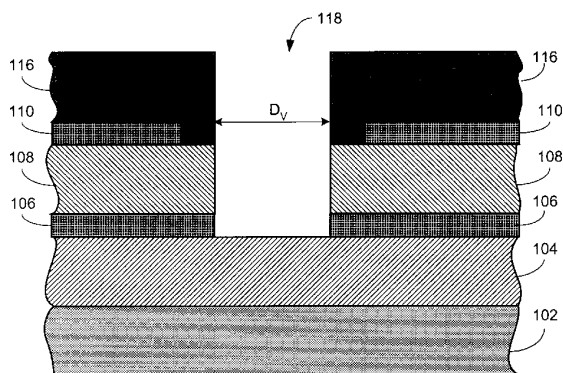
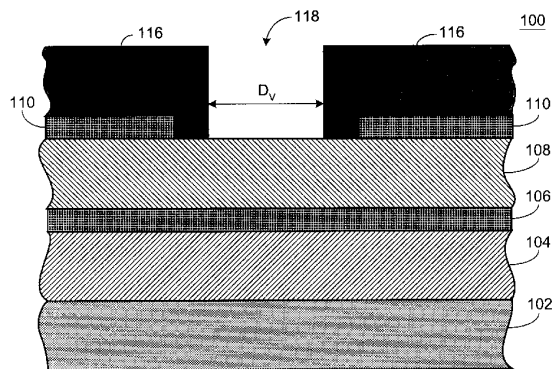
[58] Field of Search 438/618, 622, 438/634, 637, 671, 672, 675, 638

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6 Claims, 6 Drawing Sheets



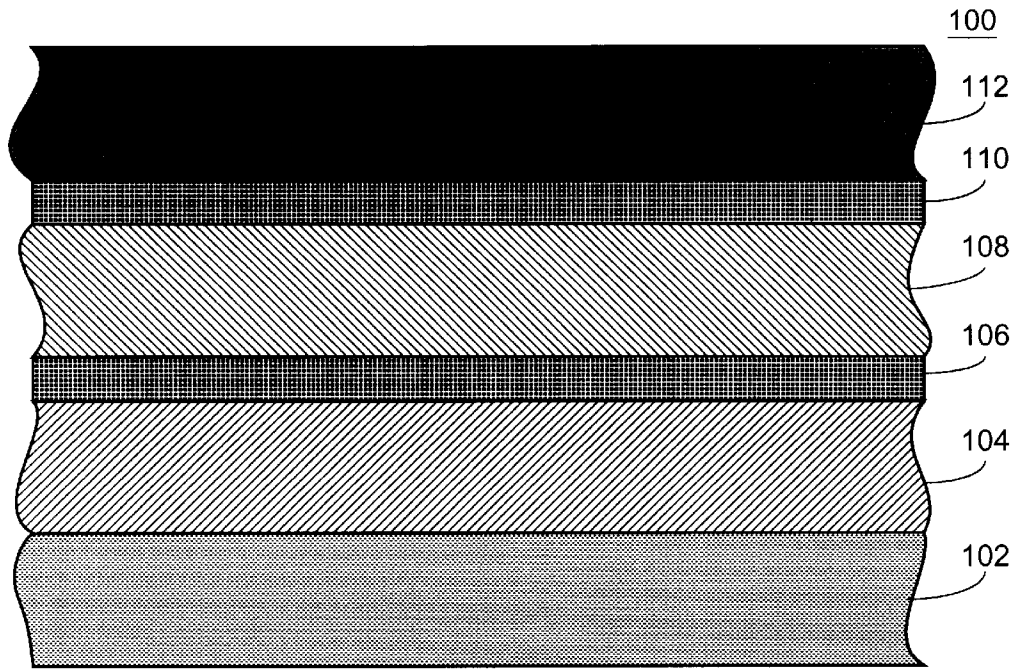


FIGURE 1A

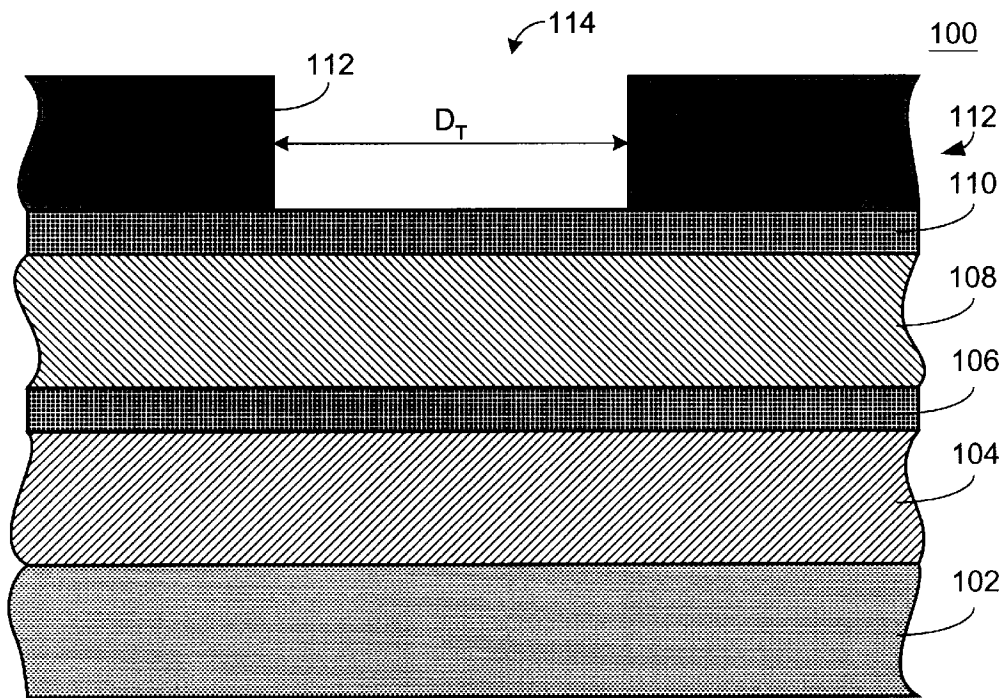


FIGURE 1B

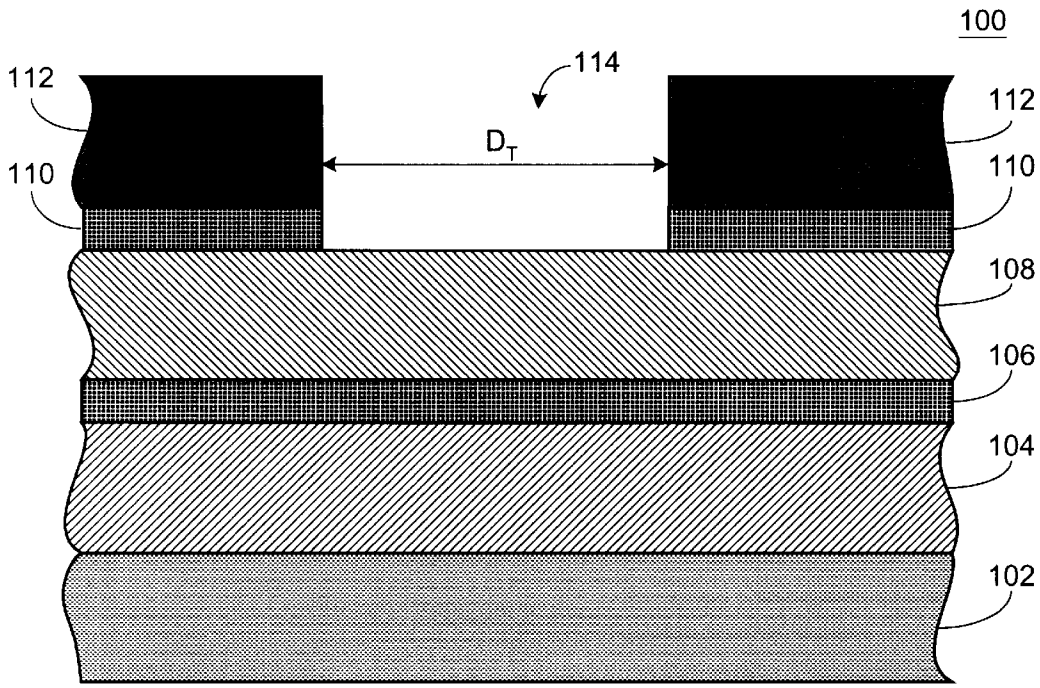


FIGURE 1C

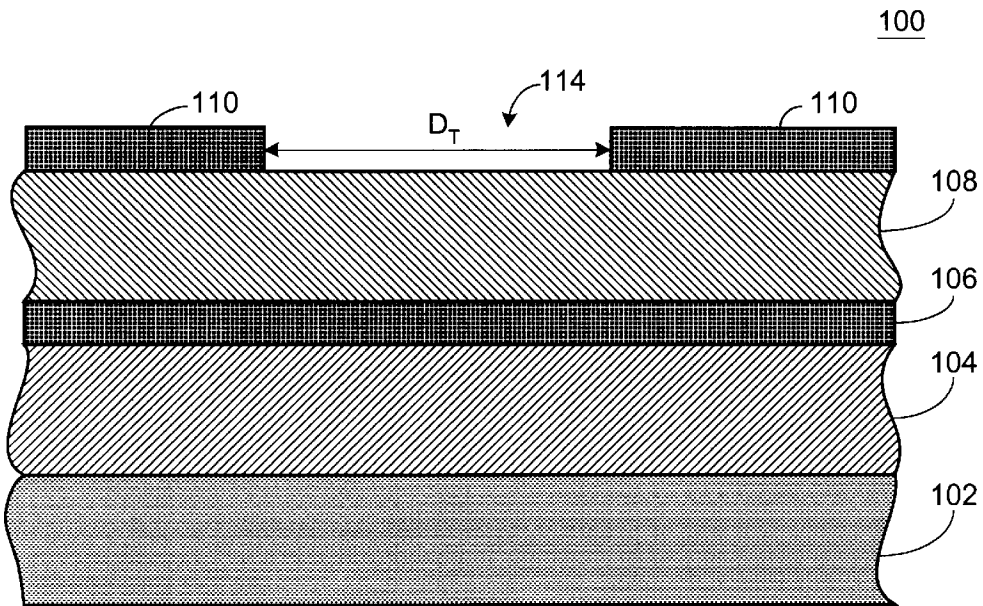


FIGURE 1D

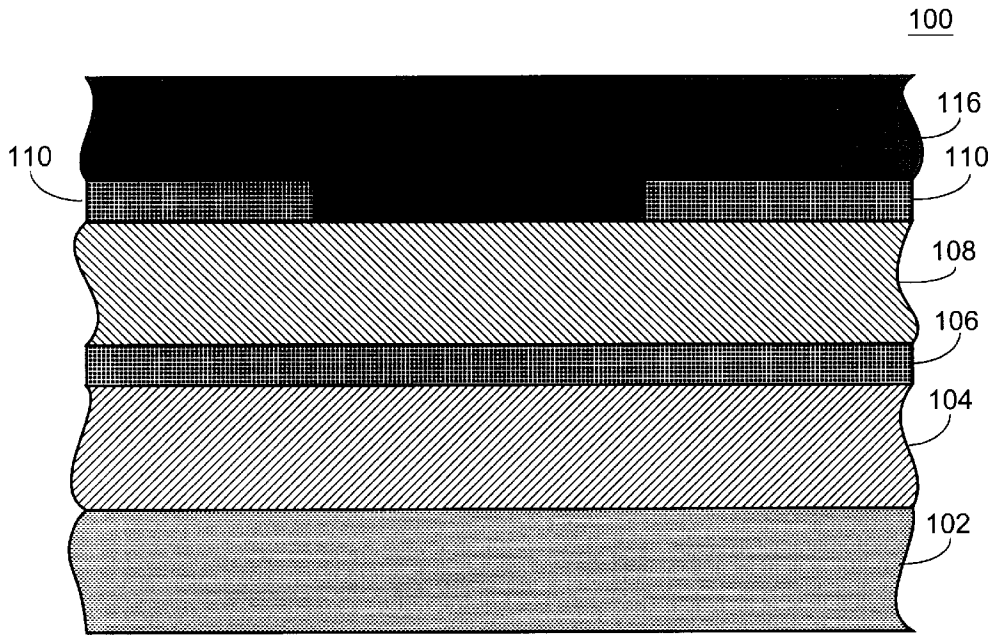


FIGURE 1E

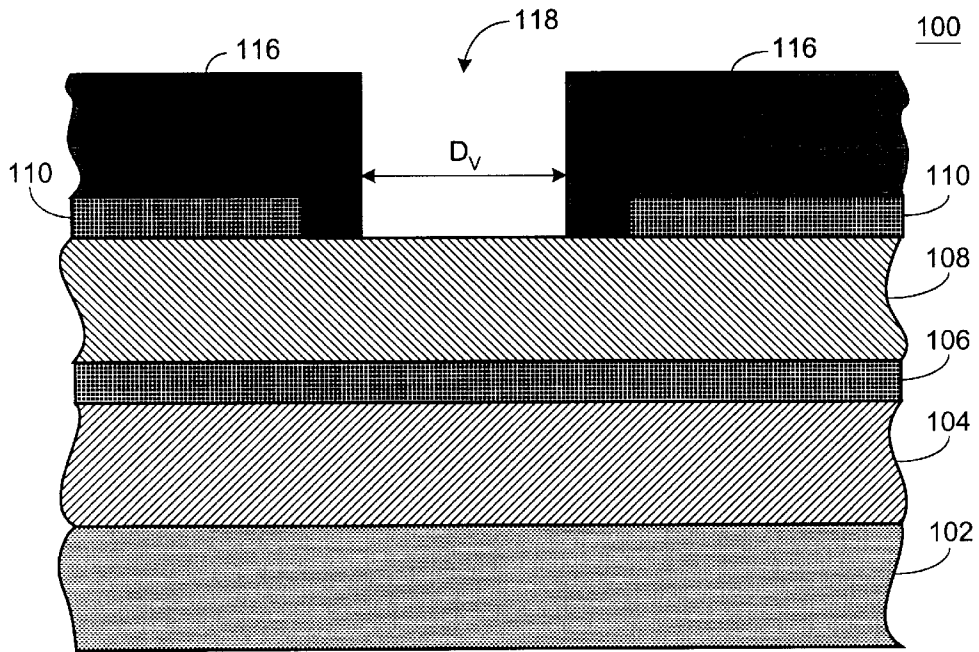


FIGURE 1F

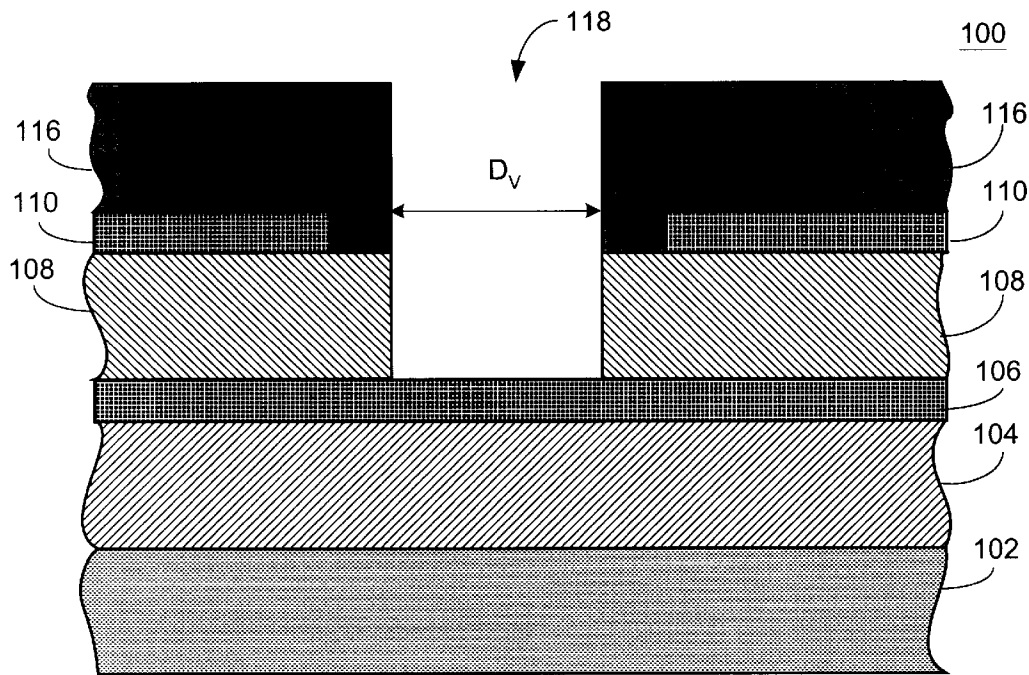


FIGURE 1G

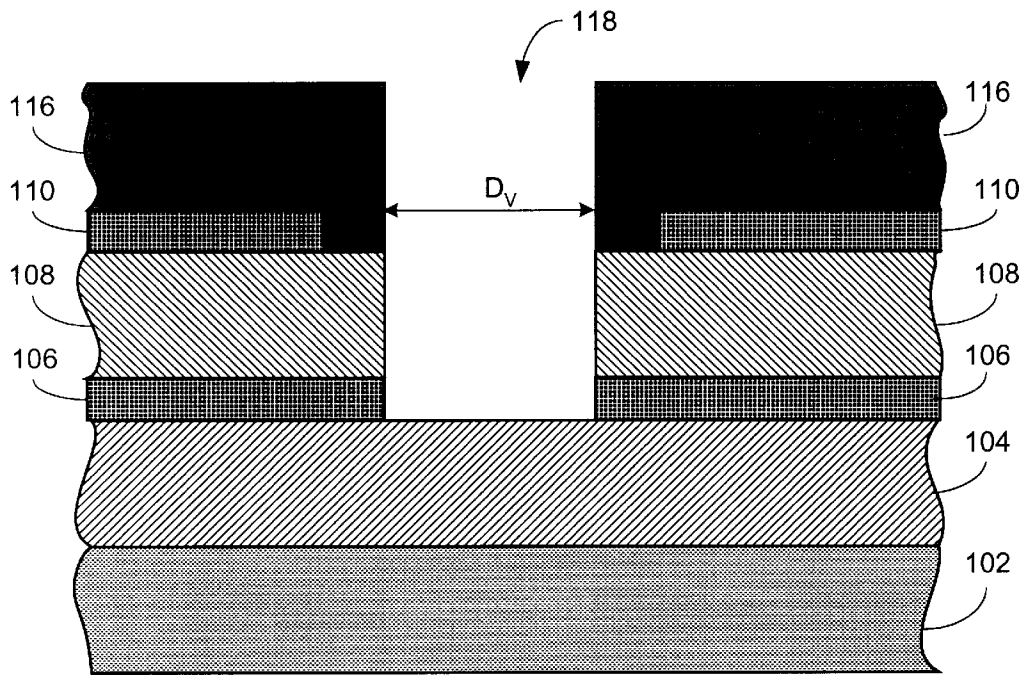


FIGURE 1H

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