CERTIFICATION OF TRANSLATION

The undersigned, Richard Patner, whose address is 26357 Lexington Drive, Bonita Springs, FL 34135, United States of America, declares and states as follows:

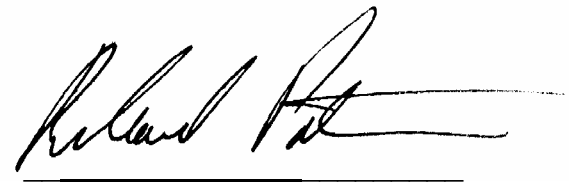
I am well acquainted with the English and Japanese languages; I have in the past translated numerous Japanese documents of legal and/or technical content into English.

I have been requested to translate into English the attached Japanese Patent No. 10-079371 titled "**Method of forming wiring structure .**"

To a copy of this Japanese document I therefore attach an English translation and my Certification of Translation.

I hereby certify that the attached English translation of Japanese Patent No. 10-079371 titled "**Method of forming wiring structure**" is, to the best of my knowledge and ability, an accurate translation.

And I declare further that all statements made herein of my own knowledge are true, that all statements made on information and belief are believed to be true, and that false statements and the like are punishable by fine and imprisonment, or both, under Section 1001 of Title 18 of the United States Code.



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Osaka-fu, Kadoma-shi, Oaza Kadoma 1006
Representative Type (1) Code (1000077931) Maeda Hiroshi
Type (1) Code ( ) Koyama Hiroki
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[Inventor]
[Address or Location] Osaka-fu, Kadoma-shi, Oaza Kadoma 1006
Matsushita Electric Industrial Co., Ltd.
[Name] AOI Nobuo
[Patent Applicant]
[Identification Number] 000005821
[Name] Matsushita Electric Industrial Co., Ltd.
[Agent]
[Identification Number] 1000077931
[Patent Attorney]
[Name or Appellation] Maeda Hiroshi
[Designated Agent]
[Identification Number] 100094134
[Patent Attorney]
[Name or Appellation] Koyama Hiroki
[Designated Agent]
[Identification Number] 100107445
[Patent Attorney]
[Name or Appellation] Koneda Ichiro
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[Name of Document] Specification
[Title of Invention] Method of forming wiring structure
[Scope of Patent Claims]
[Claim 1] A method of forming a wiring structure comprising 11 steps:
a first step of forming a first insulating film over lower-level metal wiring,
a second step of forming a second insulating film having a different structure from that of said first insulating film over the aforementioned first insulating film,
a third step of forming a third insulating film having a different structure from that of said second insulating film over the aforementioned second insulating film,
a fourth step of forming a conducting film over the aforementioned third insulating film,
a fifth step of forming a first resist pattern having an opening for the formation of wiring over the aforementioned conducting film,
a sixth step of forming a mask pattern from the aforementioned conducting film with an opening for the formation of wiring by etching the aforementioned conducting film using the aforementioned first resist pattern as a mask,
a seventh step of forming a second resist pattern with an opening for the formation of contact holes over the aforementioned third insulating film,
an eighth step of patterning the aforementioned third insulating film so as to form an opening for the formation of contact holes in said third insulating film by dry etching the aforementioned third insulating film using the first resist pattern or the second resist pattern under etching conditions such that the pattern with the higher etching rate is used while the pattern with the lower etching rate is used in etching of the aforementioned second insulating film, and by removing the entire first resist pattern and second resist pattern or leaving the lower portion,
a ninth step of patterning the aforementioned second insulating film so as to form an opening for the formation of contact holes in said second insulating film by dry etching, using the aforementioned third insulating film that had been patterned as a mask, of the aforementioned second insulating film under etching conditions such that the etching rate of the aforementioned second insulating film is higher while the etching rate of the aforementioned first insulating film and the third insulating film is lower,
a tenth step of forming wiring grooves in the aforementioned third insulating film and of forming contact holes in the aforementioned first insulating film by dry etching using the aforementioned mask pattern for the aforementioned third insulating film as a mask and by dry etching using the aforementioned second insulating film that had been patterned for the aforementioned first insulating film as a mask under etching conditions such that the etching rate of the aforementioned first insulating film and the third insulating film is higher while the etching rate of the mask pattern and of the second insulating film is lower,
and an eleventh step of forming contacts that connect the upper-level metal wiring and the aforementioned lower-level metal wiring with the aforementioned upper-level metal wiring by packing metal film in the aforementioned wiring grooves and contact holes.
[Claim 2] The method of forming a wiring structure of Claim 1 in which a step of forming adhesion layers comprising metal film in the section of the aforementioned third insulating film exposed in the aforementioned wiring grooves and in the section of the aforementioned first insulating film exposed in the aforementioned contact holes is inserted between the aforementioned tenth step and the aforementioned eleventh step.
[Claim 3] The method of forming a wiring structure of Claim 1 in which the principal constituents of the aforementioned third insulating film are organic constituents.
[Claim 4] The method of forming a wiring structure of Claim 3 in which the aforementioned third step also includes the step of forming the aforementioned third insulating film by the CVD method using reactive gas that contains perfluorodecalin.
[Claim 5] The method of forming a wiring structure of Claim 3 in which the principal constituents of the aforementioned first insulating film are organic constituents.
[Claim 6] The method of forming a wiring structure of Claim 5 in which a step of forming an adhesion layer by plasma treatment using reactive gas containing nitrogen in the section of the aforementioned third insulating film exposed in the aforementioned wiring grooves and in the section of the aforementioned first insulating film exposed in the aforementioned contact holes is further included between the aforementioned tenth step and the aforementioned eleventh

step.
[Claim 7] The method of forming a wiring structure of Claim 3 in which the aforementioned first step includes a step of forming the aforementioned third insulating film by the CVD method using reactive gas that contains perfluorodecalin.
[Claim 8] A method of forming a wiring structure comprising 12 steps:
a first step of forming a first insulating film over lower-level metal wiring,
a second step of forming a second insulating film having a different structure from that of said first insulating film over the aforementioned first insulating film,
a third step of forming a third insulating film having a different structure from that of said second insulating film over the aforementioned second insulating film,
a fourth step of forming a conducting film over the aforementioned third insulating film,
a fifth step of forming a first resist pattern having an opening for the formation of wiring over the aforementioned conducting film,
a sixth step of forming a mask pattern from the aforementioned conducting film with an opening for the formation of wiring by etching the aforementioned conducting film using the aforementioned first resist pattern as a mask,
a seventh step of forming a second resist pattern with an opening for the formation of contact holes over the aforementioned third insulating film,
an eighth step of patterning the aforementioned third insulating film so as to form an opening for the formation of contact holes in said third insulating film by dry etching the aforementioned third insulating film using the aforementioned first resist pattern or the second resist pattern as the mask under etching conditions such that the aforementioned third insulating film has a higher etching rate while the second insulating film has a lower etching rate relative to the first resist pattern and the second resist pattern,
a ninth step of patterning the aforementioned second insulating film so as to form an opening for the formation of contact holes in said second insulating film by dry etching the aforementioned second insulating film using the aforementioned first resist pattern or the second resist pattern as the mask under etching conditions such that the aforementioned second insulating film has a higher etching rate while the first insulating film and third insulating film have lower etching rates relative to the first resist pattern and the second resist pattern,
a tenth step of removing the aforementioned first resist pattern and the aforementioned second resist pattern,
an eleventh step of forming wiring grooves in the aforementioned third insulating film and of forming contact holes in the aforementioned first insulating film by dry etching of the aforementioned third insulating film using the aforementioned mask pattern as a mask and by dry etching of the aforementioned first insulating film using the aforementioned patterned second insulating film as a mask under etching conditions such that the etching rate of the aforementioned first insulating film and the third insulating film is higher while the etching rate of the aforementioned mask pattern and of the second insulating film is lower,
and a twelfth step of forming contacts that connect the upper-level metal wiring and the aforementioned lower-level metal wiring with the aforementioned upper-level metal wiring by packing metal film in the aforementioned wiring grooves and contact holes.
[Claim 9] The method of forming a wiring structure of Claim 8 in which the aforementioned third insulating film is a low-dielectric-constant SOG film with a siloxane framework.

[Detailed Description of the Invention]

[0001]

[Technical Field of Invention]

The present invention concerns a method of forming a wiring structure in semiconductor integrated circuit devices.

[0002]

[Related Art]

Accompanying higher integration of semiconductor integrated circuits, expansion of the wiring delay times attributable to increase in the interwiring capacitance, which is parasitic capacitance between metal wiring, has blocked higher performance of semiconductor integrated circuits. The wiring delay time is known as the so-called RC delay, which is proportional to the product of the metal wiring resistance and the interwiring capacitance.

[0003]

Accordingly, the resistance of the metal wiring must be reduced or the inter-wiring capacitance must be reduced in order to reduce the wiring delay time.

[0004]

Thus, IBM and Motorola have reported semiconductor integrated circuit devices that use copper instead of aluminum alloy as material for wiring in order to reduce the wiring resistance. Copper material has a specific resistance about two-thirds as high as that of an aluminum alloy material. Accordingly, in accordance with simple calculation, the wiring

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