FILE HISTORY

US 6,197,696

PATENT:	6,197,696
INVENTORS:	Aoi, Nobuo
TITLE:	Method for forming interconnection structure
APPLICATION NO:	US1999274114A
FILED:	23 MAR 1999
ISSUED:	06 MAR 2001
COMPILED:	12 MAY 2015

09/274114
03/23/99

ISSUE CLASSIFICATION	Class	Subclass
	438	700

PATENT NUMBER
6197696
6197696

U.S. UTILITY PATENT APPLICATION

O.I.P.E.	PATENT DATE
SCANNED TWO Q.A. KD	MAR 06 2001

SECTOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
	438	—	1765	

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(Attached in pocket on right inside flap)

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PREPARED AND APPROVED FOR ISSUE

ISSUING CLASSIFICATION

ORIGINAL CLASS	ORIGINAL SUBCLASS	CROSS REFERENCE(S) CLASS	CROSS REFERENCE(S) SUBCLASS (ONE SUBCLASS PER BLOCK)
438	700	706	

INTERNATIONAL CLASSIFICATION: H01L 21/311

☐ Continued on Issue Slip Inside File Jacket

1-31-01 Formal Drawings (37 shts) set L 3/23/99

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
	37	108	3b	15	1

☐ a) The term of this patent subsequent to _____ (date) has been disclaimed.

Lynette T. Umez-Eronini 10/6/2000
(Assistant Examiner) (Date)

☐ b) The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____

Benjamin L. Utech
BENJAMIN L. UTECH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700
10/11/00
(Primary Examiner) (Date)

NOTICE OF ALLOWANCE MAILED: 10-10-00

ISSUE FEE

Amount Due	Date Paid
$1240.00	1-9-01

☐ c) The terminal ____ months of this patent have been disclaimed.

(Legal Instruments Examiner) (Date)

ISSUE BATCH NUMBER: 753

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Form PTO-436A
(Rev. 6/98)

ISSUE FEE IN FILE

(LABEL AREA)

Formal Drawings(shts)set

(FACE)

METHOD FOR FORMING INTERCONNECTION STRUCTURE

Transaction History

Date	Transaction Description
03-23-1999	Workflow - Drawings Finished
03-23-1999	Workflow - Drawings Matched with File at Contractor
03-23-1999	Workflow - Drawings Received at Contractor
03-29-1999	Initial Exam Team nn
04-09-1999	IFW Scan & PACR Auto Security Review
04-14-1999	Application Dispatched from OIPE
05-11-1999	Case Docketed to Examiner in GAU
06-25-1999	Request for Foreign Priority (Priority Papers May Be Included)
08-09-1999	Information Disclosure Statement (IDS) Filed
08-09-1999	Information Disclosure Statement (IDS) Filed
02-09-2000	Information Disclosure Statement (IDS) Filed
02-09-2000	Information Disclosure Statement (IDS) Filed
10-05-2000	Case Docketed to Examiner in GAU
10-10-2000	Mail Notice of Allowance
10-10-2000	Notice of Allowance Data Verification Completed
11-29-2000	Workflow - File Sent to Contractor
01-09-2001	Issue Fee Payment Verified
01-31-2001	Workflow - Complete WF Records for Drawings
02-04-2001	Application Is Considered Ready for Issue
02-15-2001	Issue Notification Mailed
03-06-2001	Recordation of Patent Grant Mailed

jc530 U.S. PTO
09/274114
03/23/99

APR 07 1999

PATENT APPLICATION

09274114

CONTENTS

	Date received (Incl. C. of M.) or Date Mailed		Date received (Incl. C. of M.) or Date Mailed
1. Application ✓ papers.		42.	
2. Priority Paper	6-25-99	43.	
3. IDS	8.9.99	44.	
4. IDS / Prior Art	2-9-00	45.	
10/10 5. Allowance	10-10-00	46.	
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ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	MM	67814	4/11/99
O.I.P.E. CLASSIFIER		5	4-7-99
FORMALITY REVIEW	DB	70014	4/13/99

INDEX OF CLAIMS

✔	Rejected	N	Non-elected
=	Allowed	I	Interference
—	(Through numeral)... Canceled	A	Appeal
÷	Restricted	O	Objected

Claim Final	Claim Original	Date
1	(1)	10/6/2003
2	2	
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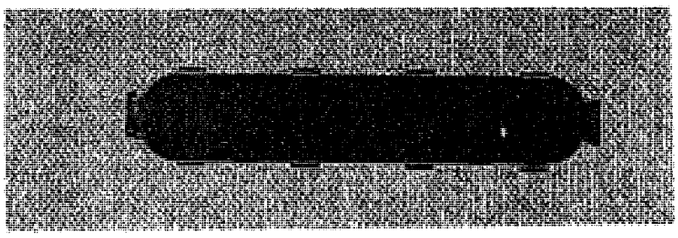

SEARCHED

Class	Sub.	Date	Exmr.
435 ↓	700 706	~~L.J.N.E~~ 10/6/2005 ↓	L.J.N.E ↓

SEARCH NOTES
(INCLUDING SEARCH STRATEGY)

	Date	Exmr.
EAST	10/6/2005	L.J.N.E

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.

(RIGHT OUTSIDE)

US006197696B1

(12) **United States Patent**
Aoi

(10) **Patent No.: US 6,197,696 B1**
(45) **Date of Patent: Mar. 6, 2001**

(54) **METHOD FOR FORMING INTERCONNECTION STRUCTURE**

(75) Inventor: **Nobuo Aoi**, Hyogo (JP)

(73) Assignee: **Matsushita Electric Industrial Co., Ltd.**, Osaka (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/274,114**

(22) Filed: **Mar. 23, 1999**

(30) **Foreign Application Priority Data**

Mar. 26, 1998 (JP) 10-079371

(51) **Int. Cl.**[7] **H01L 21/311**
(52) **U.S. Cl.** **438/700**; 438/706
(58) **Field of Search** 438/700, 706

(56) **References Cited**

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9-64034	3/1997	(JP)	H01L/21/3205
9-153545	6/1997	(JP)	H01L/21/768

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European Search Report dated Jul. 1, 1999.

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Primary Examiner—Benjamin L. Utech
Assistant Examiner—Lynette T. Umez-Eronini
(74) *Attorney, Agent, or Firm*—Eric J. Robinson; Nixon Peabody LLP

(57) **ABSTRACT**

In a method for forming an interconnection structure, first, second and third insulating films and a thin film are sequentially formed over lower-level metal interconnects. Then, the thin film is masked with a first resist pattern and etched to form a mask pattern with openings for interconnects. Next, the third insulating film is masked with a second resist pattern and dry-etched such that the third insulating film and the first and second resist patterns are etched at a high rate and that the second insulating film is etched at a low rate to form openings for contact holes in the third insulating film and remove the first and second resist patterns. Then, the second insulating film is masked with the third insulating film and dry-etched such that the second insulating film is etched at a high rate and that the first and third insulating films are etched at a low rate to form the openings for contact holes in the second insulating film. Then, the third and first insulating films are masked with the mask pattern and the second insulating film, respectively, and dry-etched such that the first and third insulating films are etched at a high rate and that the mask pattern and the second insulating film are etched at a low rate to form wiring grooves and contact holes in the third and first insulating films, respectively. Finally, upper-level metal interconnects and contacts are formed.

15 Claims, 37 Drawing Sheets

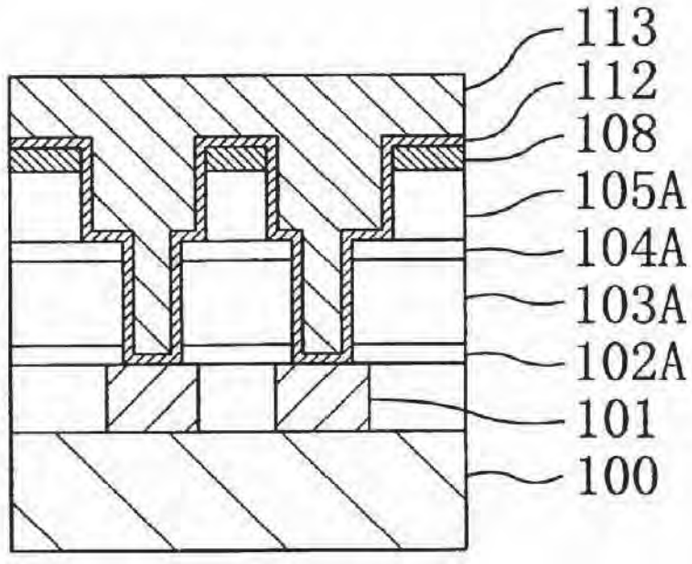


Fig. 1(a)

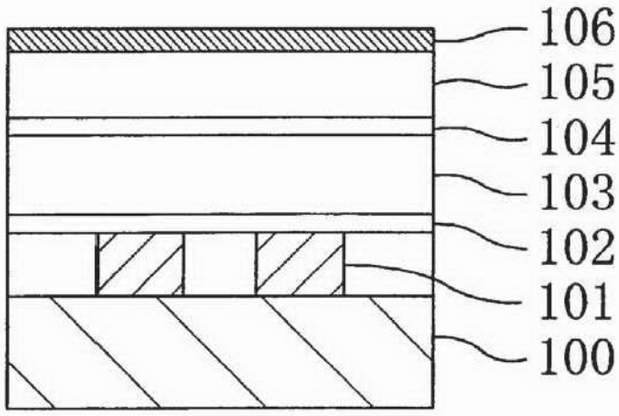


Fig. 1(b)

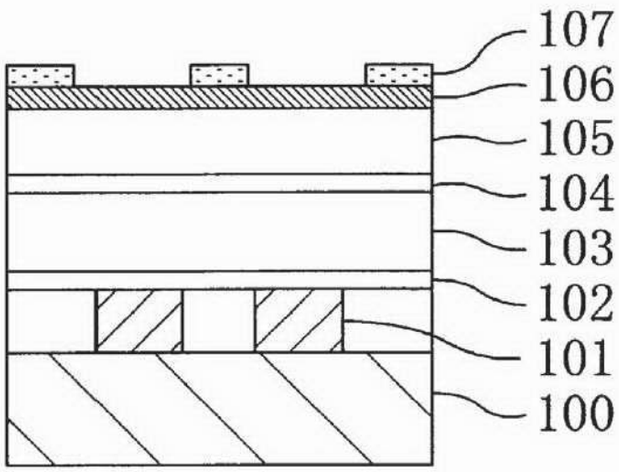


Fig. 1(c)

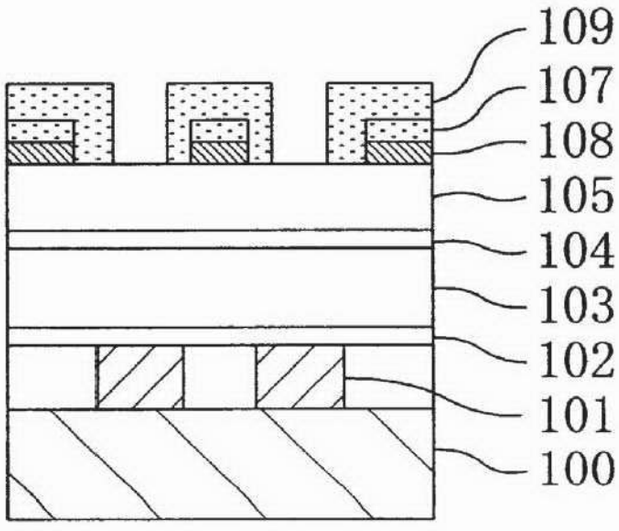


Fig. 2(a)

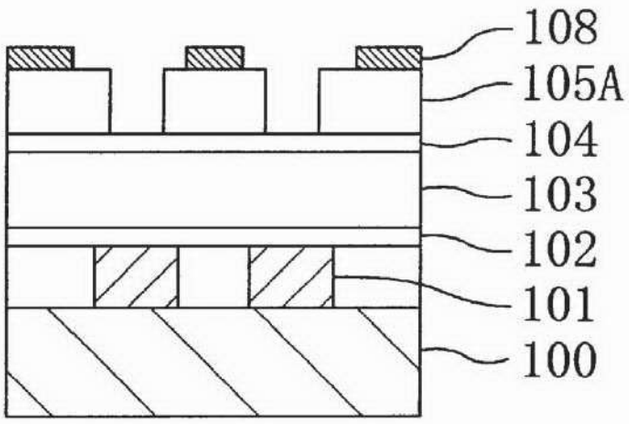


Fig. 2(b)

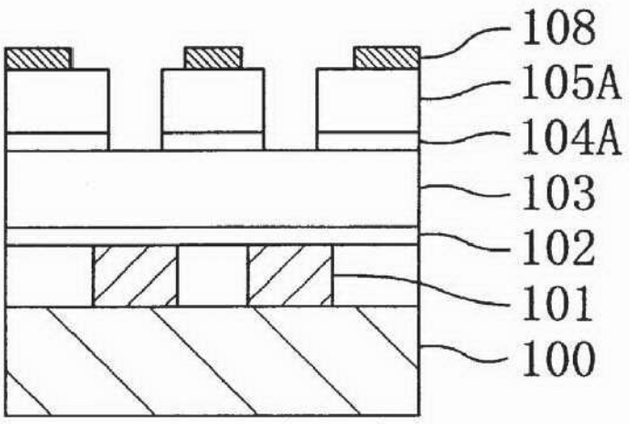


Fig. 2(c)

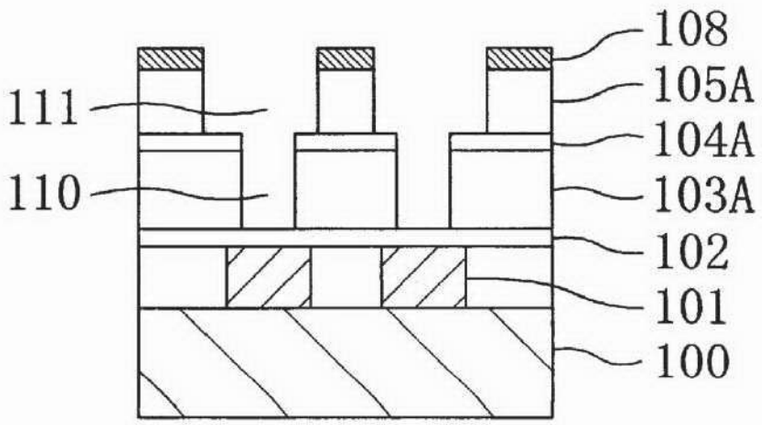


Fig. 3(a)

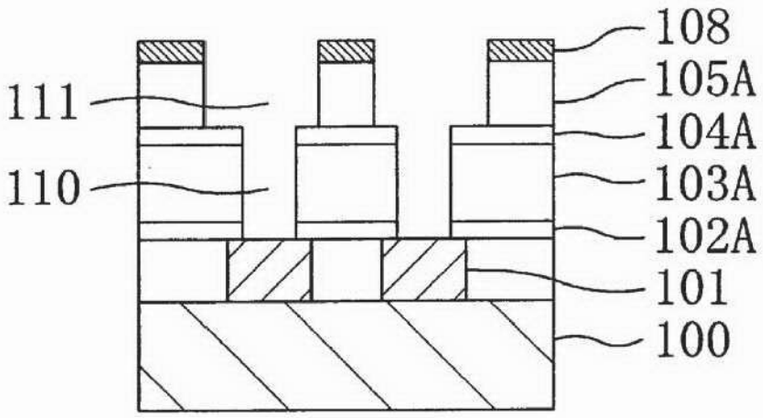


Fig. 3(b)

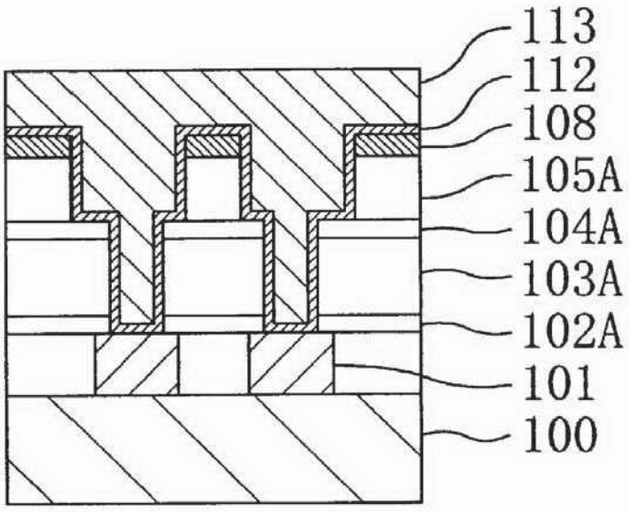


Fig. 3(c)

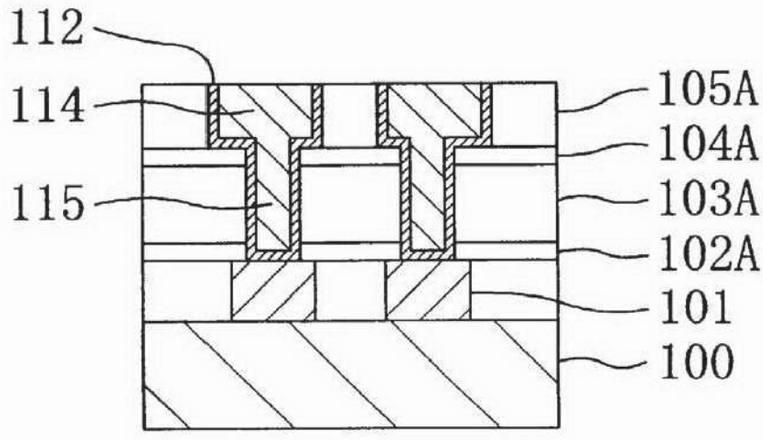


Fig. 4(a)

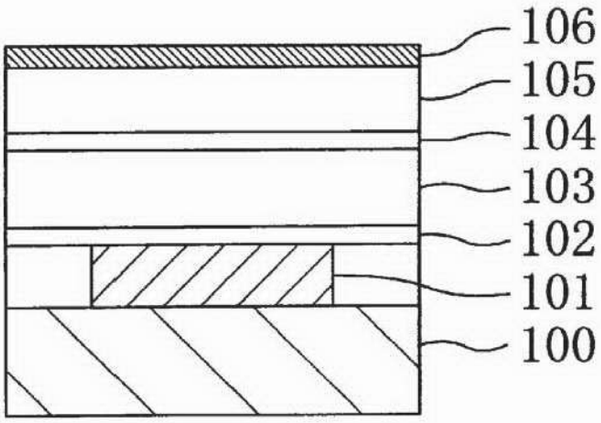


Fig. 4(b)

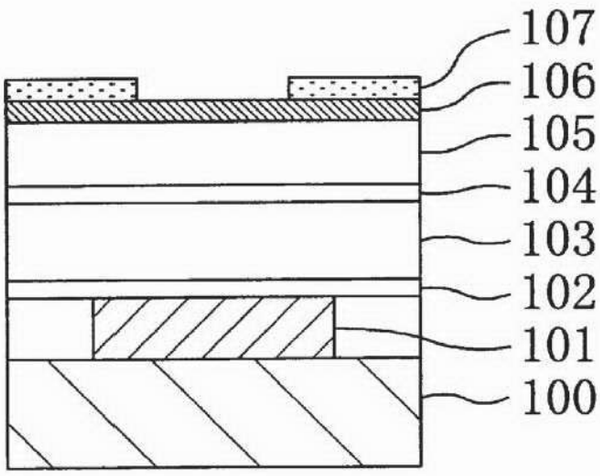


Fig. 4(c)

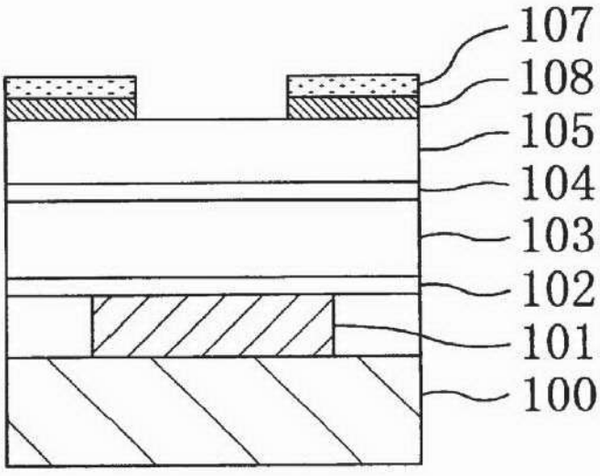


Fig. 5(a)

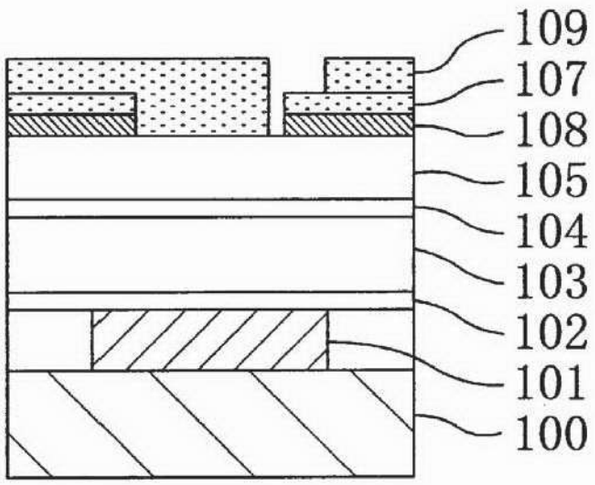


Fig. 5(b)

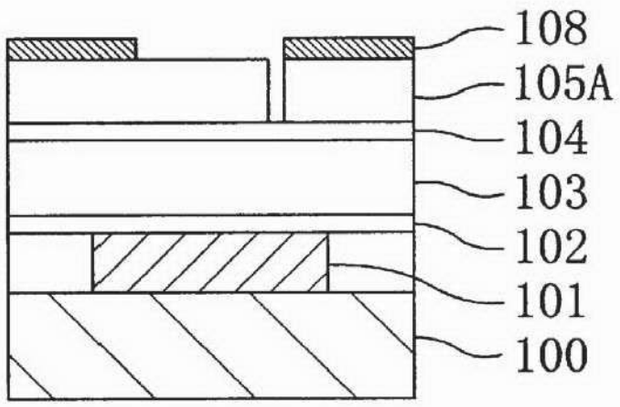


Fig. 5(c)

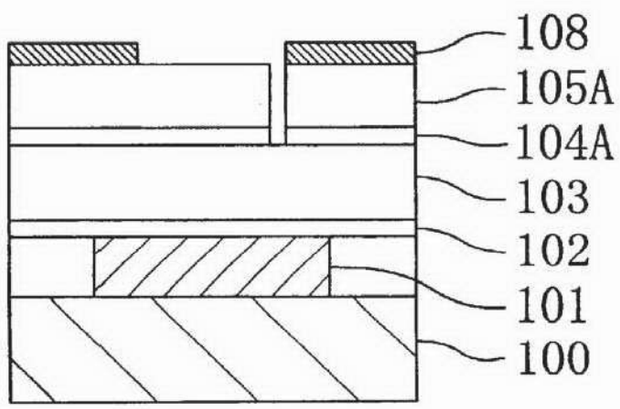


Fig. 6(a)

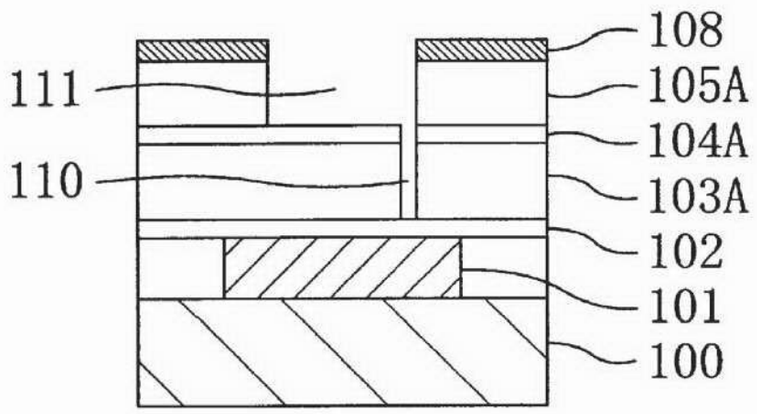


Fig. 6(b)

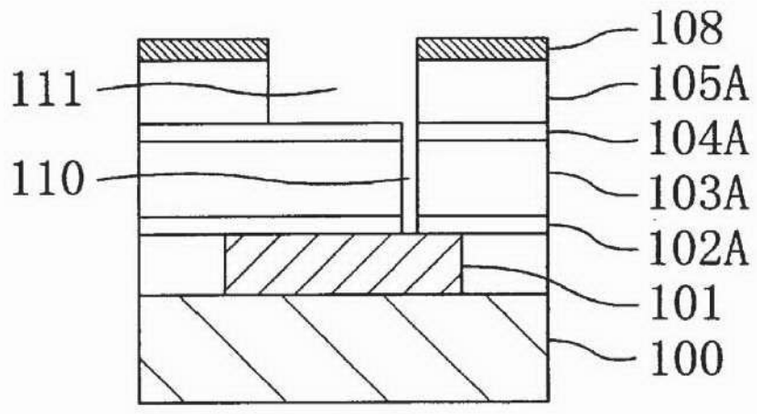


Fig. 6(c)

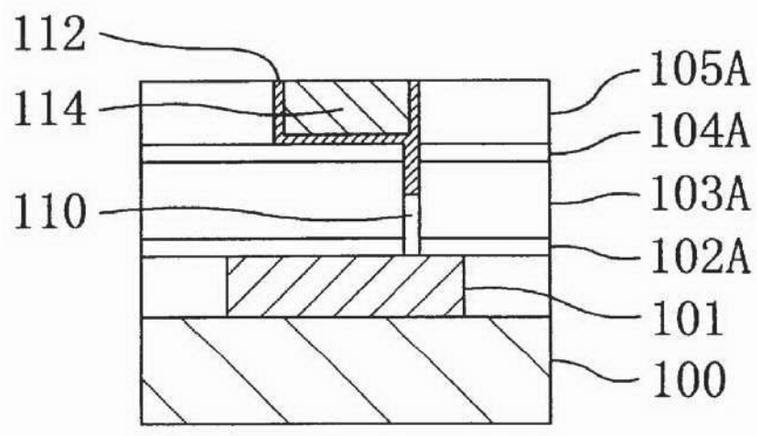


Fig. 7(a)

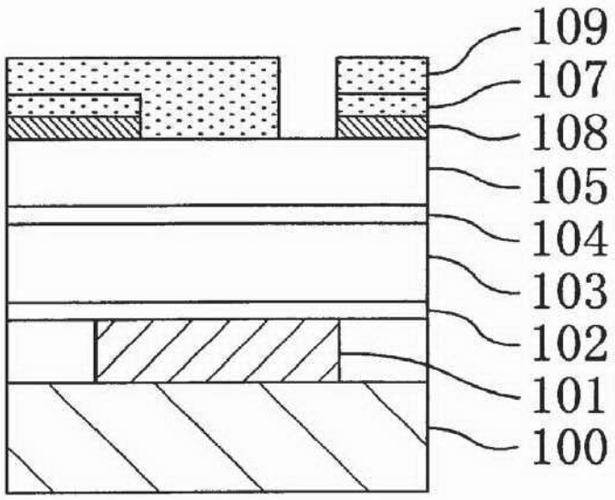


Fig. 7(b)

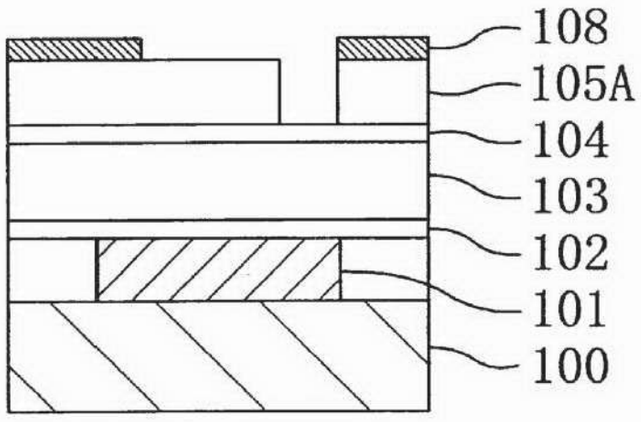


Fig. 7(c)

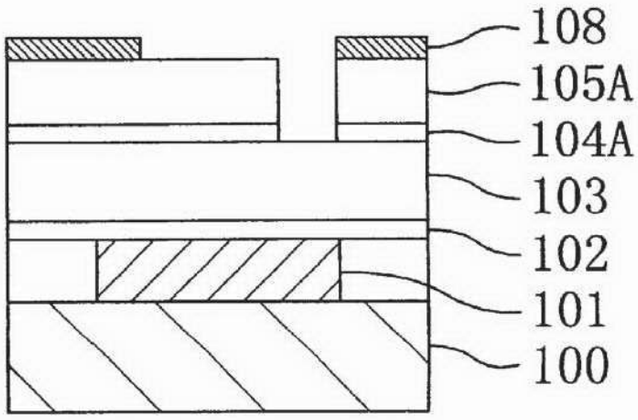


Fig. 8(a)

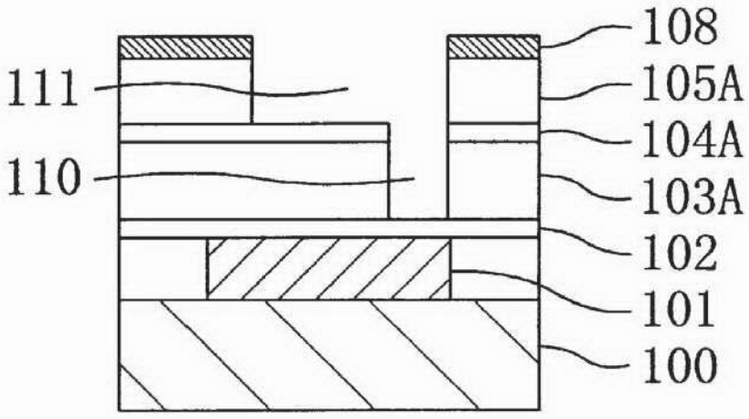


Fig. 8(b)

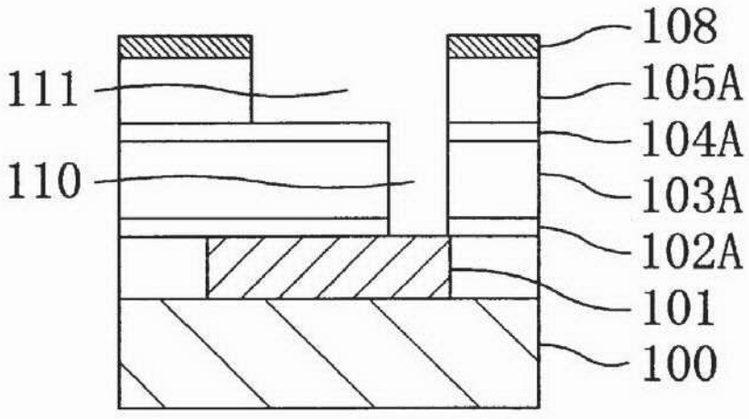


Fig. 8(c)

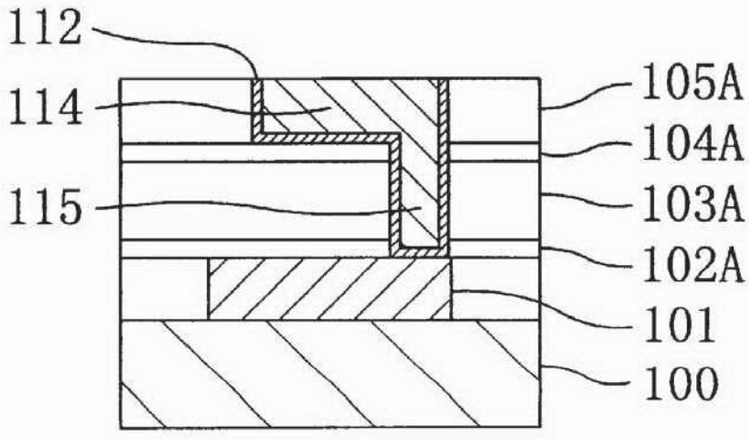


Fig. 9(a)

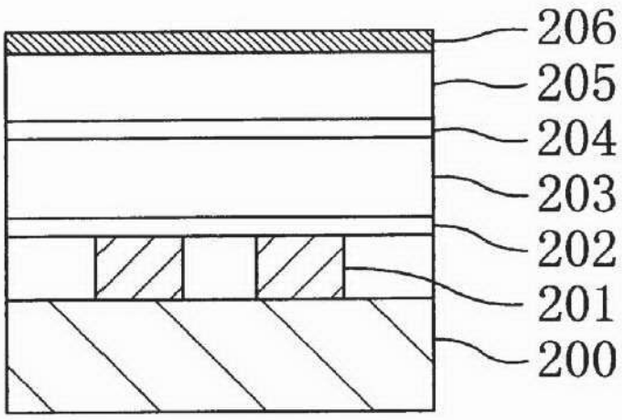


Fig. 9(b)

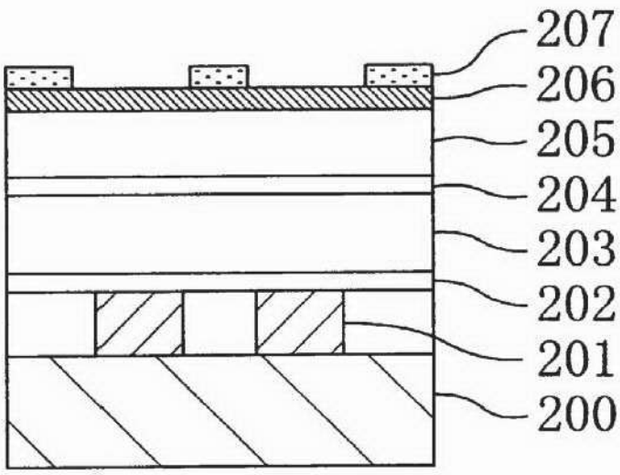


Fig. 9(c)

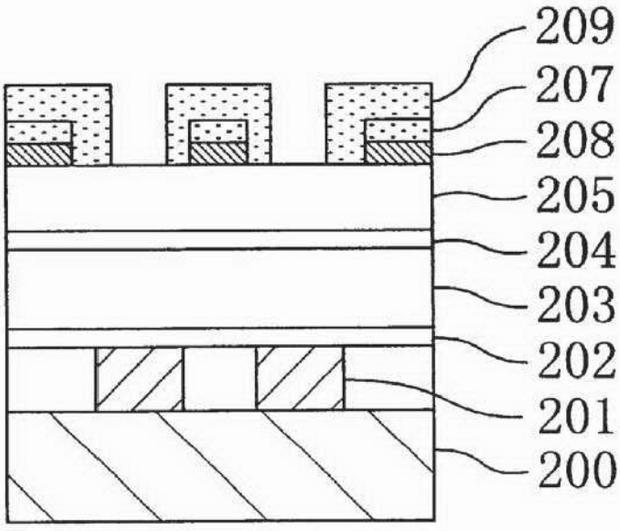


Fig. 10(a)

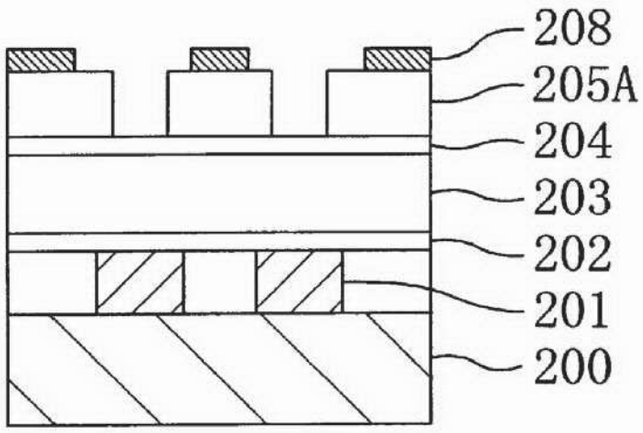


Fig. 10(b)

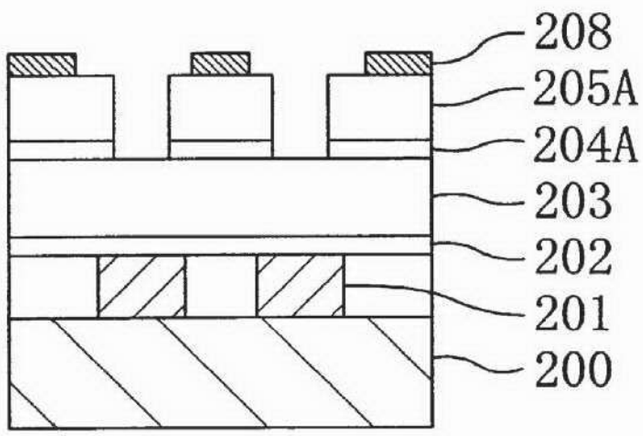


Fig. 10(c)

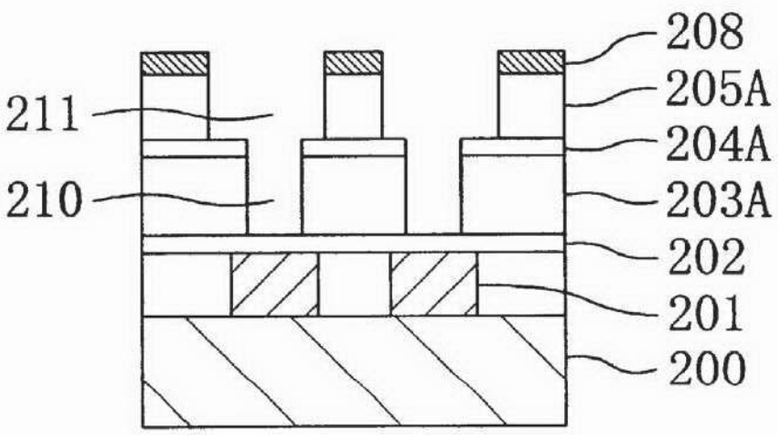


Fig. 11(a)

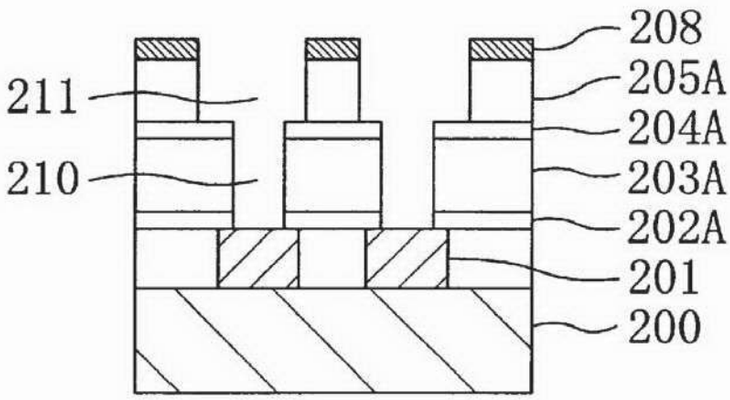


Fig. 11(b)

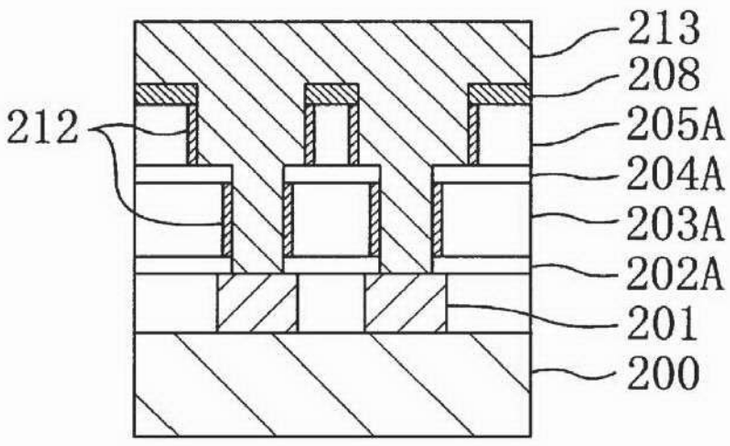


Fig. 11(c)

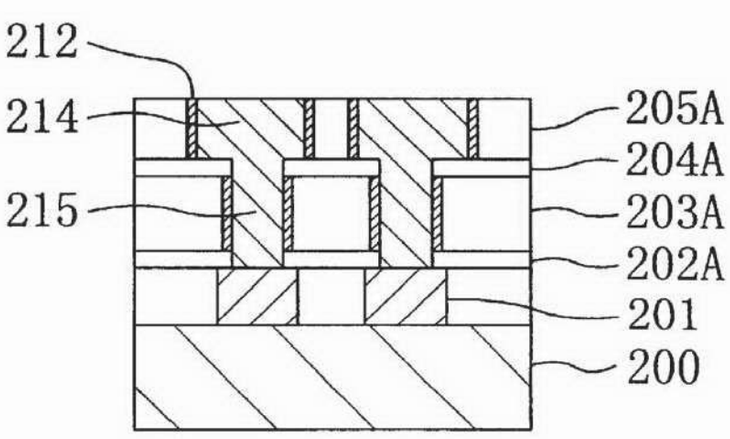


Fig. 12(a)

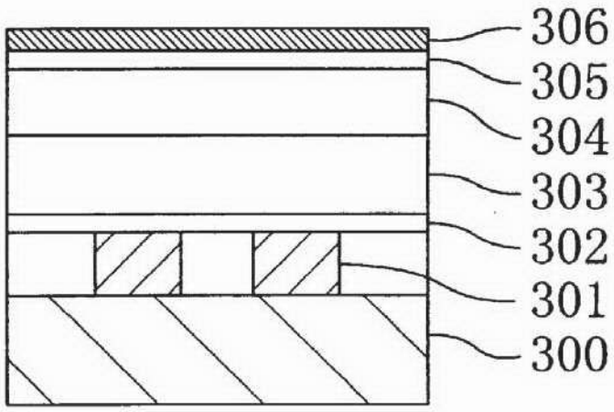


Fig. 12(b)

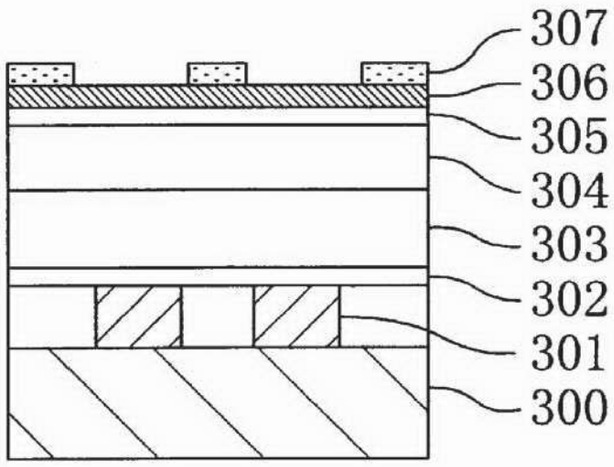


Fig. 12(c)

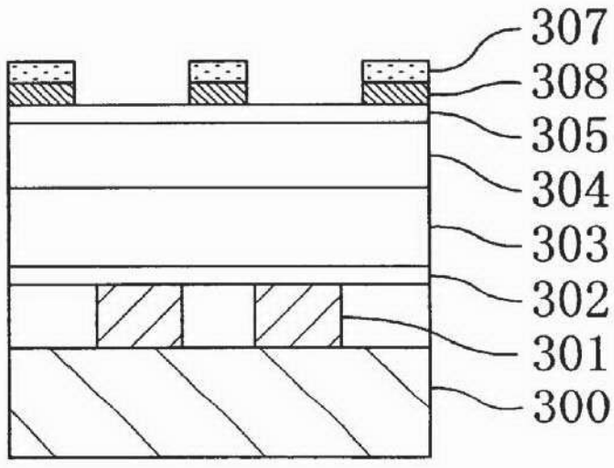


Fig. 13(a)

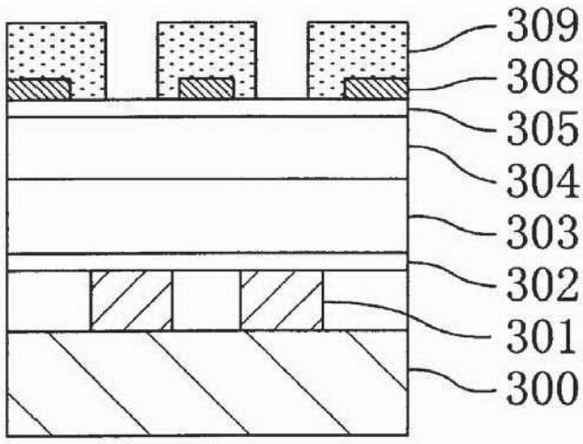


Fig. 13(b)

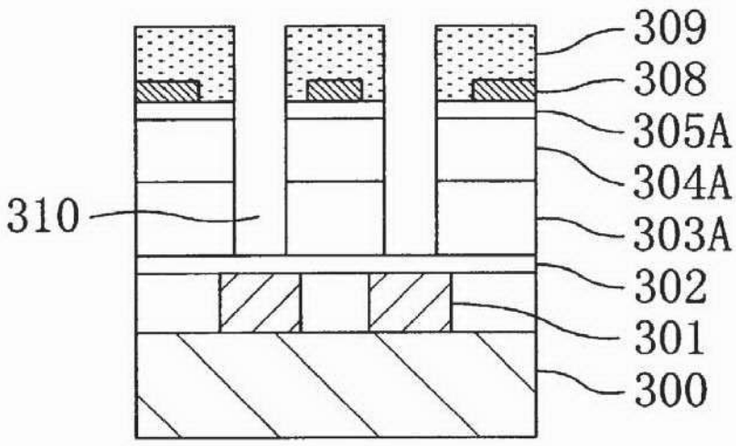


Fig. 13(c)

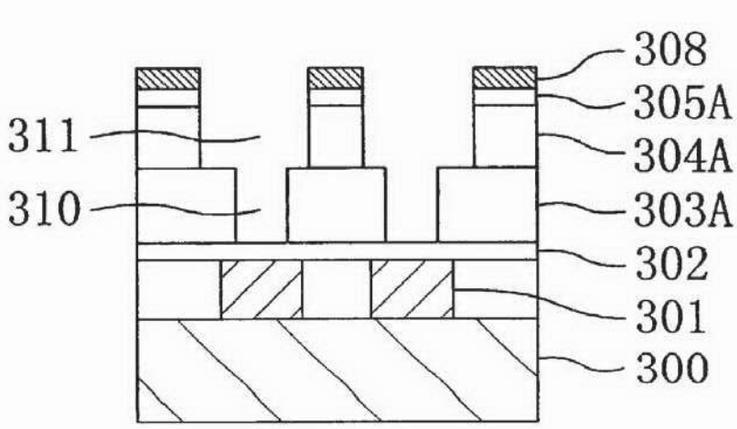


Fig. 14(a)

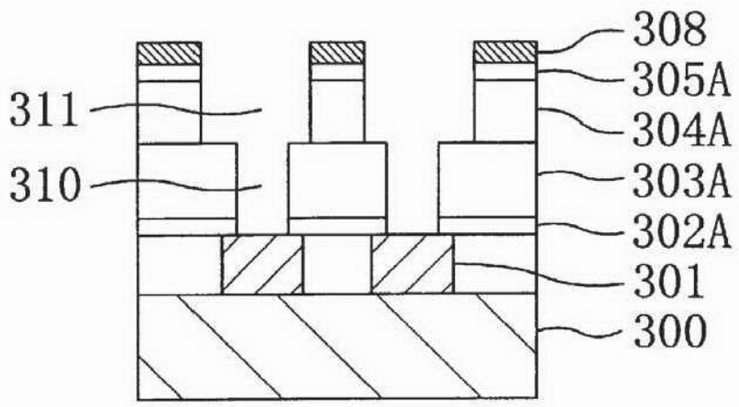


Fig. 14(b)

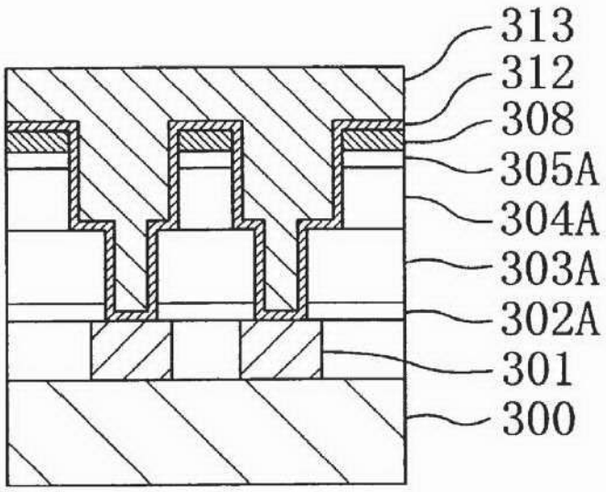


Fig. 14(c)

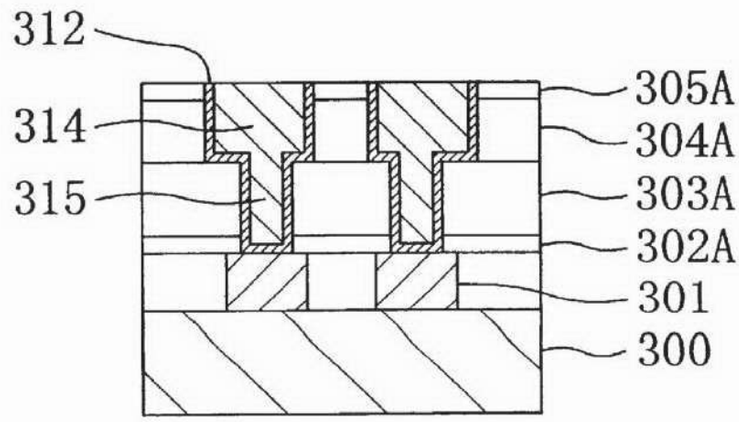


Fig. 15(a)

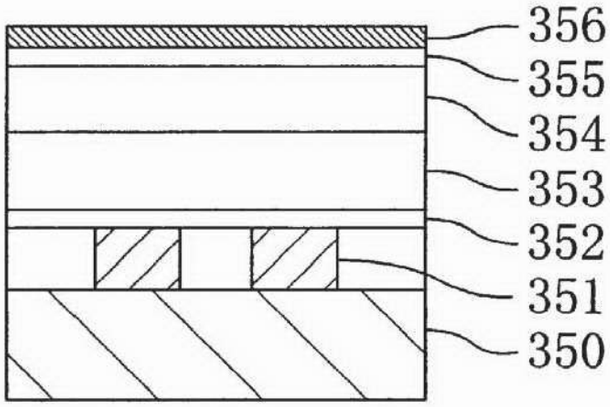


Fig. 15(b)

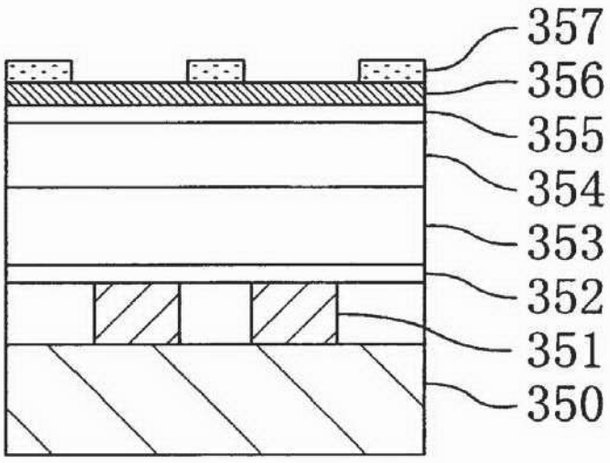


Fig. 15(c)

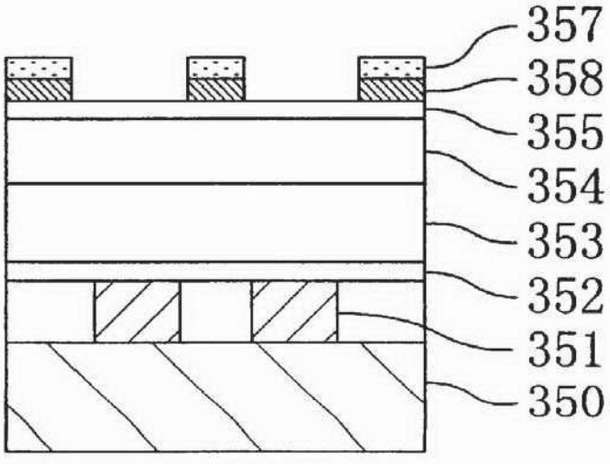


Fig. 16(a)

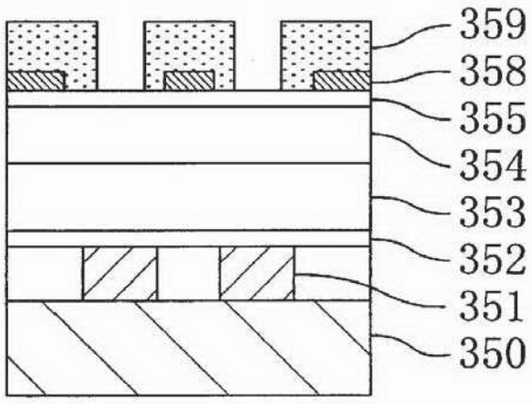


Fig. 16(b)

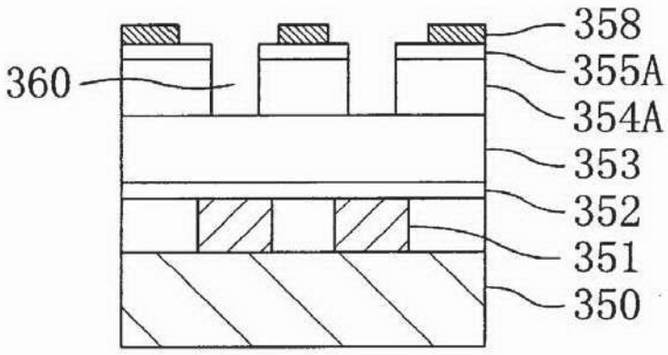


Fig. 16(c)

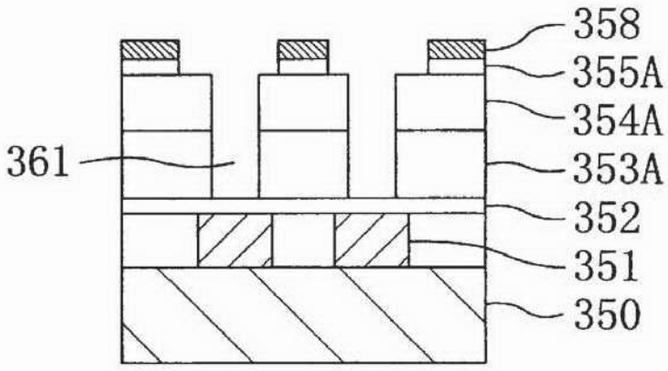


Fig. 16(d)

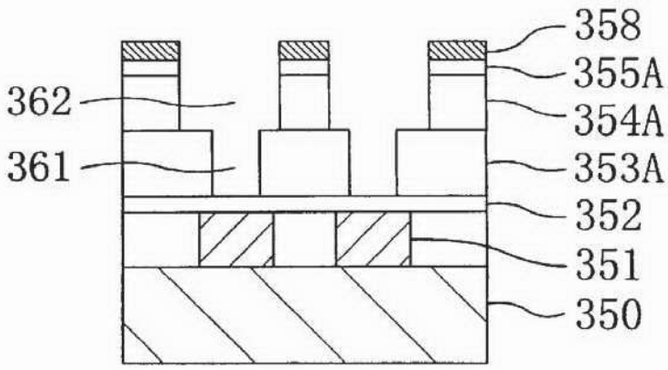


Fig. 17(a)

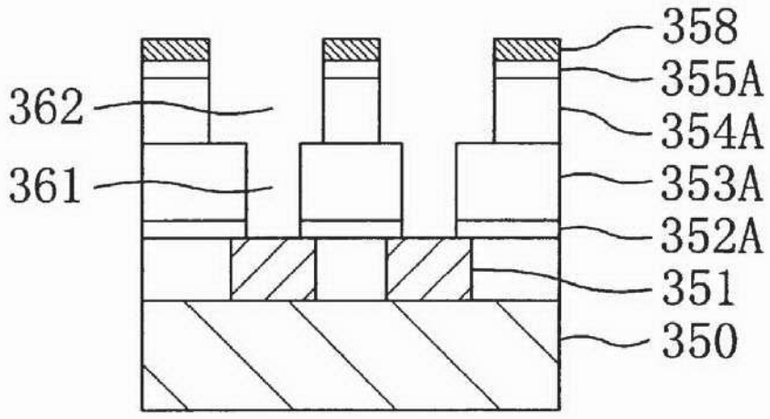


Fig. 17(b)

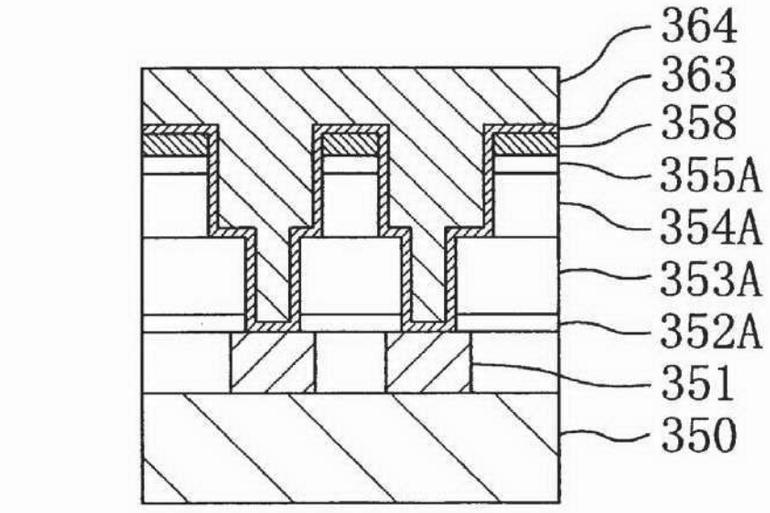


Fig. 17(c)

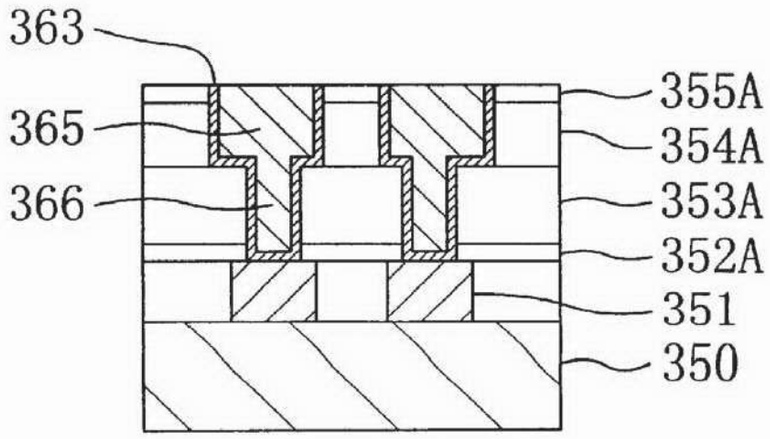


Fig. 18(a)

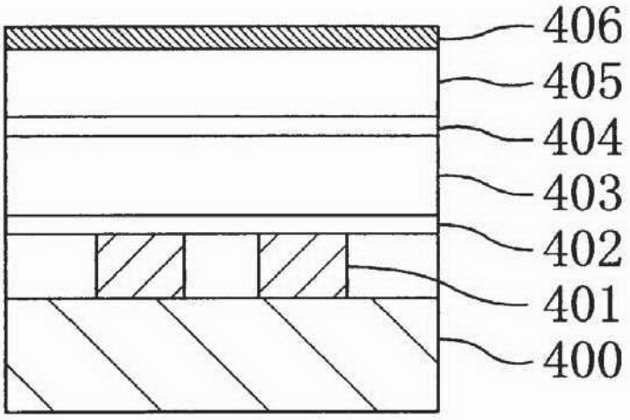


Fig. 18(b)

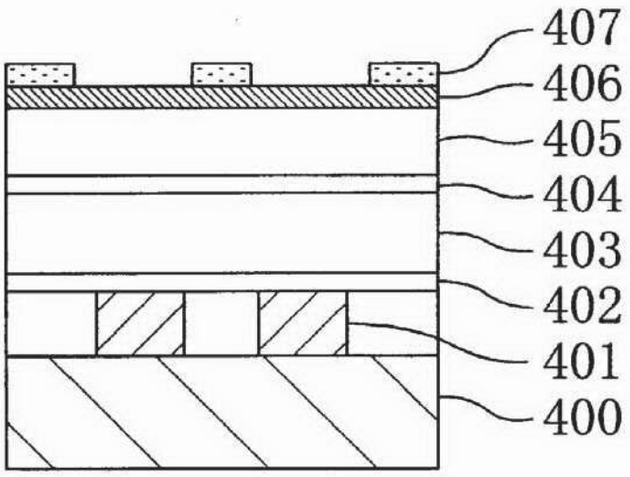


Fig. 18(c)

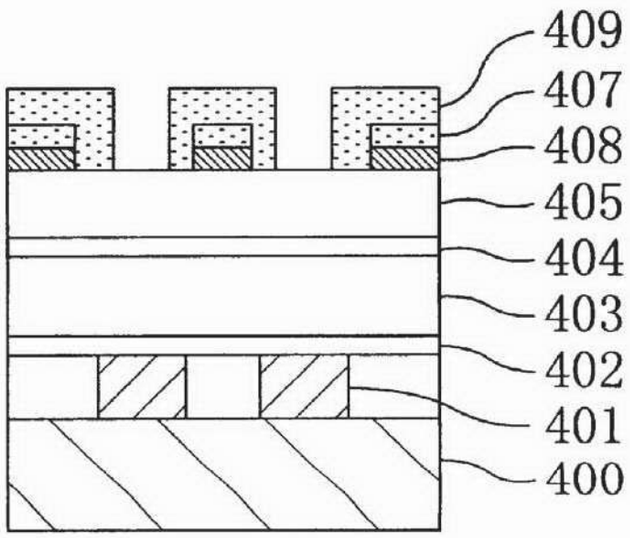


Fig. 19(a)

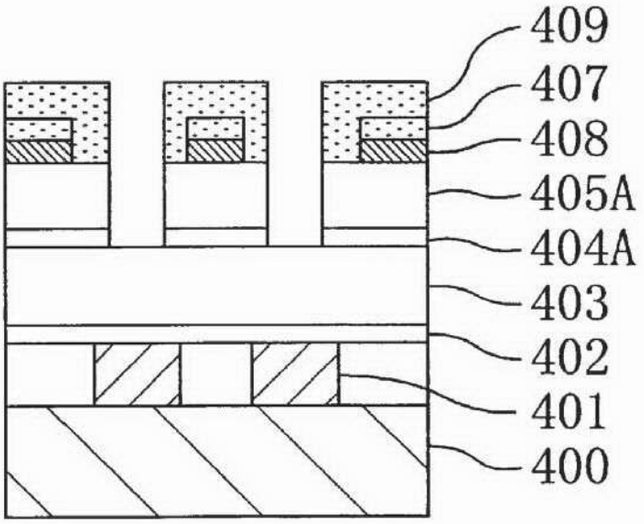


Fig. 19(b)

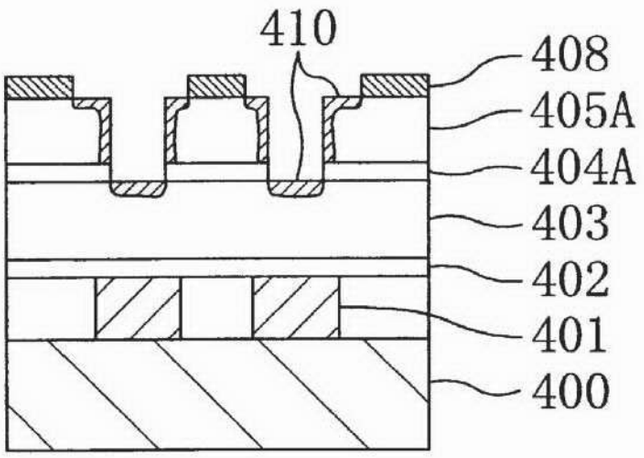


Fig. 19(c)

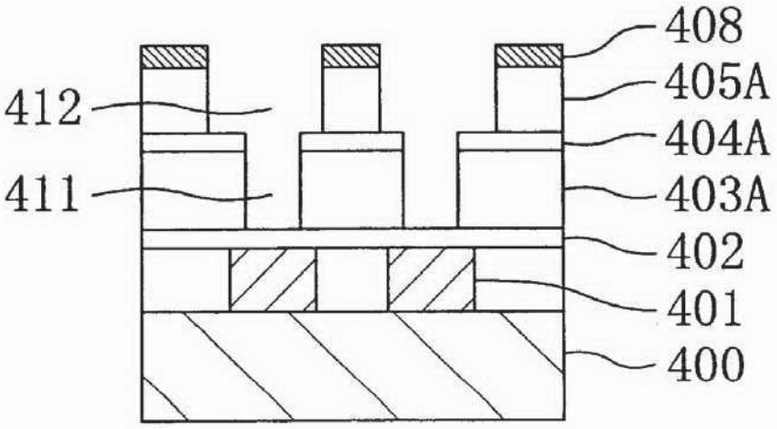


Fig. 20(a)

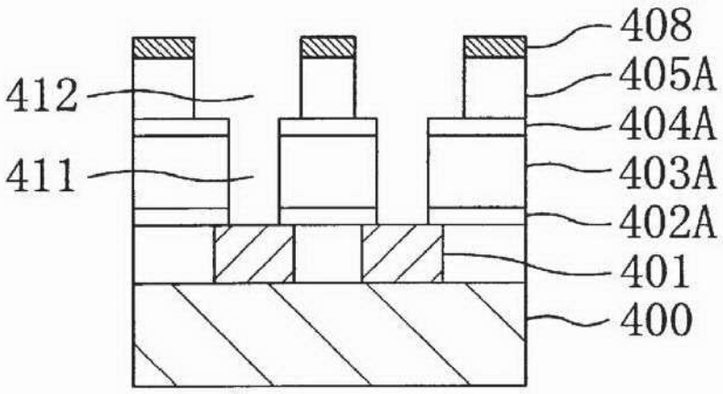


Fig. 20(b)

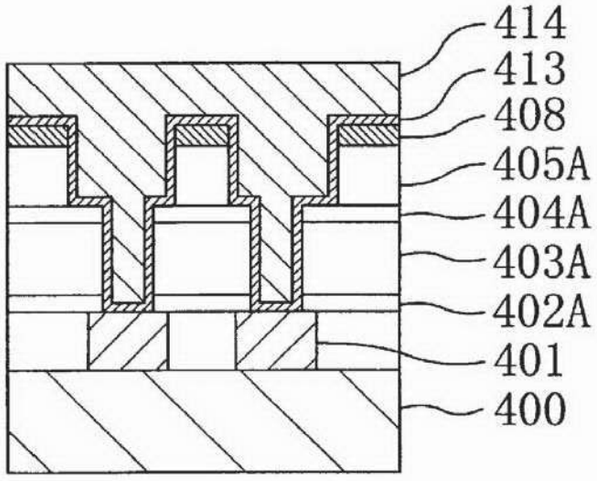


Fig. 20(c)

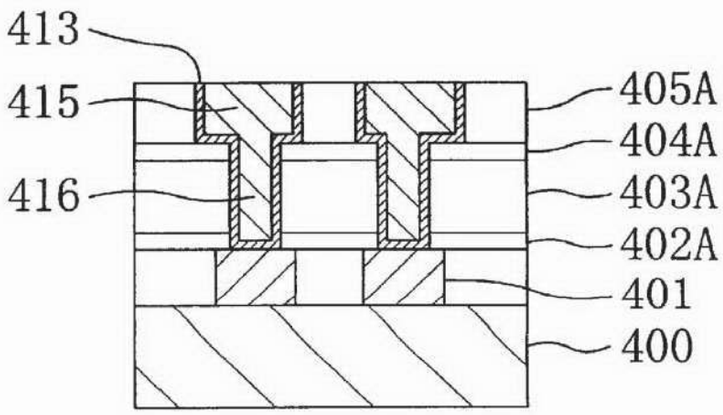


Fig. 21(a)

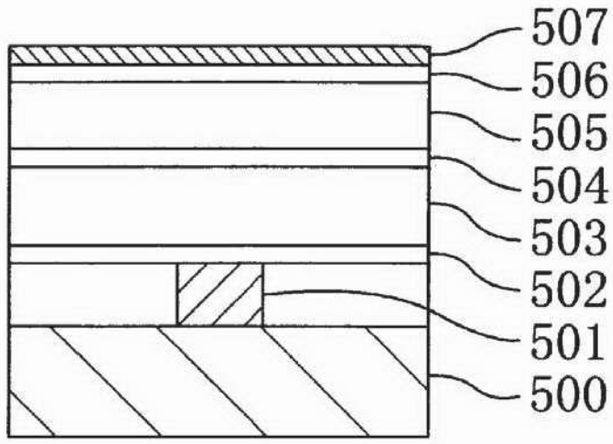


Fig. 21(b)

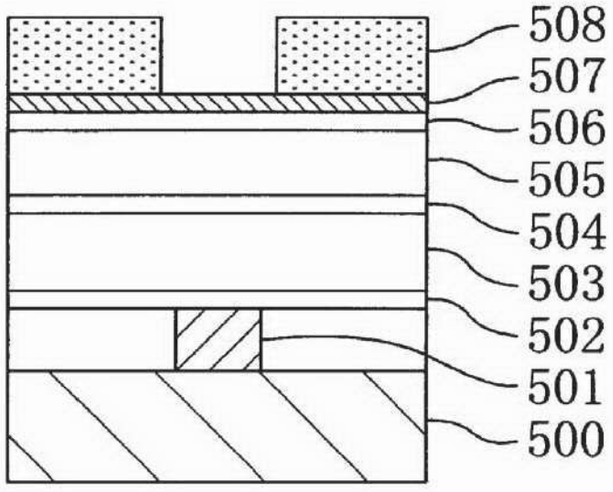


Fig. 21(c)

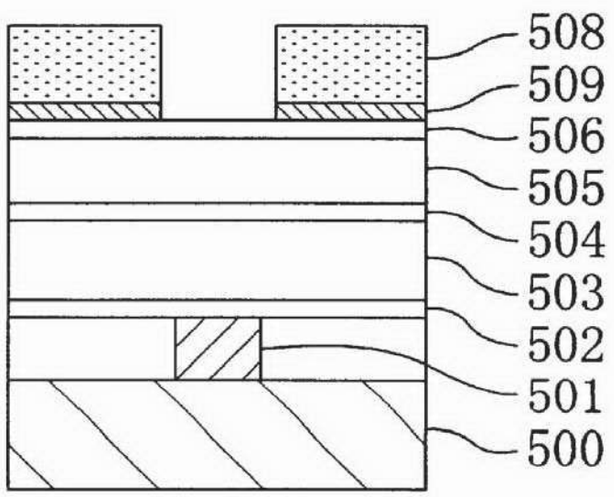


Fig. 22(a)

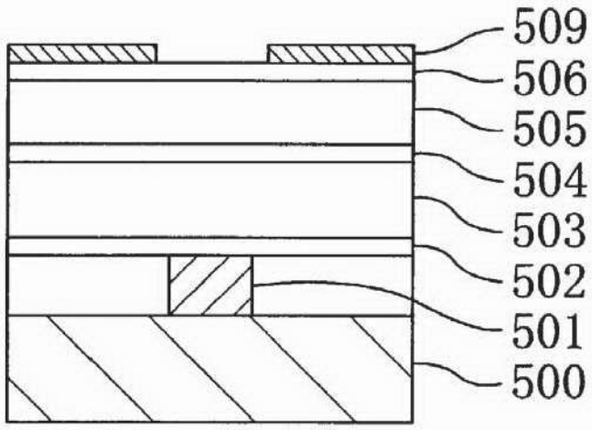


Fig. 22(b)

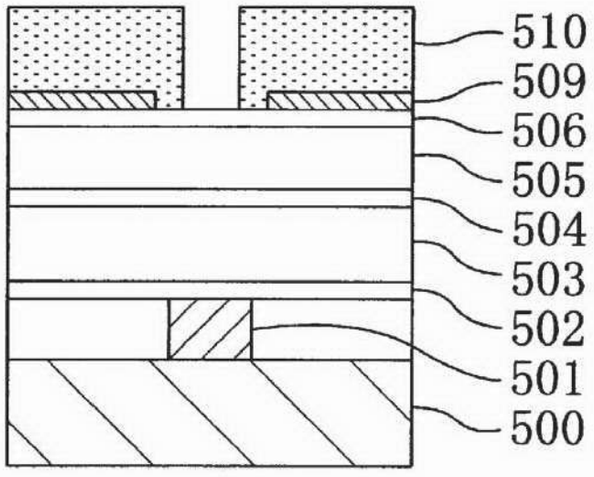


Fig. 22(c)

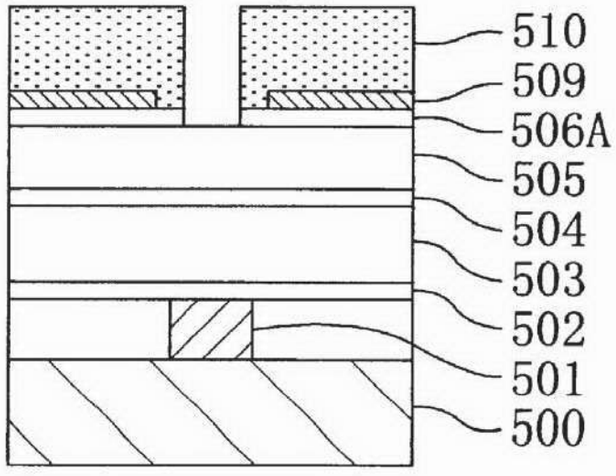


Fig. 23(a)

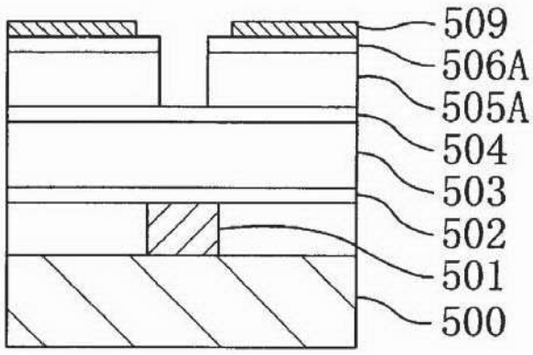


Fig. 23(b)

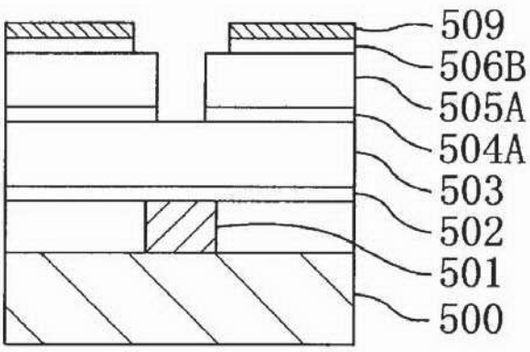


Fig. 23(c)

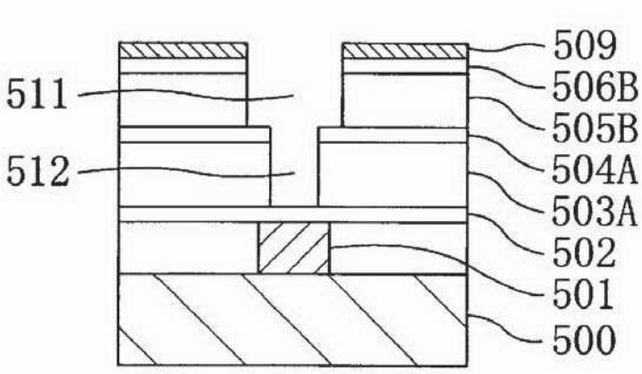


Fig. 23(d)

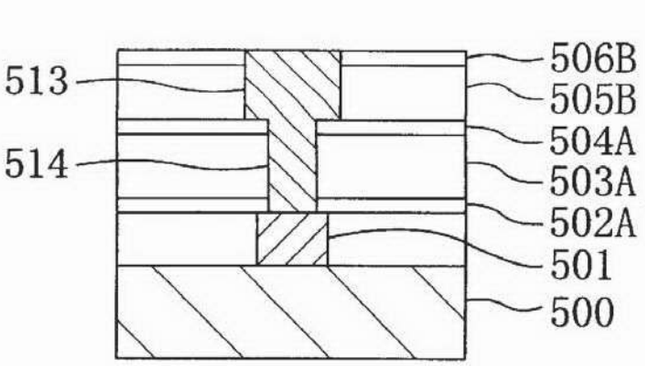


Fig. 24(a)

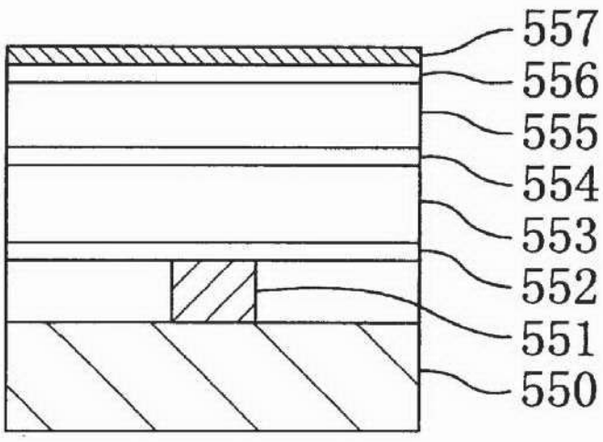


Fig. 24(b)

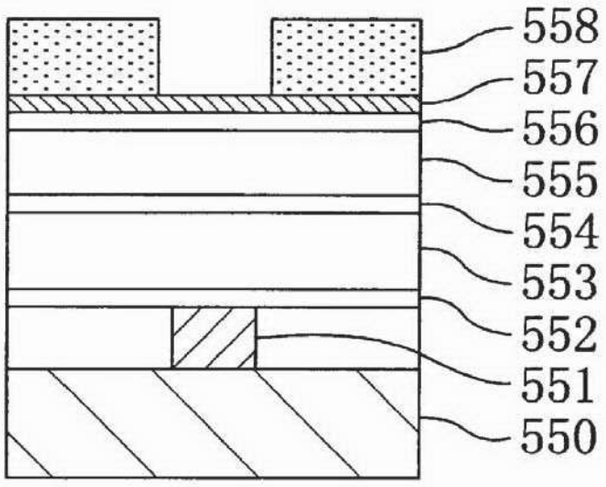


Fig. 24(c)

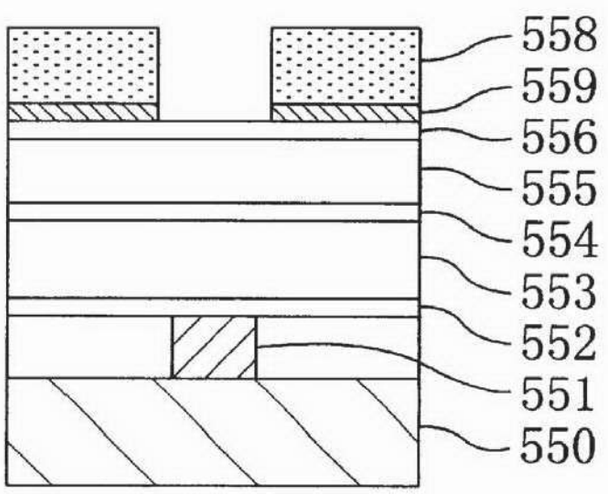


Fig. 25(a)

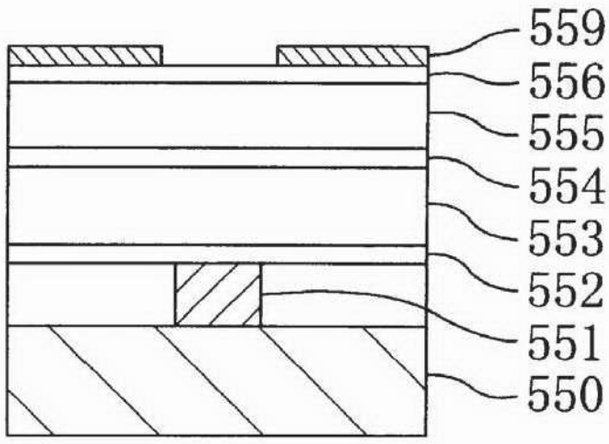


Fig. 25(b)

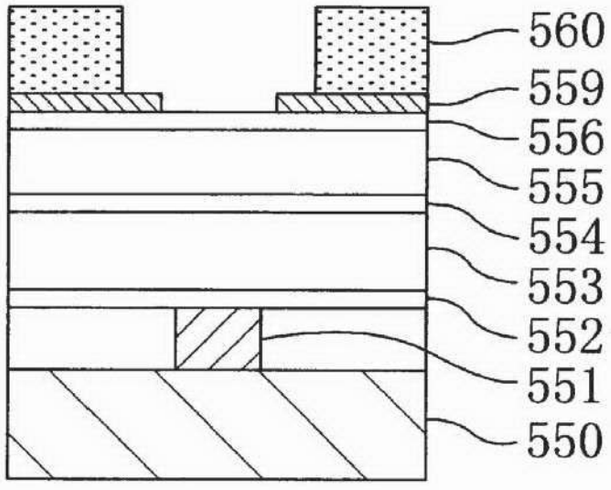


Fig. 25(c)

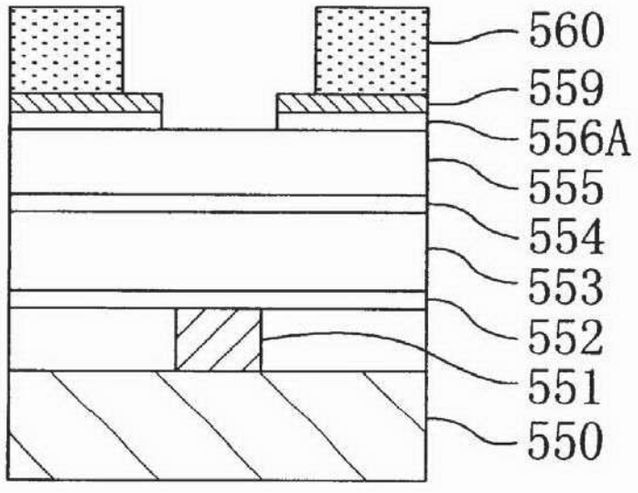


Fig. 26(a)

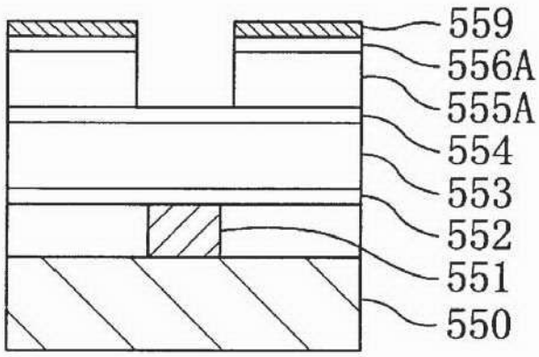


Fig. 26(b)

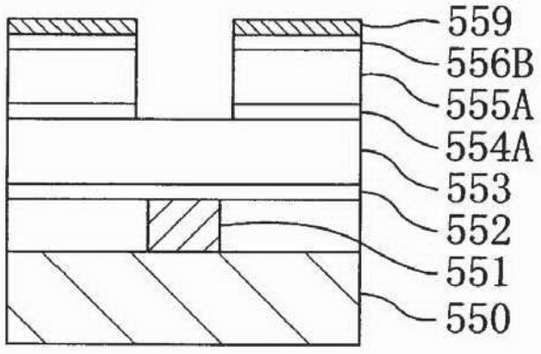


Fig. 26(c)

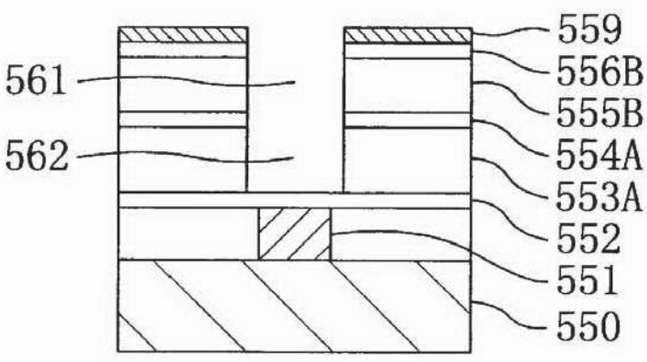


Fig. 26(d)

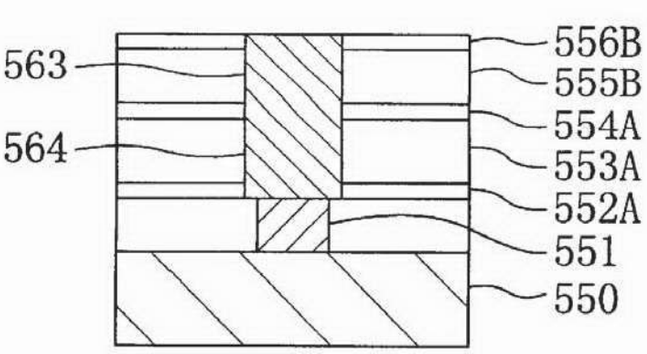


Fig. 27(a)

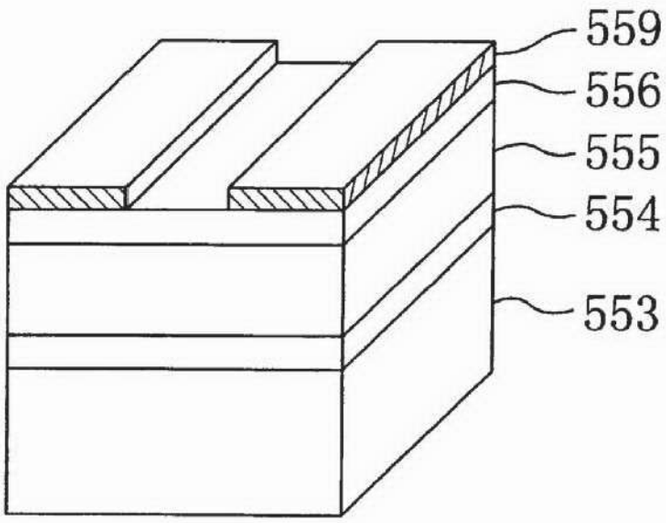


Fig. 27(b)

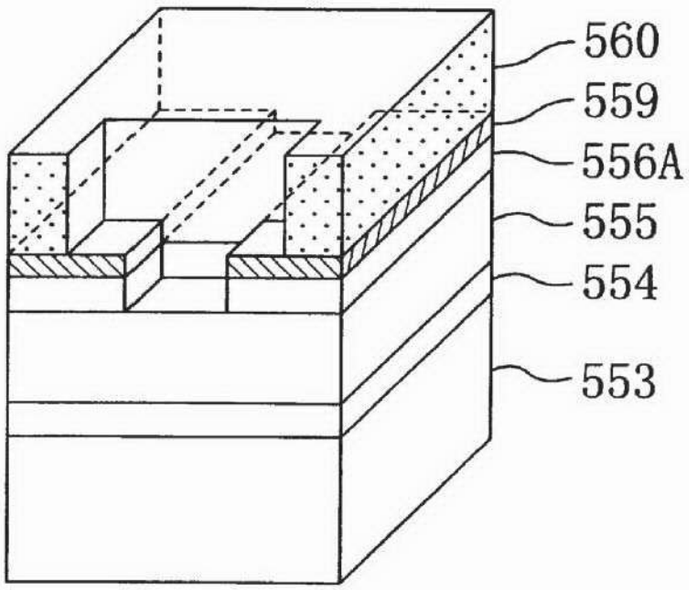


Fig. 28(a)

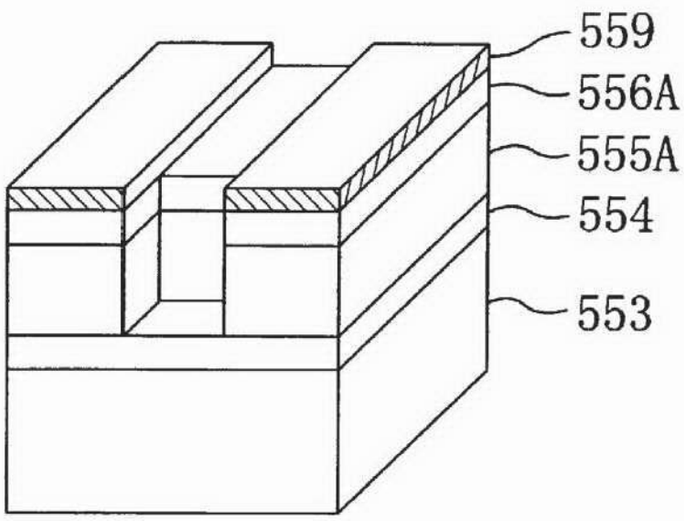


Fig. 28(b)

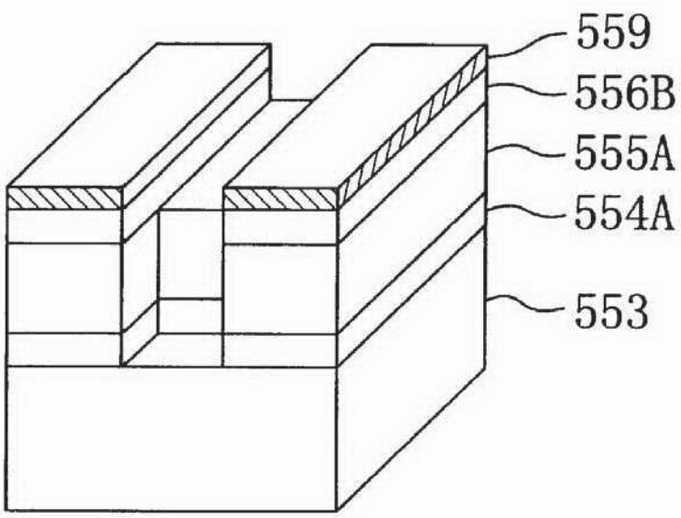


Fig. 29(a)

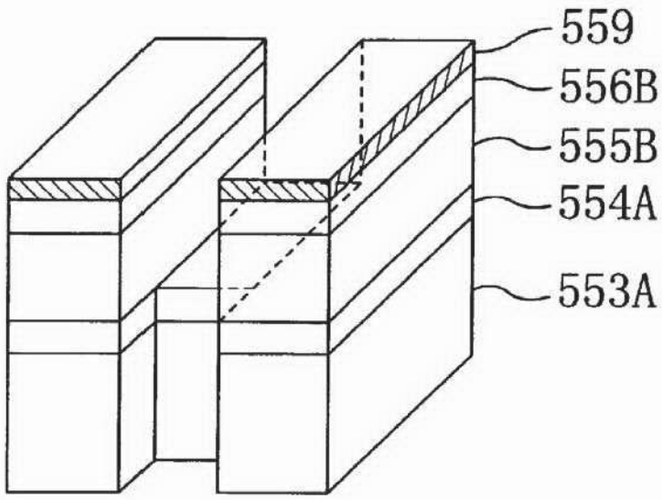


Fig. 29(b)

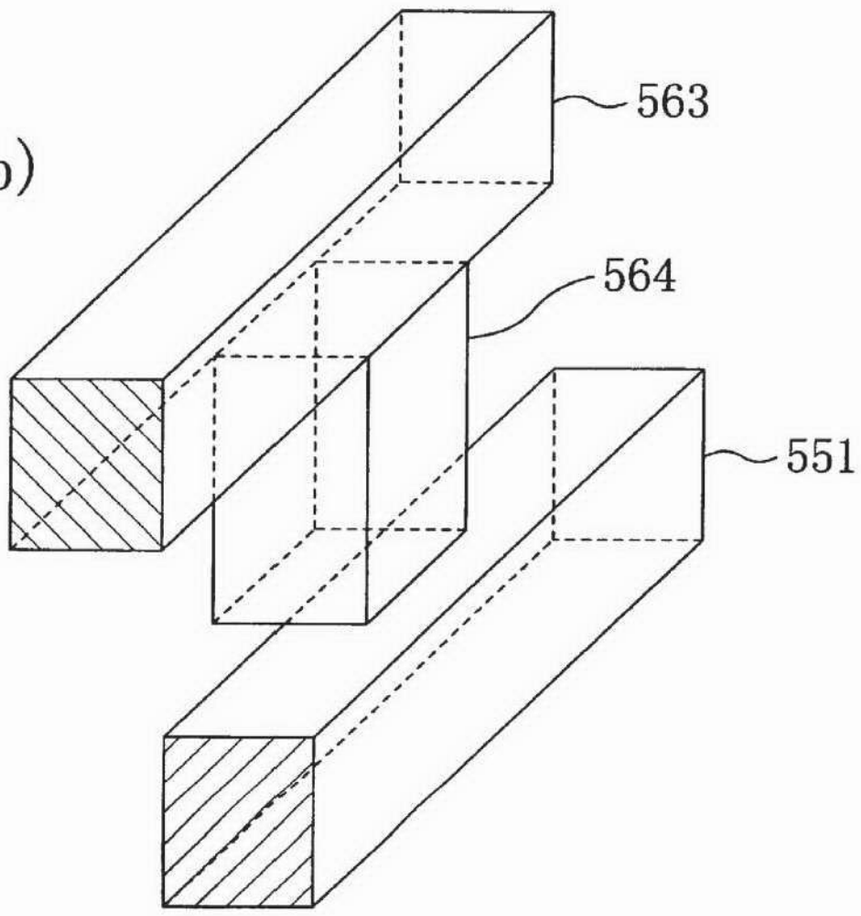


Fig. 30(a)

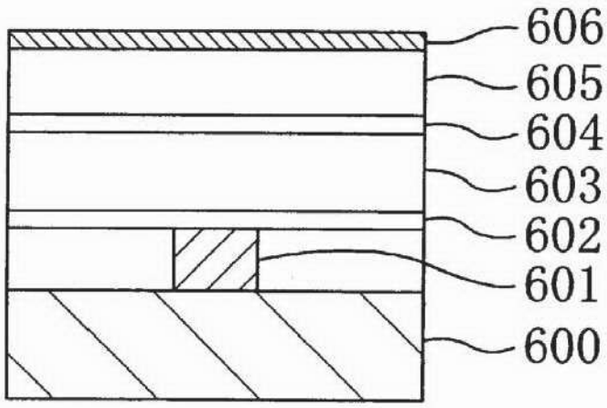


Fig. 30(b)

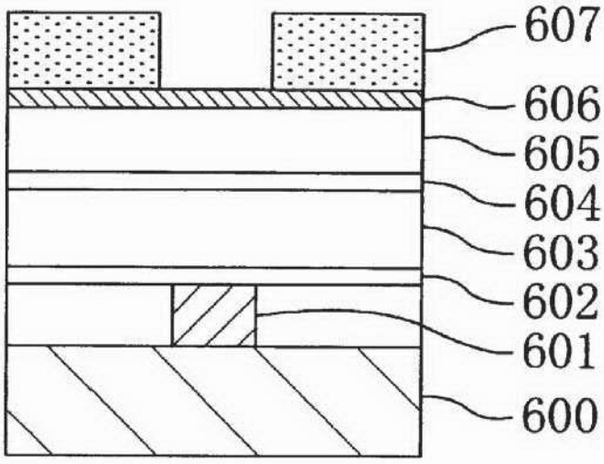


Fig. 30(c)

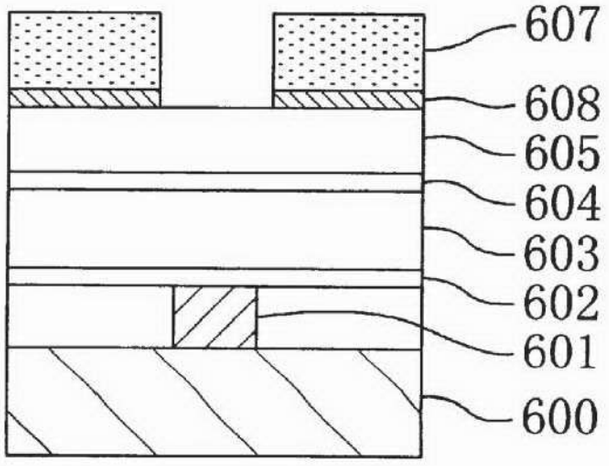


Fig. 31(a)

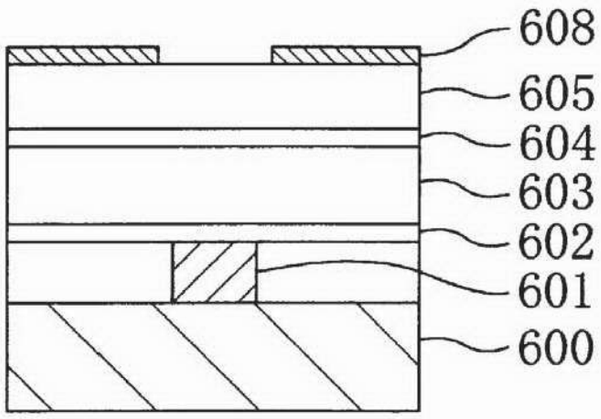


Fig. 31(b)

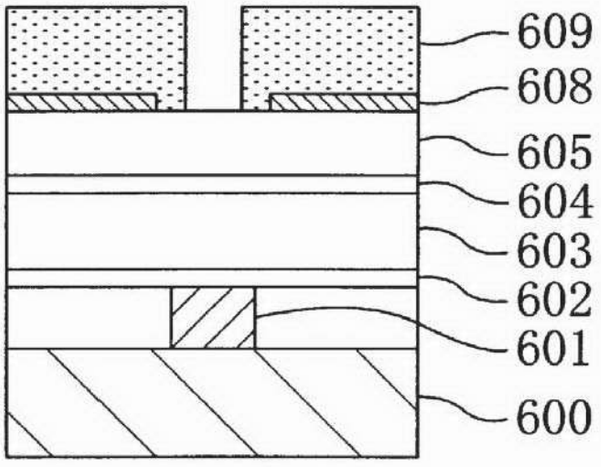


Fig. 31(c)

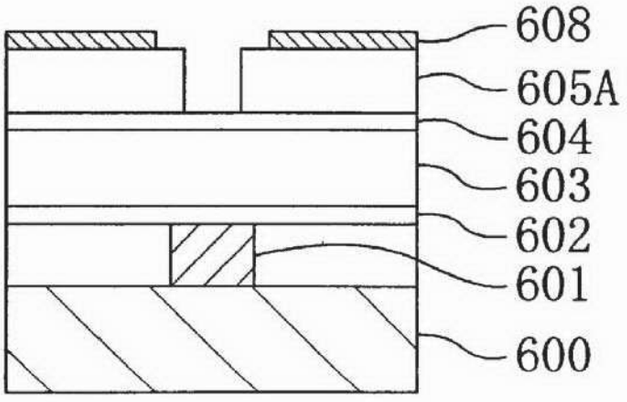


Fig. 32(a)

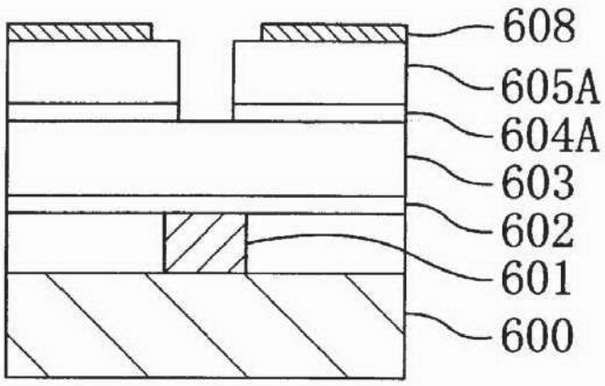


Fig. 32(b)

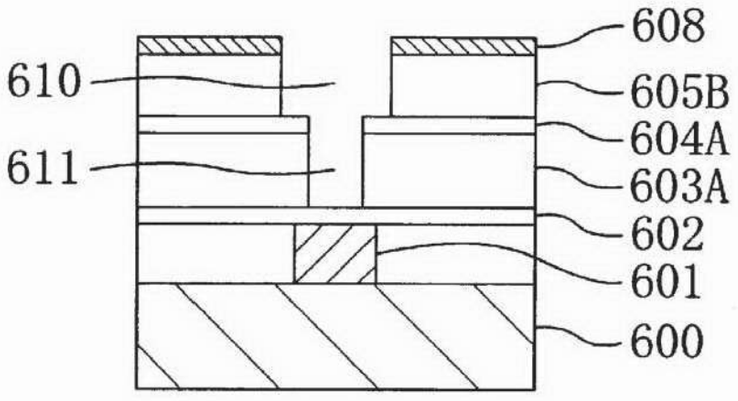


Fig. 32(c)

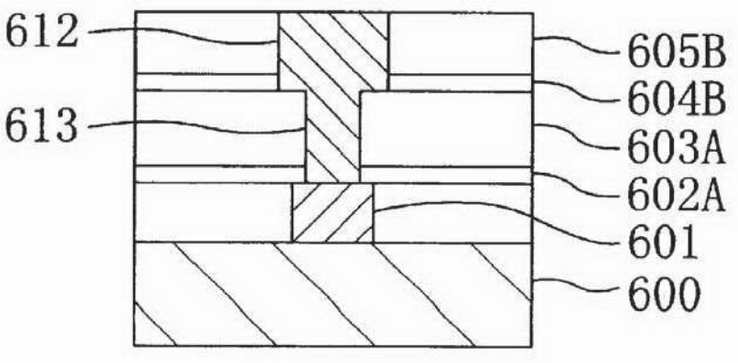


Fig. 33(a)

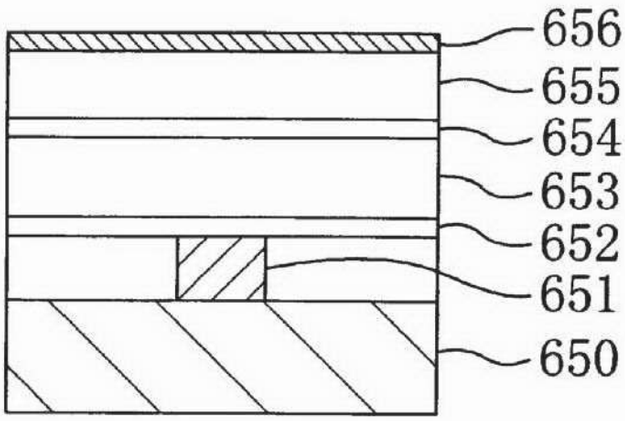


Fig. 33(b)

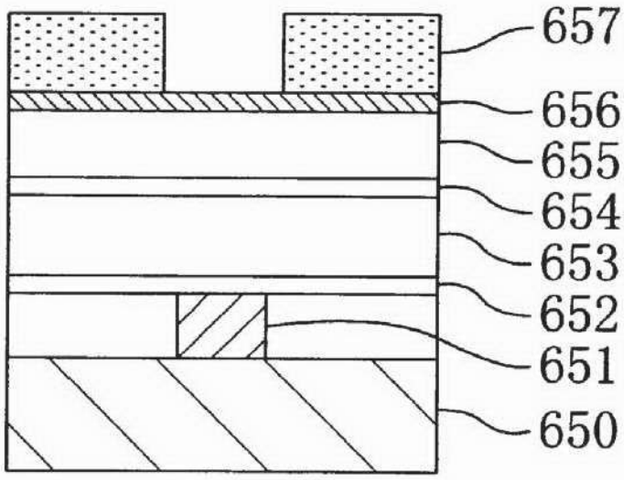


Fig. 33(c)

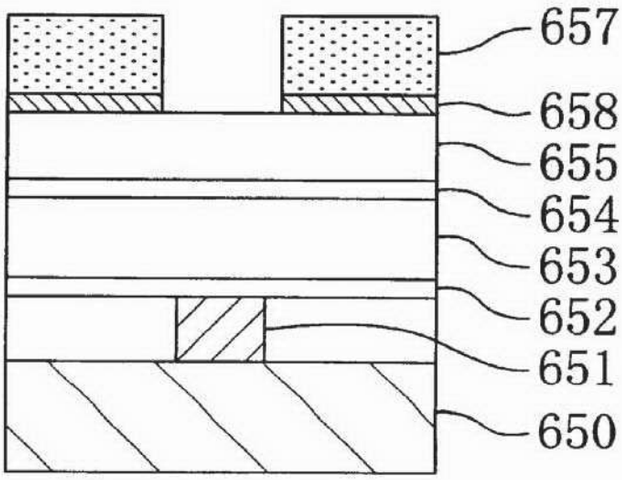


Fig. 34(a)

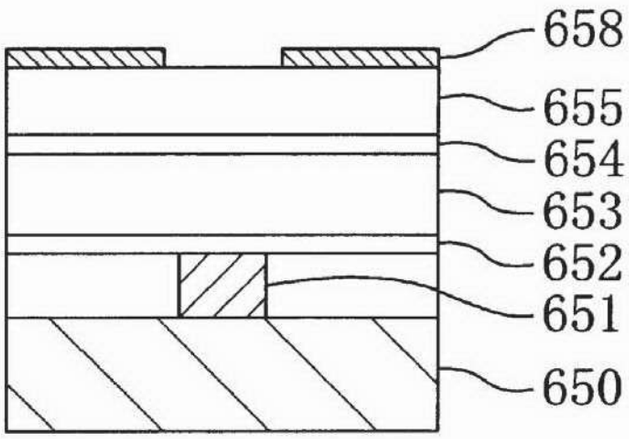


Fig. 34(b)

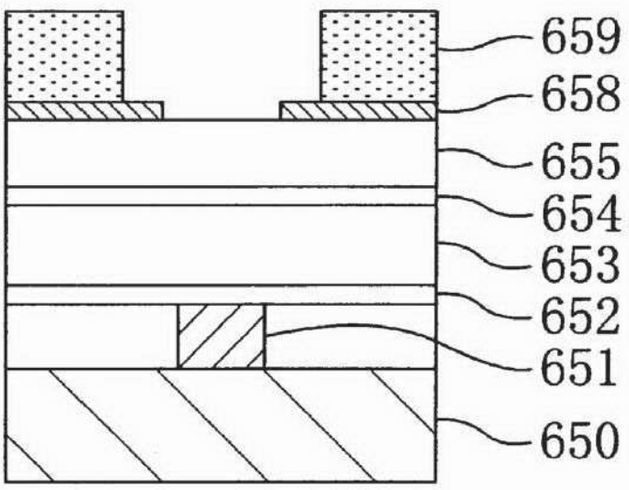


Fig. 34(c)

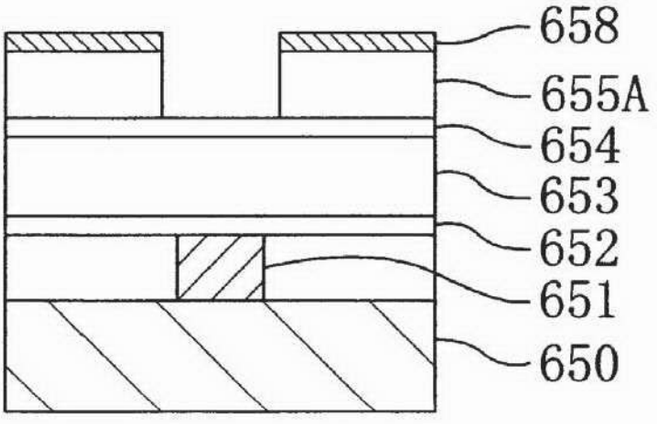


Fig. 35(a)

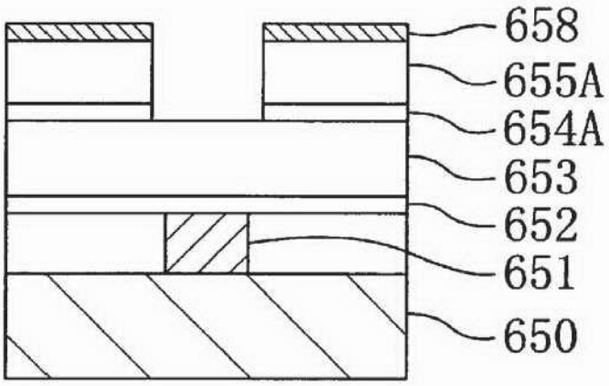


Fig. 35(b)

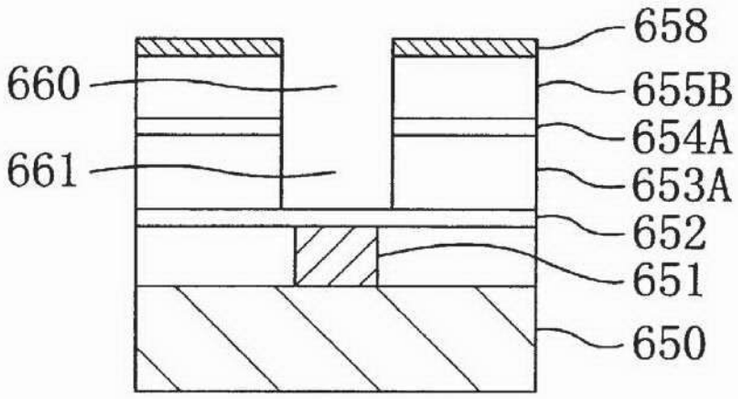


Fig. 35(c)

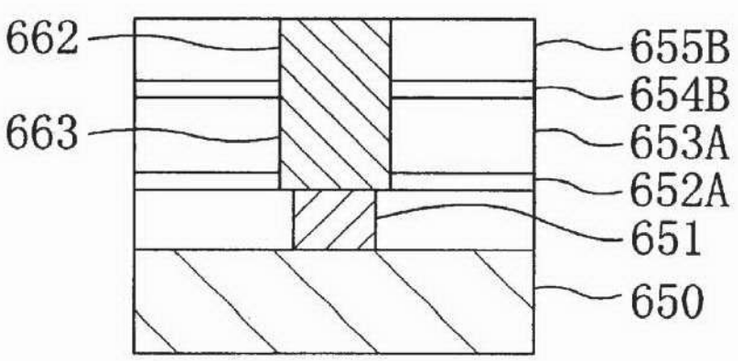


Fig. 36

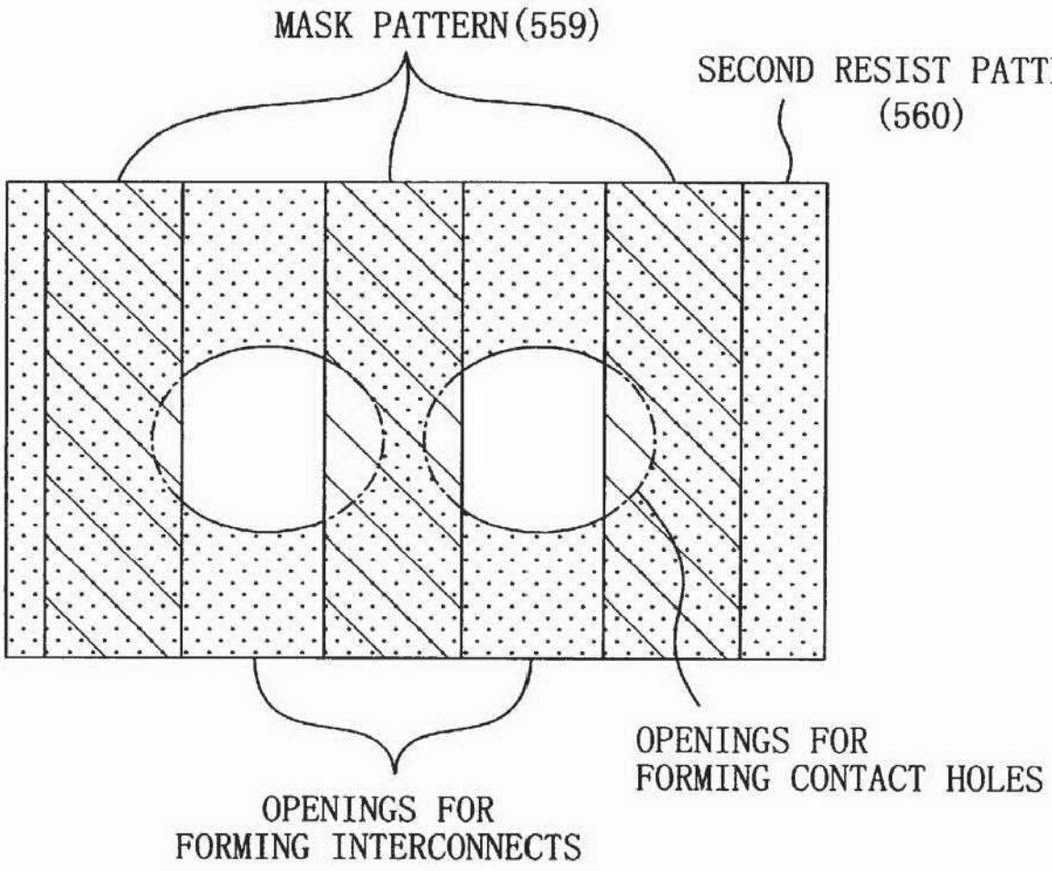

MASK PATTERN(559)
SECOND RESIST PATTERN (560)
OPENINGS FOR FORMING CONTACT HOLES
OPENINGS FOR FORMING INTERCONNECTS

Fig. 37(a)

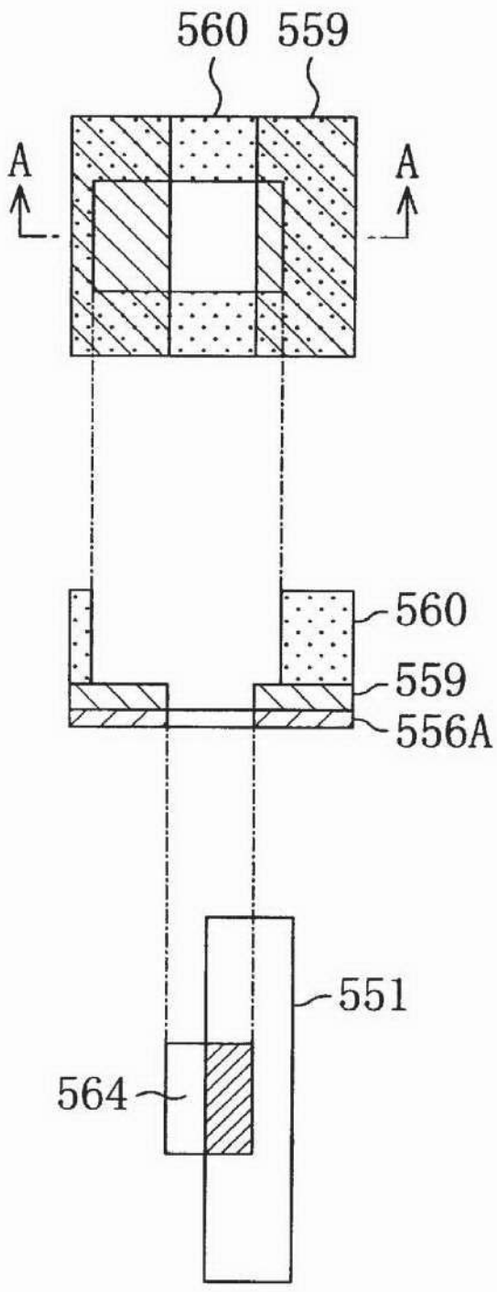
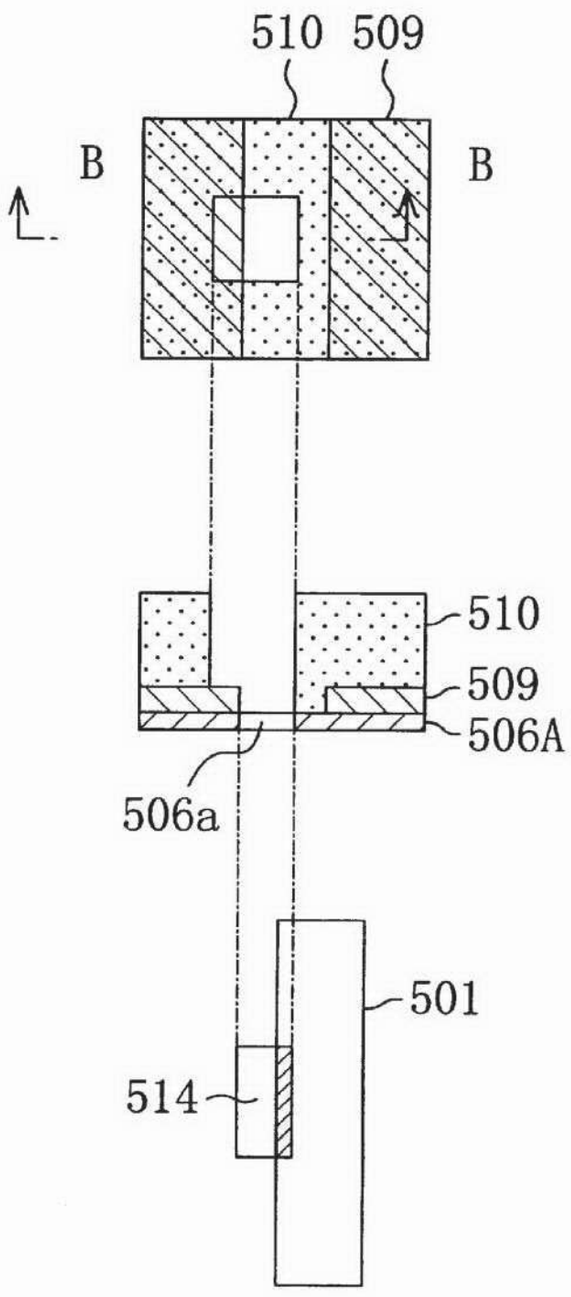


Fig. 37(b)



METHOD FOR FORMING INTERCONNECTION STRUCTURE

BACKGROUND OF THE INVENTION

The present invention relates to a method for forming an interconnection structure in a semiconductor integrated circuit.

As the number of devices, integrated within a single semiconductor integrated circuit, has been tremendously increasing these days, wiring delay has also been increasing noticeably. This is because the larger the number of devices integrated, the larger line-to-line capacitance (i.e., parasitic capacitance between metal interconnects), thus interfering with the performance improvement of a semiconductor integrated circuit. The wiring delay is so-called "RC delay", which is proportional to the product of the resistance of metal interconnection and the line-to-line capacitance.

In other words, to reduce the wiring delay, either the resistance of metal interconnection or the line-to-line capacitance should be reduced.

In order to reduce the interconnection resistance, IBM Corp., Motorola, Inc., etc. have reported semiconductor integrated circuits using copper, not aluminum alloy, as a material for metal interconnects. A copper material has a specific resistance about two-thirds as high as that of an aluminum alloy material. Accordingly, in accordance with simple calculation, the wiring delay involved with the use of a copper material for metal interconnects can be about two-thirds of that involved with the use of an aluminum alloy material therefor. That is to say, the operating speed can be increased by about 1.5 times.

However, the number of devices, integrated within a single semiconductor integrated circuit, is expected to further increase by leaps and bounds from now on, thus increasing the wiring delay considerably. Therefore, it is concerned that even the use of copper as an alternate metal interconnection material would not be able to catch up with such drastic increase. Also, the specific resistance of copper as a metal interconnection material is just a little bit higher than, but almost equal to, that of gold or silver. Accordingly, even if gold or silver is used instead of copper as a metal interconnection material, the wiring delay can be reduced only slightly.

Under these circumstances, not only reducing interconnection resistance but also suppressing line-to-line capacitance play a key role in further increasing the number of devices that can be integrated within a single semiconductor integrated circuit. And the relative dielectric constant of an interlevel insulating film should be reduced to suppress the line-to-line capacitance. A silicon dioxide film has heretofore been used as a typical material for an interlevel insulating film. The relative dielectric constant of a silicon dioxide film is, however, about 4 to about 4.5. Thus, it would be difficult to apply a silicon dioxide film to a semiconductor integrated circuit incorporating an even larger number of devices.

In order to solve such a problem, fluorine-doped silicon dioxide film, low-dielectric-constant spin-on-glass (SOG) film, organic polymer film and so on have been proposed as alternate interlevel insulating films with respective relative dielectric constants smaller than that of a silicon dioxide film.

The relative dielectric constant of a fluorine-doped silicon dioxide film is about 3.3 to about 3.7, which is about 20 percent lower than that of a conventional silicon dioxide film. Nevertheless, a fluorine-doped silicon dioxide film is highly hygroscopic, and easily absorbs water in the air, resulting in various problems in practice. For example, when the fluorine-doped silicon dioxide film absorbs water, SiOH groups, having a high relative dielectric constant, are introduced into the film. As a result, the relative dielectric constant of the fluorine-doped silicon dioxide film adversely increases, or the SiOH groups react with the water during a heat treatment to release H_2O gas. In addition, fluorine free radicals, contained in the fluorine-doped silicon dioxide film, segregate near the surface thereof during a heat treatment and react with Ti, contained in a TiN layer formed thereon as an adhesion layer, to form a TiF film, which easily peels off.

An HSQ (hydrogen silsesquioxane) film, composed of Si, O and H atoms, is an exemplary low-dielectric-constant SOG film. In the HSQ film, the number of the H atoms is about two-thirds of that of the O atoms. However, the HSQ film releases a larger amount of water than a conventional silicon dioxide film. Accordingly, since it is difficult to form a buried interconnection line in the HSQ film, a patterned metal film should be formed as metal interconnects on the HSQ film.

Also, since the HSQ film cannot adhere so strongly to metal interconnects, a CVD oxide film should be formed between the metal interconnects and the HSQ film to improve the adhesion therebetween. However, in such a case, if the CVD oxide film is formed on the metal interconnects, then the substantial line-to-line capacitance is equal to the serial capacitance formed by the HSQ and CVD films. This is because the CVD oxide film with a high dielectric constant exists between the metal interconnects. Accordingly, the resulting line-to-line capacitance is larger as compared with using the HSQ film alone.

An organic polymer film, as well as the low-dielectric-constant SOG film, cannot adhere strongly to metal interconnects, either. Accordingly, a CVD oxide film should be formed as an adhesion layer between the metal interconnects and the organic polymer film, too.

Moreover, an etch rate, at which an organic polymer film is etched, is approximately equal to an ash rate, at which a resist pattern is ashed with oxygen plasma. Accordingly, a usual resist application process is not applicable in such a situation, because the organic polymer film is likely to be damaged during ashing and removing the resist pattern. Therefore, a proposed alternate process includes: forming a CVD oxide film on an organic polymer film; forming a resist film on the CVD oxide film; and then etching the resist film using the CVD oxide film as an etch stopper, or a protective film.

However, during the step of forming the CVD oxide film on the organic polymer film, the surface of the organic polymer film is exposed to a reactive gas containing oxygen. Accordingly, the organic polymer film reacts with oxygen to take in polar groups such as carbonyl groups and ketone groups. As a result, the relative dielectric constant of the organic polymer film disadvantageously increases.

Also, in forming inlaid copper interconnects in the organic polymer film, a TiN adhesion layer, for example, should be formed around wiring grooves formed in the organic polymer film, because the organic polymer film cannot adhere strongly to the metal interconnects. However, since the TiN film has a high resistance, the effective cross-sectional area of the metal interconnects decreases. Consequently, the intended effect attainable by the use of the copper lines, i.e., reduction in resistance, would be lost.

SUMMARY OF THE INVENTION

An object of the present invention is providing a method for forming an interconnection structure in which an insulating film with a low dielectric constant can be formed by an ordinary resist application process.

A first method for forming an interconnection structure according to the present invention includes the steps of: a) forming a first insulating film over lower-level metal interconnects; b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; d) forming a thin film over the third insulating film; e) forming a first resist pattern, having a plurality of openings for forming wiring grooves, on the thin film; f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves; g) forming a second resist pattern, having a plurality of openings for forming contact holes, on the third insulating film; h) dry-etching the third insulating film under such conditions that the third insulating film and the first and second resist patterns are etched at a relatively high rate and that the second insulating film is etched at a relatively low rate, thereby patterning the third insulating film to have the openings for forming contact holes and removing the first and second resist patterns either entirely or partially with respective lower parts thereof left; i) dry-etching the second insulating film using the patterned third insulating film as a mask under such conditions that the second insulating film is etched at a relatively high rate and that the first and third insulating films are etched at a relatively low rate, thereby patterning the second insulating film to have the openings for forming contact holes; j) dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and k) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

In the first method of the present invention, the third insulating film is dry-etched under such conditions that the third insulating film and the first and second resist patterns are etched at a relatively high rate and that the second insulating film is etched at a relatively low rate, thereby patterning the third insulating film and removing the first and second resist patterns in the step h). Accordingly, it is not necessary to perform the step of ashing and removing the first and second resist patterns with oxygen plasma. In other words, since it is possible to prevent the third insulating film from being damaged during ashing and removing a resist pattern, a low-dielectric-constant insulating film, which would otherwise be damaged easily by oxygen plasma, may be used as the third insulating film. As a result, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

In addition, the second insulating film can be used as an etch stopper while the wiring grooves are formed by dry-etching the third insulating film using the mask pattern as a mask in the step j). Accordingly, the depth of each wiring groove can be equalized with the thickness of the third insulating film. That is to say, the depth of the wiring grooves can be defined by self-alignment.

Moreover, the composition of the second insulating film is different from that of the third insulating film. Thus, the second insulating film can be used as an etch stopper while the wiring grooves are formed by dry-etching the third insulating film using the mask pattern as a mask in the step j).

In one embodiment of the present invention, the first method preferably further includes the step of forming a metal adhesion layer over part of the third insulating film exposed inside the wiring grooves and part of the first insulating film exposed inside the contact holes between the steps j) and k).

In such an embodiment, the adhesion between the upper-level metal interconnects and the third insulating film and between the contacts and the first insulating film can be improved.

In another embodiment of the present invention, the third insulating film is preferably mainly composed of an organic component.

In such an embodiment, the conditions employed in the step h), i.e., that the third insulating film and the first and second resist patterns are etched at a relatively high rate and that the second insulating film is etched at a relatively low rate, are realized with much more certainty.

In this embodiment, the step c) preferably includes forming the third insulating film by a CVD process using a reactive gas containing perfluorodecalin.

Then, a film mainly composed of an organic component and having a low relative dielectric constant can be formed as the third insulating film with a lot more certainty.

In another embodiment, the first insulating film is also preferably mainly composed of an organic component.

Then, the conditions employed in the step i), i.e., that the second insulating film is etched at a relatively high rate and that the first and third insulating films are etched at a relatively low rate, are realized with much more certainty. At the same time, the conditions employed in the step j), i.e., that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, are also realized with much more certainty.

In an embodiment where the first and third insulating films are both mainly composed of organic components, the first method preferably further includes the step of forming an adhesion layer over part of the third insulating film exposed inside the wiring grooves and part of the first insulating film exposed inside the contact holes by a plasma process using a reactive gas containing nitrogen between the steps j) and k).

In such a case, the adhesion between the upper-level metal interconnects and the third insulating film mainly composed of an organic component, and between the contacts and the first insulating film mainly composed of an organic component can be improved substantially without fail.

In the embodiment where the first insulating film is mainly composed of an organic component, the step a) preferably includes forming the first insulating film by a CVD process using a reactive gas containing perfluorodecalin.

In such a case, a film mainly composed of an organic component and having a low relative dielectric constant can be formed as the first insulating film with a lot more certainty.

A second method for forming an interconnection structure according to the present invention includes the steps of: a) forming a first insulating film over lower-level metal interconnects; b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; d) forming a thin film over the third insulating film; e) forming a first resist pattern, having a plurality of openings for forming wiring grooves, on the thin film; f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves; g) forming a second resist pattern, having a plurality of openings for forming contact holes, on the third insulating film; h) dry-etching the third insulating film using the first and second resist patterns as a mask under such conditions that the third insulating film is etched at a relatively high rate and that the second insulating film and the first and second resist patterns are etched at a relatively low rate, thereby patterning the third insulating film to have the openings for forming contact holes; i) dry-etching the second insulating film using the first and second resist patterns as a mask under such conditions that the second insulating film is etched at a relatively high rate and that the first and third insulating films and the first and second resist patterns are etched at a relatively low rate, thereby patterning the second insulating film to have the openings for forming contact holes; j) removing the first and second resist patterns; k) dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and l) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

In the second method of the present invention, even if a damaged layer is formed in respective parts of the first and third insulating films that are exposed inside the openings for forming contact holes in the second insulating film during the step j) of removing the first and second resist patterns, the damaged layer can be removed without fail in the next step k). In this step, the third and first insulating films are dry-etched using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively. Accordingly, low-dielectric-constant insulating films, which would otherwise be damaged easily by oxygen plasma, can be used as the first and third insulating films. As a result, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

In one embodiment of the present invention, the third insulating film is preferably a low-dielectric-constant SOG film with a siloxane skeleton.

In such an embodiment, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

A third method for forming an interconnection structure according to the present invention includes the steps of: a) forming a first insulating film over lower-level metal interconnects; b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; d) forming a fourth insulating film, having a different composition than that of the third insulating film, over the third insulating film; e) forming a thin film over the fourth insulating film; f) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves; g) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves; h) removing the first resist pattern and then forming a second resist pattern on the fourth insulating film and the mask pattern, the second resist pattern having openings for forming contact holes; i) dry-etching the fourth insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the fourth insulating film to have the openings for forming contact holes; j) dry-etching the third insulating film using the patterned fourth insulating film as a mask, thereby patterning the third insulating film to have the openings for forming contact holes; k) dry-etching the patterned fourth insulating film and the second insulating film using the mask pattern and the patterned third insulating film as respective masks, thereby forming wiring grooves in the patterned fourth insulating film and patterning the second insulating film to have the openings for forming contact holes; l) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming the wiring grooves and the contact holes in the patterned third insulating film and the first insulating film, respectively; and m) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

In the third method of the present invention, the fourth insulating film exists on the third insulating film during the removal of the first resist pattern in the step h). Accordingly, even if the first resist pattern is removed by oxygen plasma, the third insulating film is not damaged. Also, the second insulating film exists on the first insulating film during dry-etching the third insulating film in the step j). Accordingly, the first insulating film is not damaged, either. Thus, low-dielectric-constant insulating films, which would otherwise be damaged easily by oxygen plasma or dry etching, can be used as the first and third insulating films. As a result, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

In one embodiment of the present invention, at least one of the first and third insulating films is preferably mainly composed of an organic component.

In such an embodiment, the relative dielectric constant of the interlevel insulating film can be reduced.

In another embodiment of the present invention, a size of the openings of the second resist pattern for forming contact holes is preferably larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.

In such an embodiment, even if the openings of the second resist pattern for forming contact holes have misaligned with the openings of the mask pattern for forming wiring grooves, the openings of the patterned fourth insu-

lating film for forming contact holes can be formed to be self-aligned with the openings of the mask pattern for forming wiring grooves. This is because the openings of the patterned fourth insulating film for forming contact holes are formed in respective regions where the openings of the second resist pattern for forming contact holes overlap with corresponding openings of the mask pattern for forming wiring grooves. As a result, the connection between the contacts and the upper-level metal interconnects is ensured.

A fourth method for forming an interconnection structure according to the present invention includes the steps of: a) forming a first insulating film over lower-level metal interconnects; b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; d) forming a thin film over the third insulating film; e) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves; f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves; g) removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes; h) dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes; i) dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes; j) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively; and k) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

In the fourth method of the present invention, the second insulating film exists on the first insulating film during dry-etching the third insulating film in the step h). Accordingly, the first insulating film is not damaged. Thus, low-dielectric-constant insulating films, which would otherwise be damaged easily by oxygen plasma or dry etching, can be used as the first and third insulating films. As a result, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

In one embodiment of the present invention, at least one of the first and third insulating films is preferably mainly composed of an organic component.

In such an embodiment, the relative dielectric constant of the interlevel insulating film can be reduced.

In another embodiment of the present invention, a size of the openings of the second resist pattern for forming contact holes is preferably larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.

In such an embodiment, even if the openings of the second resist pattern for forming contact holes have misaligned with the openings of the mask pattern for forming wiring grooves, the openings of the patterned third insulating film for forming contact holes can be formed to be self-aligned with the openings of the mask pattern for forming wiring grooves. This is because the openings of the patterned third insulating film for forming contact holes are formed in respective regions where the openings of the second resist pattern for forming contact holes overlap with corresponding openings of the mask pattern for forming wiring grooves. As a result, the connection between the contacts and the upper-level metal interconnects is ensured.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**(*a*) through **1**(*c*) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the first embodiment of the present invention.

FIGS. **2**(*a*) through **2**(*c*) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the first embodiment.

FIGS. **3**(*a*) through **3**(*c*) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the first embodiment.

FIGS. **4**(*a*) through **4**(*c*) are cross-sectional views illustrating problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

FIGS. **5**(*a*) through **5**(*c*) are cross-sectional views illustrating the problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

FIGS. **6**(*a*) through **6**(*c*) are cross-sectional views illustrating the problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

FIGS. **7**(*a*) through **7**(*c*) are cross-sectional views illustrating measures to solve the problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

FIGS. **8**(*a*) through **8**(*c*) are cross-sectional views illustrating the measures to solve the problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

FIGS. **9**(*a*) through **9**(*c*) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the second embodiment of the present invention.

FIGS. **10**(*a*) through **10**(*c*) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the second embodiment.

FIGS. **11**(*a*) through **11**(*c*) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the second embodiment.

FIGS. **12**(*a*) through **12**(*c*) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the third embodiment of the present invention.

FIGS. **13**(*a*) through **13**(*c*) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the third embodiment.

FIGS. **14**(*a*) through **14**(*c*) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the third embodiment.

FIGS. **15**(*a*) through **15**(*c*) are cross-sectional views **25** illustrating respective process steps for forming an interconnection structure according to a modified example of the third embodiment.

FIGS. **16**(*a*) through **16**(*d*) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the modified example of the third embodiment.

FIGS. **17**(*a*) through **17**(*c*) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the modified example of the third embodiment.

FIGS. **18**(*a*) through **18**(*c*) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the fourth embodiment of the present invention.

FIGS. **19**(*a*) through **19**(*c*) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the fourth embodiment.

FIGS. **20**(*a*) through **20**(*c*) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the fourth embodiment.

FIGS. **21**(*a*) through **21**(*c*) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the fifth embodiment of the present invention.

FIGS. **22**(*a*) through **22**(*c*) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the fifth embodiment.

FIGS. **23**(*a*) through **23**(*d*) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the fifth embodiment.

FIGS. **24**(*a*) through **24**(*c*) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to a modified example of the fifth embodiment.

FIGS. **25**(*a*) through **25**(*c*) are cross-sectional views illustrating respective process steps for forming the interconnection structure in the modified example of the fifth embodiment.

FIGS. **26**(*a*) through **26**(*d*) are cross-sectional views illustrating respective process steps for forming the interconnection structure in the modified example of the fifth embodiment.

FIGS. **27**(*a*) and **27**(*b*) are perspective views illustrating respective process steps for forming the interconnection structure in the modified example of the fifth embodiment.

FIGS. **28**(*a*) and **28**(*b*) are perspective views illustrating respective process steps for forming the interconnection structure in the modified example of the fifth embodiment.

FIGS. **29**(*a*) and **29**(*b*) are perspective views illustrating respective process steps for forming the interconnection structure in the modified example of the fifth embodiment.

FIGS. **30**(*a*) through **30**(*c*) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the sixth embodiment of the present invention.

FIGS. **31**(*a*) through **31**(*c*) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the sixth embodiment.

FIGS. **32**(*a*) through **32**(*c*) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the sixth embodiment.

FIGS. **33**(*a*) through **33**(*c*) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to a modified example of the sixth embodiment.

FIGS. **34**(*a*) through **34**(*c*) are cross-sectional views illustrating respective process steps for forming the interconnection structure in the modified example of the sixth embodiment.

FIGS. **35**(*a*) through **35**(*c*) are cross-sectional views illustrating respective process steps for forming the interconnection structure in the modified example of the sixth embodiment.

FIG. **36** is a plan view illustrating a positional relationship between the openings of a mask pattern for forming wiring grooves and the openings of a second resist pattern for forming contact holes in the modified example of the fifth embodiment.

FIG. **37**(*a*) illustrates respective positional relationships between the mask pattern and the second resist pattern and between a first metal interconnect and an associated contact in the modified example of the fifth embodiment; and

FIG. **37**(*b*) illustrates respective positional relationships between the mask pattern and the second resist pattern and between a first metal interconnect and an associated contact in the fifth embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

EMBODIMENT 1

Hereinafter, an exemplary method for forming an interconnection structure according to the first embodiment of the present invention will be described with reference to FIGS. **1**(*a*) through **1**(*c*), FIGS. **2**(*a*) through **2**(*c*) and FIGS. **3**(*a*) through **3**(*c*).

First, as shown in FIG. **1**(*a*), a silicon nitride film **102** is formed over first metal interconnects **101** formed on a semiconductor substrate **100**. The silicon nitride film **102** is formed to be 50 nm thick, for example, and used to protect the first metal interconnects **101** during a subsequent etching process step. Thereafter, a first organic film **103** (first in **25** sulating film), mainly composed of an organic component, is formed to be 1 μm thick, for example, on the silicon nitride film **102**. Next, an organic-containing silicon dioxide film **104** (second insulating film), containing an organic component in silicon dioxide, is formed to be 50 nm thick, for example, on the first organic film **103**. Then, a second organic film **105** (third insulating film), mainly composed of an organic component, is formed to be 400 nm thick, for example, on the organic-containing silicon dioxide film **104**. And a titanium nitride film **106** is formed to be 50 nm thick, for example, on the second organic film **105**.

The first and second organic films **103** and **105** may be deposited by any arbitrary technique. For example, these films **103** and **105** may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic films **103** and **105**.

Moreover, the first organic film **103** may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin and organic silane such as hexamethyl disiloxane, arylalkoxy silane or alkylalkoxy silane. In such a case, an organic/inorganic hybrid film can be obtained.

Similarly, the organic-containing silicon dioxide film **104** may also be deposited by any arbitrary technique. For instance, the film **104** may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. In such a case, an organic-containing silicon dioxide film **104**, having a structure in which a phenyl group bonded to a silicon atom is introduced into silicon dioxide, can be obtained.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films **103** and **105** and the organic-containing silicon dioxide film **104**, i.e., a film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **106**.

Next, as shown in FIG. **1**(*b*), a first resist pattern **107**, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film **106**. Thereafter, the titanium nitride film **106** is dry-etched using the first resist pattern **107** as a mask, thereby forming a mask pattern **108** out of the titanium nitride film **106** as shown in FIG. **1**(*c*).

Subsequently, a second resist pattern **109**, having openings for forming contact holes, is formed by lithography on the second organic film **105** without removing the first resist pattern **107**. Then, the second organic film **105** is dry-etched, thereby forming a patterned second organic film **105**A having the openings for forming contact holes as shown in FIG. **2**(*a*). In this case, since the second organic film **105** and the first and second resist patterns **107** and **109** are all mainly composed of organic components, the second organic film **105** is etched at a substantially equal rate to that of the first and second resist patterns **107** and **109**. Thus, when the second organic film **105** is dry-etched, the first and second resist patterns **107** and **109** are also removed simultaneously.

It should be noted that part of the second resist pattern **109** may be left in the process step of dry-etching the second organic film **105**. This is because the residual second resist pattern **109** can be removed during a subsequent process step of forming wiring grooves **111** in the patterned second organic film **105**A (see FIG. **2**(*c*)).

Then, the organic-containing silicon dioxide film **104** is dry-etched using the patterned second organic film **105**A as a mask, thereby forming a patterned organic-containing silicon dioxide film **104**A having the openings for forming contact holes as shown in FIG. **2**(*b*). In this process step, by selecting such etching conditions that the organic-containing silicon dioxide film **104** is etched at a rate higher than that of the patterned second organic film **105**A, it is possible to prevent the patterned second organic film **105**A from being erroneously etched.

Next, the patterned second organic film **105**A is dry-etched using the mask pattern **108** as a mask, thereby forming the wiring grooves **111** in the patterned second organic film **105**A as shown in FIG. **2**(*c*). At the same time, the first organic film **103** is also dry-etched using the patterned organic-containing silicon dioxide film **104**A as a mask, thereby forming a patterned first organic film **103**A having the contact holes as shown in FIG. **2**(*c*).

Subsequently, the silicon nitride film **102** is dry-etched using the patterned organic-containing silicon dioxide film **104**A as a mask, thereby forming a patterned silicon nitride film **102**A and exposing the first metal interconnects **101** within the contact holes **110** as shown in FIG. **3**(*a*).

Then, as shown in FIG. **3**(*b*), an adhesion layer **112**, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **110** and the wiring grooves **111**. Thereafter, a metal film **113** is deposited over the entire surface of the substrate to completely fill in the contact holes **110** and the wiring grooves **111**. In this embodiment, the metal film **113** may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film **113** may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in FIG. **3**(*c*), respective portions of the adhesion layer **112**, the metal film **113** and the mask pattern **108**, which are deposited on the patterned second organic film **105**A, are removed by a CMP technique, for example. As a result, second metal interconnects **114** and contacts **115**, connecting the first and second metal interconnects **101** and **114**, are formed out of the metal film **113**.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **114** through the same process steps as those described above.

In the first embodiment, the organic-containing silicon dioxide film **104** is formed by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. Accordingly, the film **104** has a structure in which a phenyl group (i.e., an exemplary organic group), bonded to a silicon atom, is introduced into silicon dioxide. Thus, the film **104** can be processed as well as a conventional CVD oxide film, and the relative dielectric constant of the film **104** is as low as that of the conventional CVD oxide film. In addition, the film **104** can adhere strongly to organic film, oxide film and metal film.

After the mask pattern **108** has been formed out of the titanium nitride film **106**, the second resist pattern **109** is formed without removing the first resist pattern **107**, and the first and second resist patterns **107** and **109** are removed while the second organic film **105** is dry-etched. Thus, it is no longer necessary to ash and remove the first and second resist patterns **107** and **109** with oxygen plasma. That is to say, it is possible to prevent the second organic film **105** from being damaged during the step of ashing and removing a resist pattern. Accordingly, although the second organic film **105** with a low relative dielectric constant is used as an interlevel insulating film, an ordinary resist application process is applicable to this embodiment.

Moreover, the wiring grooves **111** are formed by dry-etching the patterned second organic film **105**A using the mask pattern **108** as a mask and using the patterned organic-containing silicon dioxide film **104**A as an etch stopper. Accordingly, the depth of the wiring grooves **111** matches with the thickness of the second organic film **105**. That is to say, the depth of the wiring grooves **111** can be defined by self-alignment.

Hereinafter, problems caused by the misalignment of the second resist pattern **109** with the first resist pattern **107** and the measured taken to solve the problems will be described.

First, it will be described with reference to FIGS. **4**(*a*) through **4**(*c*), FIGS. **5**(*a*) through **5**(*c*) and FIGS. **6**(*a*) through **6**(*c*) what problems are caused if the second resist pattern **109** has misaligned.

As in the first embodiment, a silicon nitride film **102** is first formed to be 50 nm thick, for example, over first metal interconnects **101** formed on a semiconductor substrate **100** as shown in FIG. **4**(*a*). Thereafter, a first organic film **103**, mainly composed of an organic component, is formed to be 1 μm thick, for example, on the silicon nitride film **102**.

Next, an organic-containing silicon dioxide film **104**, containing an organic component in silicon dioxide, is formed to be 50 nm thick, for example, on the first organic film **103**. Then, a second organic film **105**, mainly composed of an organic component, is formed to be 400 nm thick, for example, on the organic-containing silicon dioxide film **104**. And a titanium nitride film **106** is formed to be 50 nm thick, for example, on the second organic film **105**.

Next, as shown in FIG. **4**(*b*), a first resist pattern **107**, having openings for forming wiring grooves, is formed on

the titanium nitride film **106**. Thereafter, the titanium nitride film **106** is dry-etched using the first resist pattern **107** as a mask, thereby forming a mask pattern **108** out of the titanium nitride film **106** as shown in FIG. **4**(*c*).

Subsequently, a second resist pattern **109**, having openings for forming contact holes, is formed on the second organic film **105** without removing the first resist pattern **107**. As can be seen if FIGS. **5**(*a*) and **1**(*c*) are compared with each other, the second resist pattern **109** has misaligned with the first resist pattern **107** in this case.

Then, the second organic film **105** is dry-etched, thereby forming a patterned second organic film **105**A having the openings for forming contact holes as shown in FIG. **5**(*a*). As in the first embodiment, since the second organic film **105** and the first and second resist patterns **107** and **109** are all mainly composed of organic components, the first and second resist patterns **107** and **109** are removed simultaneously with the dry-etching of the second organic film **105**. In this case, since the second resist pattern **109** has misaligned with the first resist pattern **107**, the diameter of the openings for forming contact holes, which are provided in the second organic film **105**A, is smaller than desired.

Then, the organic-containing silicon dioxide film **104** is dry-etched using the patterned second organic film **105**A as a mask, thereby forming a patterned organic-containing silicon dioxide film **104**A having the openings for forming contact holes as shown in FIG. **5**(*c*).

Next, the patterned second organic film **105**A is dry-etched using the mask pattern **108** as a mask, thereby forming the wiring grooves **111** in the patterned second organic film **105**A as shown in FIG. **6**(*a*). At the same time, the first organic film **103** is also dry-etched using the patterned organic-containing silicon dioxide film **104**A as a mask, thereby forming a patterned first organic film **103**A having the contact holes **110** as shown in FIG. **6**(*a*). Subsequently, the silicon nitride film **102** is dry-etched using the patterned organic-containing silicon dioxide film **104**A as a mask, thereby forming a patterned silicon nitride film **102**A and exposing the first metal interconnects **101** within the contact holes **110** as shown in FIG. **6**(*b*).

Then, an adhesion layer **112**, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **110** and the wiring grooves **111**. Thereafter, a metal film is deposited over the entire surface of the substrate and respective portions of the adhesion layer **112**, the metal film and the mask pattern **108**, which are deposited on the patterned second organic film lO5A, are removed by a CMP technique, for example. As a result, second metal interconnects **114** are certainly formed. However, since the diameter of the contact holes **110** is smaller than desired, the contact holes **110** cannot be completely filled in with the metal film, and the first and second metal interconnects **101** and **112** cannot be connected to each other, resulting in a contact failure.

Next, it will be described with reference to FIGS. **7**(*a*) through **7**(*c*) and FIGS. **8**(*a*) through **8**(*c*) what measures should be taken to solve the problems caused by the misalignment of the second resist pattern **109**.

First, a second resist pattern **109**, having openings for forming contact holes, is formed through the same process steps as those described with reference to FIGS. **4**(*a*) through **4**(*c*) and FIG. **5**(*a*). In this case, the second resist pattern **109** has also misaligned with the first resist pattern **107** (see FIG. **5**(*a*)).

Thus, as shown in FIG. **7**(*a*), the first resist pattern **107** and the mask pattern **108** are dry-etched using the second resist pattern **109** as a mask. In this manner, portions of the first resist pattern **107**, not overlapping with the second resist pattern **109**, are removed and each opening of the mask pattern **108** is expanded to be equal to or larger than each opening for forming wiring grooves or each opening for forming contact holes. As a result, the pattern for the openings of the second resist pattern for forming contact holes **109** can be transferred to the first resist pattern **107** and the mask pattern **108**.

Then, the second organic film **105** is dry-etched, thereby forming a patterned second organic film **105**A having the openings for forming contact holes as shown in FIG. **7**(*b*). In this case, since the second organic film **105** and the first and second resist patterns **107** and **109** are all mainly composed of organic components, the first and second resist patterns **107** and **109** are removed simultaneously with the dry-etching of the second organic film **105**.

Then, the organic-containing silicon dioxide film **104** is dry-etched using the patterned second organic film **105**A as a mask, thereby forming a patterned organic-containing silicon dioxide film **104**A having the openings for forming contact holes as shown in FIG. **7**(*c*).

As described above, the second resist pattern **109** has misaligned with the first resist pattern **107**. However, in this case, the pattern for the openings of the second resist pattern for forming contact holes **109** has been successfully transferred to the first resist pattern **107** and the mask pattern **108**. Thus, the diameter of the openings for forming contact holes, which have been formed in the patterned second organic film **105**A and the patterned organic-containing silicon dioxide film **104**A, is a predetermined size.

Next, the patterned second organic film **105**A is dry-etched using the mask pattern **108** as a mask, thereby forming the wiring grooves **111** in the patterned second organic film **105**A as shown in FIG. **8**(*a*). At the same time, the first organic film **103** is also dry-etched using the patterned organic-containing silicon dioxide film **104**A as a mask, thereby forming a patterned first organic film **103**A having the contact holes **110** as shown in FIG. **8**(*a*). Subsequently, the silicon nitride film **102** is dry-etched using the patterned organic-containing silicon dioxide film **104**A as a mask, thereby forming a patterned silicon nitride film **102**A and exposing the first metal interconnects **101** within the contact holes **110** as shown in FIG. **8**(*b*).

Then, an adhesion layer **112**, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **110** and the wiring grooves **111**. Thereafter, a metal film is deposited over the entire surface of the substrate and respective portions of the adhesion layer **112**, the metal film and the mask pattern **108**, which are deposited on the patterned second organic film **105**A, are removed by a CMP technique, for example. As a result, second metal interconnects **114** and contacts **115** are formed out of the titanium nitride film **112** and the metal film as shown in FIG. **8**(*c*).

EMBODIMENT 2

Next, an exemplary method for forming an interconnection structure according to the second embodiment of the present invention will be described with reference to FIGS. **9**(*a*) through **9**(*c*), FIGS. **10**(*a*) through **10**(*c*) and FIGS. **11**(*a*) through **11**(*c*).

First, as shown in FIG. **9**(*a*), a silicon nitride film **202** is formed to be 50 nm thick, for example, over first metal interconnects **201** formed on a semiconductor substrate **200**. Thereafter, a first organic film **203** (first insulating film),

mainly composed of an organic component, is formed to be 1 μm thick, for example, on the silicon nitride film **202**. Next, an organic-containing silicon dioxide film **204** (second insulating film), containing an organic component in silicon dioxide, is formed to be 50 nm thick, for example, on the first organic film **203**. Then, a second organic film **205** (third insulating film), mainly composed of an organic component, is formed to be 400 nm thick, for example, on the organic-containing silicon dioxide film **204**. And a titanium nitride film **206** is formed to be 50 nm thick, for example, on the second organic film **205**.

The first and second organic films **203** and **205** may be deposited by any arbitrary technique. For example, these films **203** and **205** may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic films **203** and **205**.

Similarly, the organic-containing silicon dioxide film **204** may also be deposited by any arbitrary technique. For instance, the film **204** may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films **203** and **205** and the organic-containing silicon dioxide film **204**, i.e., a film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **206**.

Next, as shown in FIG. **9**(*b*), a first resist pattern **207**, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film **206**. Thereafter, the titanium nitride film **206** is dry-etched using the first resist pattern **207** as a mask, thereby forming a mask pattern **208** out of the titanium nitride film **206** as shown in FIG. **9**(*c*).

Subsequently, a second resist pattern **209**, having openings for forming contact holes, is formed by lithography on the second organic film **205** without removing the first resist pattern **207**. Then, the second organic film **205** is dry-etched, thereby forming a patterned second organic film **205**A having the openings for forming contact holes as shown in FIG. **10**(*a*). In this case, since the second organic film **205** and the first and second resist patterns **207** and **209** are all mainly composed of organic components, the second organic film **205** is etched at a rate substantially equal to that of the first and second resist patterns **207** and **209**. Accordingly, when the second organic film **205** is dry-etched, the first and second resist patterns **207** and **209** are also removed simultaneously.

If the second resist pattern **209** may have been misaligned with the first resist pattern **207**, then the first resist pattern **207** and the mask pattern **208** should be dry-etched using the second resist pattern **209** as a mask. In this manner, parts of the first resist pattern **207**, not overlapping with the second resist pattern **209**, are removed and the openings of the mask pattern **208** are expanded to be equal to or larger than the openings for forming wiring grooves and contact holes as described in the first embodiment.

Then, the organic-containing silicon dioxide film **204** is dry-etched using the patterned second organic film **205**A as a mask, thereby forming a patterned organic-containing silicon dioxide film **204**A having the openings for forming contact holes as shown in FIG. **10**(*b*). Next, the patterned second organic film **205**A is dry-etched using the mask pattern **208** as a mask, thereby forming the wiring grooves **211** in the patterned second organic film **205**A as shown in FIG. **10**(*c*). At the same time, the first organic film **203** is also dry-etched using the patterned organic-containing silicon dioxide film **204**A as a mask, thereby forming a patterned first organic film **203**A having the contact holes **210** as also shown in FIG. **10**(*c*).

Subsequently, the silicon nitride film **202** is dry-etched using the patterned organic-containing silicon dioxide film **204**A as a mask, thereby forming a patterned silicon nitride film **202**A and exposing the first metal interconnects **201** within the contact holes **210** as shown in FIG. **11**(*a*).

Then, the patterned first and second organic films **203**A and **205**A are subjected to plasma processing using ammonium gas. As a result, as shown in FIG. **11**(*b*), an adhesion layer **212**, including amino and amide groups, is deposited on the wall faces of the patterned first organic film **203**A exposed inside the contact holes **210** and on the wall faces of the patterned second organic film **205**A exposed inside the wiring grooves **211**. Thereafter, a metal film **213** is deposited over the entire surface of the substrate to completely fill in the contact holes **210** and the wiring grooves **211**. In this embodiment, the metal film **213** may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film **213** may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in FIG. **11**(*c*), respective portions of the metal film **213** and the mask pattern **208**, which are deposited on the patterned second organic film **205**A, are removed by a CMP technique, for example. As a result, second metal interconnects **214** and contacts **215** are formed out of the metal film **213**.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **214** through the same process steps as those described above.

EMBODIMENT 3

Next, an exemplary method for forming an interconnection structure according to the third embodiment of the present invention will be described with reference to FIGS. **12**(*a*) through **12**(*c*), FIGS. **13**(*a*) through **13**(*c*) and FIGS. **14**(*a*) through **14**(*c*).

First, as shown in FIG. **12**(*a*), a silicon nitride film **302** is formed over first metal interconnects **301** formed on a semiconductor substrate **300**. The silicon nitride film **302** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **301** during a subsequent etching process step. Thereafter, a first organic-containing silicon dioxide film **303** (first insulating film), containing an organic component in silicon dioxide, is formed to be 1 μm thick, for example, on the silicon nitride film **302**. Next, a low-dielectric-constant SOG film **304** (second insulating film), having a siloxane skeleton, is deposited to be 400 nm thick, for example, on the first organic-containing silicon dioxide film **303**. Then, a second organic-containing silicon dioxide film **305** (third insulating film), containing an organic component in silicon dioxide, is formed to be 50 nm thick, for example, on the low-dielectric-constant SOG film **304**. And a titanium nitride film **306** is formed to be 50 nm thick, for example, on the second organic-containing silicon dioxide film **305**.

The first and second organic-containing silicon dioxide films **303** and **305** may be deposited by any arbitrary technique. For example, these films **303** and **305** may be

deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. Also, an HSQ film may be used as the low-dielectric-constant SOG film **304** with a siloxane skeleton.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic-containing silicon dioxide films **303** and **305** and the low-dielectric-constant SOG film **304**, i.e., a film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **306**.

Next, as shown in FIG. **12**(*b*), a first resist pattern **307**, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film **306**. Thereafter, the titanium nitride film **306** is dry-etched using the first resist pattern **307** as a mask, thereby forming a mask pattern **308** out of the titanium nitride film **306** as shown in FIG. **12**(*c*).

Subsequently, as shown in FIG. **13**(*a*), the first resist pattern **307** is removed and then a second resist pattern **309**, having openings for forming contact holes, is formed on the second organic-containing silicon dioxide film **305**. Then, the second organic-containing silicon dioxide film **305**, the low-dielectric-constant SOG film **304** and the first organic-containing silicon dioxide film **303** are sequentially dry-etched using the second resist pattern **309** as a mask. As a result, a patterned second organic-containing silicon dioxide film **305**A, a patterned low-dielectric-constant SOG film **304**A and a patterned first organic-containing silicon dioxide film **303**A having contact holes **310** are formed as shown in FIG. **13**(*b*).

Next, as shown in FIG. **13**(*c*), the second resist pattern **309** is removed and the patterned second organic-containing silicon dioxide film **305**A is dry-etched using the mask pattern **308** as a mask, thereby forming openings for forming wiring grooves in the patterned second organic-containing silicon dioxide film **305**A. Thereafter, the patterned low-dielectric-constant SOG film **304**A is dry-etched using the mask pattern **308** and the patterned second organic-containing silicon dioxide film **305**A having the openings for wiring grooves as a mask, thereby forming the wiring grooves **311**. In forming the wiring grooves **311**, by selecting such etching conditions that the first organic-containing silicon dioxide film **303**A is etched at a rate sufficiently lower than that of the low-dielectric-constant SOG film **304**A, sufficient selectivity can be secured for the patterned first organic-containing silicon dioxide film **303**A. Accordingly, the depth of the wiring grooves **311** can be determined univalently at the sum of the thicknesses of the second organic-containing silicon dioxide film **305** and the low-dielectric-constant SOG film **304**.

If the second resist pattern **309** may have been misaligned with the first resist pattern **307**, the mask pattern **308** should be dry-etched using the second resist pattern **309** as a mask before the second organic-containing silicon dioxide film **305** is dry-etched using the second resist pattern **309** as a mask. That is to say, if the mask pattern **308** is partially exposed inside the openings of the second resist pattern **309** for forming contact holes because of the misalignment of the second resist pattern **309** with the first resist pattern **307**, then the mask pattern **308** is dry-etched using the second resist pattern **309** as a mask. In this manner, the openings of the mask pattern **308** are expanded to include the openings for forming wiring grooves and contact holes.

Subsequently, the silicon nitride film **302** is dry-etched using the patterned first organic-containing silicon dioxide film **303**A as a mask, thereby forming a patterned silicon nitride film **302**A and exposing the first metal interconnects **301** within the contact holes **310** as shown in FIG. **14**(*a*).

Then, as shown in FIG. **14**(*b*), an adhesion layer **312**, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **310** and the wiring grooves **311**. Thereafter, a metal film **313** is deposited over the entire surface of the substrate to completely fill in the contact holes **310** and the wiring grooves **311**. In this embodiment, the metal film **313** may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film **313** may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in FIG. **14**(*c*), respective portions of the adhesion layer **312**, the metal film **313** and the mask pattern **308**, which are deposited on the patterned second organic-containing silicon dioxide film **305**A, are removed by a CMP technique, for example. As a result, second metal interconnects **314** and contacts **315**, connecting the first and second metal interconnects **301** and **314**, are formed out of the metal film **313**.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **314** through the same process steps as those described above.

In the third embodiment, while the first resist pattern **307** is ashed and removed with oxygen plasma, the low-dielectric-constant SOG film **304** is not exposed to the oxygen plasma, because the second organic-containing silicon dioxide film **305** exists on the low-dielectric-constant SOG film **304**.

Also, in this embodiment, after the second organic-containing silicon dioxide film **305**, the low-dielectric-constant SOG film **304** and the first organic-containing silicon dioxide film **303** have been sequentially dry-etched using the second resist pattern **309** as a mask, the second resist pattern **309** is ashed and removed with oxygen plasma. Accordingly, the regions of the patterned low-dielectric-constant SOG film **304**A, which are exposed inside the openings for forming contact holes, are exposed to oxygen plasma and damaged. However, the damaged layer, formed in the patterned low-dielectric-constant SOG film **304**A, can be removed when the wiring grooves **311** are formed in the patterned low-dielectric-constant SOG film **304**A, and does not have harmful effects on subsequent process steps.

Accordingly, the low-dielectric-constant SOG film **304** may be made of a material degradable with oxygen plasma. For example, in general, if an HSQ film is exposed to oxygen plasma, the Si—H bonds thereof are oxidized and the content of water and the relative dielectric constant thereof both increase to deteriorate the reliability and performance of the device. However, according to the third embodiment, the patterned low-dielectric-constant SOG film **304**A, in which the wiring grooves **311** have already been formed, is not affected by oxygen plasma. Thus, even if an HSQ film is used as an interlevel insulating film, the deterioration in reliability and performance of the device can be avoided.

MODIFIED EXAMPLE OF EMBODIMENT 3

Next, an exemplary method for forming an interconnection structure according to a modified example of the third embodiment of the present invention will be described with reference to FIGS. **15**(*a*) through **15**(*c*), FIGS. **16**(*a*) through **16**(*c*) and FIGS. **17**(*a*) through **17**(*c*).

First, as shown in FIG. **15**(*a*), a silicon nitride film **352** is formed over first metal interconnects **351** formed on a

semiconductor substrate **350**. The silicon nitride film **352** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **351** during a subsequent etching process step. Thereafter, a first silicon dioxide film **353** (first insulating film) is formed to be 1 μm thick, for example, on the silicon nitride film **352**. Next, an organic film **354** (second insulating film) is deposited to be 400 nm thick, for example, on the first silicon dioxide film **353**. Then, a second silicon dioxide film **355** (third insulating film) is formed to be 50 nm thick, for example, on the organic film **354**. And a titanium nitride film **356** is formed to be 50 nm thick, for example, on the second silicon dioxide film **355**.

The first and second silicon dioxide films **353** and **355** may be deposited by any arbitrary technique. For example, these films **353** and **355** may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane.

It should be noted that a thin film showing high etch selectivity with respect to the first and second silicon dioxide films **353** and **355** and the organic film **354**, i.e., a film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **356**.

Next, as shown in FIG. **15**(*b*), a first resist pattern **357**, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film **356**. Thereafter, the titanium nitride film **356** is dry-etched using the first resist pattern **357** as a mask, thereby forming a mask pattern **358** out of the titanium nitride film **356** as shown in FIG. **15**(*c*).

Subsequently, as shown in FIG. **16**(*a*), the first resist pattern **357** is removed and then a second resist pattern **359**, having openings for forming contact holes, is formed on the second silicon dioxide film **355**. Then, the second silicon dioxide film **355** and the organic film **354** are sequentially dry-etched using the second resist pattern **359** as a mask, thereby forming a patterned second silicon dioxide film **355**A and a patterned organic film **354**A having openings **360** for forming contact holes as shown in FIG. **16**(*b*). In this case, the second resist pattern **359** is removed during the step of etching the organic film **354**.

Next, as shown in FIG. **16**(*c*), the first silicon dioxide film **353** is dry-etched using the patterned second silicon dioxide film **355**A and the patterned organic film **354**A as a mask, thereby forming a patterned first silicon dioxide film **353**A having contact holes **361**. In this etching process step, the mask pattern **358** is transferred to the patterned second silicon dioxide film **355**A. Accordingly, openings for forming wiring grooves are formed in the patterned second silicon dioxide film **355**A.

Thereafter, as shown in FIG. **16**(*d*), the patterned organic film **354**A is dry-etched using the mask pattern **358** and the patterned second silicon dioxide film **355**A having the openings for forming wiring grooves as a mask, thereby forming the wiring grooves **362**. In forming the wiring grooves **362**, by selecting such etching conditions that the first silicon dioxide film **353**A is etched at a rate sufficiently lower than that of the organic film **354**A, sufficient selectivity can be secured for the patterned first silicon dioxide film **353**A. Accordingly, the depth of the wiring grooves **362** can be determined univalently at the sum of the thicknesses of the second silicon dioxide film **355** and the organic film **354**.

If the second resist pattern **359** may have been misaligned with the first resist pattern **357**, then the mask pattern **358** should be dry-etched using the second resist pattern **359** as a mask before the second silicon dioxide film **355** is dry-etched using the second resist pattern **359** as a mask. That is to say, if the mask pattern **358** is partially exposed inside the openings of the second resist pattern **359** for forming contact holes because of the misalignment of the second resist pattern **359** with the first resist pattern **357**, then the mask pattern **358** is dry-etched using the second resist pattern **359** as a mask. In this manner, the openings of the mask pattern **358** are expanded to include the openings for forming wiring grooves and contact holes.

Subsequently, the silicon nitride film **352** is dry-etched using the patterned first silicon dioxide film **353**A as a mask, thereby forming a patterned silicon nitride film **352**A and exposing the first metal interconnects **351** within the contact holes **361** as shown in FIG. **17**(*a*).

Then, as shown in FIG. **17**(*b*), an adhesion layer **363**, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **361** and the wiring grooves **362**. Thereafter, a metal film **364** is deposited over the entire surface of the substrate to completely fill in the contact holes **361** and the wiring grooves **362**. In this embodiment, the metal film **364** may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film **364** may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in FIG. **17**(*c*), respective portions of the adhesion layer **363**, the metal film **364** and the mask pattern **358**, which are deposited on the patterned second silicon dioxide film **355**A, are removed by a CMP technique, for example. As a result, second metal interconnects **365** and contacts **366**, connecting the first and second metal interconnects **351** and **365**, are formed out of the metal film **364**.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **365** through the same process steps as those described above.

In this modified example of the third embodiment, while the first resist pattern **357** is ashed and removed by oxygen plasma, the organic film **354** is not exposed to the oxygen plasma, because the second silicon dioxide film **355** exists on the organic film **354**.

Also, in this example, the second resist pattern **359** is removed while the second silicon dioxide film **355** and the organic film **354** are dry-etched using the second resist pattern **359** as a mask. Accordingly, since there is no need to ash and remove the second resist pattern **359** with oxygen plasma, the organic film **354** is not exposed to oxygen plasma.

EMBODIMENT 4

Next, an exemplary method for forming an interconnection structure according to the fourth embodiment of the present invention will be described with reference to FIGS. **18**(*a*) through **18**(*c*), FIGS. **19**(*a*) through **19**(*c*) and FIGS. **20**(*a*) through **20**(*c*).

First, as shown in FIG. **18**(*a*), a silicon nitride film **402** is formed over first metal interconnects **401** formed on a semiconductor substrate **400**. The silicon nitride film **402** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **401** during a subsequent etching process step. Thereafter, a first low-dielectric-constant SOG film **403** (first insulating film), having a siloxane skeleton, is formed to be 1 μm thick, for example, on the silicon nitride film **402**. Next, an organic-containing silicon dioxide film **404** (second insulating film), containing an organic component in silicon dioxide, is deposited to be 50 nm thick, for

example, on the first low-dielectric-constant SOG film **403**. Then, a second low-dielectric-constant SOG film **405** (third insulating film), having a siloxane skeleton, is formed to be 400 nm thick, for example, on the organic-containing silicon dioxide film **404**. And a titanium nitride film **406** is formed to be 50 nm thick, for example, on the second low-dielectric-constant SOG film **405**.

The first and second low-dielectric-constant SOG films **403** and **405** may be HSQ films, for example. The organic-containing silicon dioxide film **404** may be deposited by any arbitrary technique. For example, the film **404** may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. Then, an organic-containing silicon dioxide film **404**, having a structure in which a phenyl group bonded to a silicon atom is introduced into silicon dioxide, can be obtained.

It should be noted that a thin film showing high etch selectivity with respect to the first and second low-dielectric-constant SOG films **403** and **405** and the organic-containing silicon dioxide film **404**, i.e., a film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **406**.

Next, as shown in FIG. **18**(*b*), a first resist pattern **407**, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film **406**. Thereafter, the titanium nitride film **406** is dry-etched using the first resist pattern **407** as a mask, thereby forming a mask pattern **408** out of the titanium nitride film **406** as shown in FIG. **18**(*c*).

Subsequently, a second resist pattern **409**, having openings for forming contact holes, is formed by lithography on the second low-dielectric-constant SOG film **405** without removing the first resist pattern **407**. Then, the second low-dielectric-constant SOG film **405** and the organic-containing silicon dioxide film **404** are sequentially dry-etched using the second resist pattern **409** as a mask, thereby forming a patterned second low-dielectric-constant SOG film **405**A and a patterned organic-containing silicon dioxide film **404**A as shown in FIG. **19**(*a*).

Next, the first and second resist patterns **407** and **409** are ashed and removed with oxygen plasma. As a result, a damaged layer **410** is unintentionally formed in respective portions of the patterned second low-dielectric-constant SOG film **405**A and the first low-dielectric-constant SOG film **403**, which are exposed inside the openings for forming contact holes, as shown in FIG. **19**(*b*).

Then, the patterned second low-dielectric-constant SOG film **405**A is dry-etched using the mask pattern **408** as a mask, thereby forming wiring grooves **412** in the patterned second low-dielectric-constant SOG film **405**A as shown in FIG. **19**(*c*). At the same time, the first low-dielectric-constant SOG film **403** is dry-etched using the patterned organic-containing silicon dioxide film **404**A as a mask, thereby forming a patterned first low-dielectric-constant SOG film **403**A having contact holes **411** as shown in FIG. **19**(*c*). By performing this dry-etching process step, the damaged layer **410** can be removed from the patterned second low-dielectric-constant SOG films **405**A and the first low-dielectric-constant SOG film **403**.

Subsequently, the silicon nitride film **402** is dry-etched using the patterned organic-containing silicon dioxide film **404**A as a mask, thereby forming a patterned silicon nitride film **402**A and exposing the first metal interconnects **401** within the contact holes **411** as shown in FIG. **20**(*a*).

Then, as shown in FIG. **20**(*b*), an adhesion layer **413**, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **411** and the wiring grooves **412**. Thereafter, a metal film **414** is deposited over the entire surface of the substrate to completely fill in the contact holes **411** and the wiring grooves **412**. In this embodiment, the metal film **414** may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film **414** may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in FIG. **20**(*c*), respective portions of the adhesion layer **413**, the metal film **414** and the mask pattern **408**, which are deposited on the patterned second low-dielectric-constant SOG film **405**A, are removed by a CMP technique, for example. As a result, second metal interconnects **415** and contacts **416**, connecting the first and second metal interconnects **401** and **415**, are formed out of the metal film **414**.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **415** through the same process steps as those described above.

In the fourth embodiment, while the first and second resist patterns **407** and **409** are ashed and removed with oxygen plasma, a damaged layer **410** is formed in the first low-dielectric-constant SOG film **403** and the patterned second low-dielectric-constant SOG film **405**A. But the damaged layer **410** can be removed while the contact holes **411** and the wiring grooves **412** are formed.

Accordingly, the first and second low-dielectric-constant SOG films **403** and **405** may be made of a material degradable with oxygen plasma. For example, in general, if an HSQ film is exposed to oxygen plasma, Si—H bonds thereof are oxidized and the content of water and the relative dielectric constant thereof both increase to deteriorate the reliability and performance of the device. However, according to the fourth embodiment, the patterned first low-dielectric-constant SOG film **403**A, in which the contact holes **411** have already been formed, and the patterned second low-dielectric-constant SOG film **405**A, in which the wiring grooves **412** have already been formed, are not affected by oxygen plasma any more. Thus, even if an HSQ film is used as an interlevel insulating film, the deterioration in reliability and performance of the device can be avoided.

EMBODIMENT 5

Next, an exemplary method for forming an interconnection structure according to the fifth embodiment of the present invention will be described with reference to FIGS. **21**(*a*) through **21**(*c*), FIGS. **22**(*a*) through **22**(*c*) and FIGS. **23**(*a*) through **23**(*d*).

First, as shown in FIG. **21**(*a*), a silicon nitride film **502** is formed over first metal interconnects **501** formed on a semiconductor substrate **500**. The silicon nitride film **502** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **501** during a subsequent etching process step. Thereafter, a first organic film **503** (first insulating film), mainly composed of an organic component, is deposited to be 400 nm thick, for example, on the silicon nitride film **502**. Then, a first silicon dioxide film **504** (second insulating film) is deposited to be 100 nm thick, for example, on the first organic film **503**. Subsequently, a second organic film **505** (third insulating film), mainly composed of an organic component, is deposited to be 300 nm thick, for example, on the first silicon dioxide film **504**. Next, a second silicon dioxide film **506** (fourth insulating film) is deposited to be 200 nm thick, for example, on the

second organic film **505**. And a titanium nitride film **507** (thin film) is deposited to be 50 nm thick, for example, on the second silicon dioxide film **506**.

The first and second organic films **503** and **505** may be deposited by any arbitrary technique. For example, these films **503** and **505** may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic films **503** and **505**. More specifically, the organic films **503** and **505** may be made of polytetrafluoroethylene, oxygen-containing polytetrafluoroethylene, polyimide fluoride or polyaryl ether.

The first and second silicon dioxide films **504** and **506** may also be deposited by any arbitrary technique. For example, these films **504** and **506** may be deposited by a plasma CVD process.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films **503** and **505** and the first and second silicon dioxide films **504** and **506**, i.e., a thin film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **507**.

Next, as shown in FIG. **21**(*b*), a first resist pattern **508**, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film **507**. Thereafter, the titanium nitride film **507** is dry-etched using the first resist pattern **508** as a mask, thereby forming a mask pattern **509**, having openings for forming wiring grooves, out of the titanium nitride film **507** as shown in FIG. **21**(*c*).

Subsequently, as shown in FIG. **22**(*a*), the first resist pattern **508** is removed by oxygen plasma, for example. In this case, even if the first resist pattern **508** is ashed and removed using oxygen plasma, the quality of the second organic film **505** does not degrade, because the second silicon dioxide film **506** exists on the second organic film **505** mainly composed of an organic component.

Then, as shown in FIG. **22**(*b*), a second resist pattern **510**, having openings for forming contact holes, is formed by lithography on the mask pattern **509**. Thereafter, the second silicon dioxide film **506** is dry-etched using the second resist pattern **510** and the mask pattern **509** as a mask, thereby forming a patterned second silicon dioxide film **506**A having openings for forming contact holes as shown in FIG. **22**(*c*).

Next, the second organic film **505** is dry-etched using the patterned second silicon dioxide film **506**A as a mask, thereby forming a patterned second organic film **505**A having openings for forming contact holes as shown in FIG. **23**(*a*). In this case, the second organic film **505** and the second resist pattern **510** are both mainly composed of organic components, the second organic film **505** is etched at a substantially equal rate to that of the second resist pattern **510**. Thus, when the second organic film **505** is dry-etched, the second resist pattern **510** is also removed simultaneously. The patterned second silicon dioxide film **506**A functions as an etch stopper during dry-etching the second resist pattern **510**.

It should be noted that part of the second resist pattern **510** may be left in the process step of dry-etching the second organic film **505**. This is because the residual second resist pattern **510** can be removed during a subsequent process step of dry-etching the first organic film **503** (see FIG. **23**(*c*)).

Thereafter, the patterned second silicon dioxide film **506**A and the first silicon dioxide film **504** are dry-etched using the mask pattern **509** and the patterned second organic film **505**A as respective masks, thereby forming a patterned second silicon dioxide film **506**B having openings for forming wiring grooves and a patterned first silicon dioxide film **504**A having openings for forming contact holes as shown in FIG. **23**(*b*).

Then, the patterned second organic film **505**A and the first organic film **503** are dry-etched using the mask pattern **509** and the patterned first silicon dioxide film **504**A as respective masks, thereby forming a patterned second organic film **505**B having wiring grooves **511** and a patterned first organic film **503**A having contact holes **512** as shown in FIG. **23**(*c*).

Subsequently, the silicon nitride film **502** is dry-etched using the patterned first silicon dioxide film **504**A as a mask, thereby forming a patterned silicon nitride film **502**A (see FIG. **23**(*d*)) and exposing the first metal interconnects **501** within the contact holes **512**. Then, although not shown, an adhesion layer, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **512** and the wiring grooves **511** as in the first embodiment. Thereafter, a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes **512** and the wiring grooves **511**. In this embodiment, the metal film may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed. Finally, respective portions of the adhesion layer, the metal film and the mask pattern **509**, which are deposited on the patterned second silicon dioxide film **506**B, are removed by a CMP technique, for example. As a result, second metal interconnects **513** and contacts **514**, connecting the first and second metal interconnects **501** and **513** together, are formed as shown in FIG. **23**(*d*).

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **513** through the same process steps as those described above.

In the fifth embodiment, while the first resist pattern **508** is being removed by oxygen plasma, for example, the quality of the second organic film **505** does not degrade. This is because the second silicon dioxide film **506** exists on the second organic film **505**, which is likely to be damaged by oxygen plasma.

Also, in this embodiment, the first silicon dioxide film **504** functions as an etch stopper during dry-etching the second organic film **505**. Accordingly, it is possible to prevent the quality of the first organic film **503** from being degraded.

MODIFIED EXAMPLE OF EMBODIMENT 5

Next, a method for forming an interconnection structure according to a modified example of the fifth embodiment will be described with reference to FIGS. **24**(*a*) through **24**(*c*), FIGS. **25**(*a*) through **25**(*c*), FIGS. **26**(*a*) through **26**(*d*), FIGS. **27**(*a*) and **27**(*b*), FIGS. **28**(*a*) and **28**(*b*) and FIGS. **29**(*a*) and **29**(*b*).

First, as shown in FIG. **24**(*a*), a silicon nitride film **552** is formed over first metal interconnects **551** formed on a semiconductor substrate **550**. The silicon nitride film **552** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **551** during a subsequent etching process step. Thereafter, a first organic film **553** (first insulating film), mainly composed of an organic component, is deposited to be 400 nm thick, for example, on the silicon

nitride film **552**. Then, a first silicon dioxide film **554** (second insulating film) is formed to be 100 nm thick, for example, on the first organic film **553**. Subsequently, a second organic film **555** (third insulating film), mainly composed of an organic component, is deposited to be 300 nm thick, for example, on the first silicon dioxide film **554**. Next, a second silicon dioxide film **556** (fourth insulating film) is deposited to be 200 nm thick, for example, on the second organic film **555**. And a titanium nitride film **557** is deposited to be 50 nm thick, for example, on the second silicon dioxide film **556**.

The first and second organic films **553** and **555** and the first and second silicon dioxide films **554** and **566** may be deposited by any arbitrary technique as in the fifth embodiment. Also, a thin film showing high etch selectivity with respect to the first and second organic films **553** and **555** and the first and second silicon dioxide films **554** and **556** may be used instead of the titanium nitride film **557**.

Next, as shown in FIG. **24**(*b*), a first resist pattern **558**, having openings for forming wiring grooves, is formed on the titanium nitride film **557**. Thereafter, the titanium nitride film **557** is dry-etched using the first resist pattern **558** as a mask, thereby forming a mask pattern **559**, having openings for forming wiring grooves, out of the titanium nitride film **557** as shown in FIG. **24**(*c*).

Subsequently, as shown in FIGS. **25**(*a*) and **27**(*a*), the first resist pattern **558** is removed. Then, a second resist pattern **560**, having openings for forming contact holes, is formed on the mask pattern **559** as shown in FIG. **25**(*b*). in this modified example of the fifth embodiment, the sizes of the openings of the second resist pattern **560** for forming contact holes are set larger than designed sizes of the contact holes in respective directions vertical and parallel to wiring grooves for forming second metal interconnects. The reason thereof will be described later.

Then, the second silicon dioxide film **556** is dry-etched using the second resist pattern **560** and the mask pattern **559** as a mask, thereby forming a patterned second silicon dioxide film **556**A having openings for forming contact holes as shown in FIGS. **25**(*c*) and **27**(*b*).

As described above, the sizes of the openings of the second resist pattern **560** for forming contact holes are set larger than designed sizes of the contact holes in respective directions vertical and parallel to wiring grooves for forming second metal interconnects. Accordingly, even if the openings of the second resist pattern **560** for forming contact holes have misaligned with the openings of the mask pattern **559** for forming wiring grooves, the openings of the patterned second silicon dioxide film **556**A for forming contact holes can be formed to be self-aligned with the openings of the mask pattern **559** for forming wiring grooves. This is because the openings of the patterned second silicon dioxide film **556**A for forming contact holes are formed in respective regions where the openings of the second resist pattern **560** for forming contact holes overlap with corresponding openings of the mask pattern **559** for forming wiring grooves.

In addition, the size of the openings of the second resist pattern **560** for forming contact holes is also extended in the direction parallel to the wiring grooves for forming second metal interconnects. Thus, the contact area between contacts **564** to be formed later and second metal interconnects **563** (see FIG. **26**(*d*)) expands. As a result, the contacts **564** can connect the first and second metal interconnects **551** and **563** together with a lot more certainty.

Next, the second organic film **555** is dry-etched using the patterned second silicon dioxide film **556**A as a mask, thereby forming a patterned second organic film **555**A having openings for forming contact holes as shown in FIGS. **26**(*a*) and **28**(*a*). In this case, the second organic film **555** and the second resist pattern **560** are both mainly composed of organic components, the second organic film **555** is etched at a substantially equal rate to that of the second resist pattern **560**. Thus, when the second organic film **555** is dry-etched, the second resist pattern **560** is also removed simultaneously. It should be noted that part of the second resist pattern **560** may be left in the process step of dry-etching the second organic film **555**. This is because the residual second resist pattern **560** can be removed during a subsequent process step of dry-etching the first organic film **553** (see FIG. **26**(*c*)).

Thereafter, the patterned second silicon dioxide film **556**A and the first silicon dioxide film **554** are dry-etched using the mask pattern **559** and the patterned second organic film **555**A as respective masks, thereby forming a patterned second silicon dioxide film **556**B having wiring grooves and a patterned first silicon dioxide film **554**A having openings for forming contact holes as shown in FIGS. **26**(*b*) and **28**(*b*). Then, the patterned second organic film **555**A is dry-etched using the mask pattern **559** and the patterned second silicon dioxide film **556**B as a mask, and the first organic film **553** is dry-etched using the patterned first silicon dioxide film **554**A as a mask, thereby forming a patterned second organic film **555**B having wiring grooves **561** and a patterned first organic film **553**A having contact holes **562** as shown in FIGS. **26**(*c*) and **29**(*a*).

Subsequently, the silicon nitride film **552** is dry-etched using the patterned first silicon dioxide film **554**A as a mask, thereby forming a patterned silicon nitride film **552**A (see FIG. **26**(*d*)) having contact holes, and exposing the first metal interconnects **551** within the contact holes **562**. Then, although not shown, an adhesion layer, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **562** and the wiring grooves **561** as in the first embodiment. Thereafter, a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes **562** and the wiring grooves **561**. Finally, respective portions of the adhesion layer, the metal film and the mask pattern **559**, which are deposited on the patterned second silicon dioxide film **556**B, are removed by a CMP technique, for example. As a result, second metal interconnects **563** and contacts **564**, connecting the first and second metal interconnects **551** and **563** together, are formed as shown in FIGS. **26**(*d*) and **29**(*b*).

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **563** through the same process steps as those described above.

According to this modified example of the fifth embodiment, the sizes of the openings of the second resist pattern **560** for forming contact holes are set larger than designed sizes of the contact holes in respective directions vertical and parallel to the wiring grooves for forming the second metal interconnects. Thus, even if the openings of the second resist pattern **560** for forming contact holes have misaligned with the openings of the mask pattern **559** for forming wiring grooves, the openings of the patterned second silicon dioxide film **556**A for forming contact holes can be formed to be self-aligned with the openings of the mask pattern **559** for forming wiring grooves. This is because the openings of the patterned second silicon dioxide film **556**A for forming contact holes are formed in respective regions where the openings of the second resist pattern **560** for forming contact holes overlap with corresponding open-

ings of the mask pattern **559** for forming wiring grooves. Accordingly, the connection between the contacts **564** and the second metal interconnects **563** is ensured.

In addition, the size of the openings of the second resist pattern **560** for forming contact holes is also extended in the direction parallel to the wiring grooves for forming the second metal interconnects. Thus, the contact area between contacts **564** and the second metal interconnects **563** expands. As a result, the contacts **564** can connect the first and second metal interconnects **551** and **563** together with a lot more certainty.

FIG. **36** illustrates a positional relationship between the openings of the mask pattern **559** for forming wiring grooves and those of the second resist pattern **560** for forming contact holes in this modified example of the fifth embodiment. As shown in FIG. **36**, the size of the openings of the second resist pattern **560** for forming contact holes are larger than the designed size.

FIG. **37**(*a*) illustrates respective positional relationships between the mask pattern **559** and the second resist pattern **560** and between a first metal interconnect **551** and a contact **564** in this modified example of the fifth embodiment. Specifically, the upper part of FIG. **37**(*a*) illustrates a positional relationship between an opening of the mask pattern **559** for forming a wiring groove and an associated opening of the second resist pattern **560** for forming a contact hole. The middle part of FIG. **37**(*a*) illustrates the cross section of the upper part taken along the line A—A. And the lower part of FIG. **37**(*a*) illustrates a positional relationship between a first metal interconnect **551** and an associated contact **564**. FIG. **37**(*b*) illustrates respective positional relationships between the mask pattern **509** and the second resist pattern **510** and between a first metal interconnect **501** and a contact **514** in the fifth embodiment. Specifically, the upper part of FIG. **37**(*b*) illustrates a positional relationship between an opening of the mask pattern **509** for forming a wiring groove and an associated opening of the second resist pattern **510** for forming a contact hole. The middle part of FIG. **37**(*b*) illustrates the cross section of the upper part taken along the line B—B. And the lower part of FIG. **37**(*b*) illustrates a positional relationship between a first metal interconnect **501** and an associated contact **514**.

Setting the size of an opening of the second resist pattern **510** for forming a contact hole at the designed size thereof as in the fifth embodiment, if the opening of the second resist pattern **510** for forming a contact hole has misaligned with an associated opening of the mask pattern **509** for forming a wiring groove, then the contact area (indicated by hatching) between the contact **514** and the first metal interconnect **501** greatly decreases as can be seen from FIG. **37**(*b*). In contrast, setting the size of an opening of the second resist pattern **560** for forming a contact hole larger than the designed size thereof as in this modified example of the fifth embodiment, even if the opening of the second resist pattern **560** for forming a contact hole has misaligned with an associated opening of the mask pattern **559** for forming a wiring groove, the contact area (indicated by hatching) between the contact **564** and the first metal interconnect **551** does not decrease so much as can be seen from FIG. **37**(*a*).

EMBODIMENT 6

Next, an exemplary method for forming an interconnection structure according to the sixth embodiment of the present invention will be described with reference to FIGS. **30**(*a*) through **30**(*c*), FIGS. **31**(*a*) through **31**(*c*) and FIGS. **32**(*a*) through **32**(*c*).

First, as shown in FIG. **30**(*a*), a silicon nitride film **602** is formed over first metal interconnects **601** formed on a semiconductor substrate **600**. The silicon nitride film **602** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **601** during a subsequent etching process step. Thereafter, a first organic film **603** (first insulating film), mainly composed of an organic component, is deposited to be 400 nm thick, for example, on the silicon nitride film **602**. Then, a silicon dioxide film **604** (second insulating film) is deposited to be 100 nm thick, for example, on the first organic film **603**. Subsequently, a second organic film **605** (third insulating film), mainly composed of an organic component, is deposited to be 300 nm thick, for example, on the silicon dioxide film **604**. And a titanium nitride film **606** (thin film) is deposited to be 50 nm thick, for example, on the second organic film **605**.

The first and second organic films **603** and **605** may be deposited by any arbitrary technique. For example, these films **603** and **605** may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic films **603** and **605**. More specifically, the organic films **603** and **605** may be made of polytetrafluoroethylene, oxygen-containing polytetrafluoroethylene, polyimide fluoride or polyaryl ether.

The silicon dioxide film **604** may also be deposited by any arbitrary technique. For example, the film **604** may be deposited by a plasma CVD process.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films **603** and **605** and the silicon dioxide film **604**, i.e., a thin film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **606**.

Next, as shown in FIG. **30**(*b*), a first resist pattern **607**, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film **606**. Thereafter, the titanium nitride film **606** is dry-etched using the first resist pattern **607** as a mask, thereby forming a mask pattern **608**, having openings for forming wiring grooves, out of the titanium nitride film **606** as shown in FIG. **30**(*c*).

Subsequently, as shown in FIG. **31**(*a*), the first resist pattern **607** is removed using an organic parting agent, for example. In such a case, since the second organic film **605** is not exposed to oxygen plasma, the quality of the second organic film **605** does not degrade.

Then, as shown in FIG. **31**(*b*), a second resist pattern **609**, having openings for forming contact holes, is formed by lithography on the mask pattern **608**. Then, the second organic film **605** is dry-etched using the second resist pattern **609** and the mask pattern **608** as a mask, thereby forming a patterned second organic film **605**A having openings for forming contact holes as shown in FIG. **31**(*c*). In this case, the second organic film **605** and the second resist pattern **609** are both mainly composed of organic components, the second organic film **605** is etched at a substantially equal rate to that of the second resist pattern **609**. Thus, when the second organic film **605** is dry-etched, the second resist pattern **609** is also removed simultaneously.

It should be noted that part of the second resist pattern **609** may be left in the process step of dry-etching the second organic film **605**. This is because the residual second resist pattern **609** can be removed during a subsequent process step of dry-etching the first organic film **603** (see FIG. **32**(*b*)).

Thereafter, the silicon dioxide film **604** is dry-etched using the patterned second organic film **605**A as a mask, thereby forming a patterned silicon dioxide film **604**A having openings for forming contact holes as shown in FIG. **32**(*a*).

Then, the patterned second organic film **605**A and the first organic film **603** are dry-etched using the mask pattern **608** and the patterned silicon dioxide film **604**A as respective masks, thereby forming a patterned second organic film **605**B having wiring grooves **610** and a patterned first organic film **603**A having contact holes **611** as shown in FIG. **32**(*b*).

Subsequently, the patterned silicon dioxide film **604**A and the silicon nitride film **602** are dry-etched using the mask pattern **608** and the patterned first organic film **603**A as respective masks, thereby forming a patterned silicon dioxide film **604**B having wiring grooves (see FIG. **32**(*c*)) and a patterned silicon nitride film **602**A having the contact holes (see FIG. **32**(*c*)), and exposing the first metal interconnects **601** within the contact holes **611**. Then, although not shown, an adhesion layer, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **611** and the wiring grooves **610** as in the first embodiment. Thereafter, a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes **611** and the wiring grooves **610**. In this embodiment, the metal film may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed. Finally, respective portions of the adhesion layer, the metal film and the mask pattern **608**, which are deposited on the patterned second organic film **605**B, are removed by a CMP technique, for example. As a result, second metal interconnects **612** and contacts **613**, connecting the first and second metal interconnects **601** and **612** together, are formed as shown in FIG. **32**(*c*).

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **612** through the same process steps as those described above.

In the sixth embodiment, a patterned second organic film **605**B, having wiring grooves **610**, and a patterned first organic film **603**A, having contact holes **611**, are formed by a single dry-etching process using the mask pattern **608**, having the openings for forming wiring grooves, and the patterned silicon dioxide film **604**A as respective masks. That is to say, the wiring grooves **610** and the contact holes **611** can be formed during the same etching process step. Accordingly, a dual damascene structure can be formed with the increase in number of process steps suppressed.

Also, in the sixth embodiment, since the first resist pattern **607** is removed by an organic parting agent, for example, the quality of the second organic film **605** does not degrade.

Furthermore, in this embodiment, the silicon dioxide film **604** functions as an etch stopper during dry-etching the second organic film **605**. Accordingly, it is possible to prevent the quality of the first organic film **603** from being degraded.

MODIFIED EXAMPLE OF EMBODIMENT 6

Next, a method for forming an interconnection structure according to a modified example of the sixth embodiment will be described with reference to FIGS. **33**(*a*) through **33**(*c*), FIGS. **34**(*a*) through **34**(*c*) and FIGS. **35**(*a*) through **35**(*c*).

First, as shown in FIG. **33**(*a*), a silicon nitride film **652** is formed over first metal interconnects **651** formed on a semiconductor substrate **650**. The silicon nitride film **652** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **651** during a subsequent etching process step. Thereafter, a first organic film **653** (first insulating film), mainly composed of an organic component, is deposited to be 400 nm thick, for example, on the silicon nitride film **652**. Then, a silicon dioxide film **654** (second insulating film) is deposited to be 100 nm thick, for example, on the first organic film **653**. Subsequently, a second organic film **655** (third insulating film), mainly composed of an organic component, is deposited to be 300 nm thick, for example, on the silicon dioxide film **654**. And a titanium nitride film **656** (thin film) is deposited to be 50 nm thick, for example, on the second organic film **655**.

The first and second organic films **653** and **655** may be deposited by any arbitrary technique. For example, these films **653** and **655** may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic films **653** and **655**. More specifically, the organic films **653** and **655** may be made of polytetrafluoroethylene, oxygen-containing polytetrafluoroethylene, polyimide fluoride or polyaryl ether.

The silicon dioxide film **654** may also be deposited by any arbitrary technique. For example, the film **654** may be deposited by a plasma CVD process.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films **653** and **655** and the silicon dioxide film **654**, i.e., a thin film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **656**.

Next, as shown in FIG. **33**(*b*), a first resist pattern **657**, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film **656**. Thereafter, the titanium nitride film **656** is dry-etched using the first resist pattern **657** as a mask, thereby forming a mask pattern **658**, having openings for forming wiring grooves, out of the titanium nitride film **656** as shown in FIG. **33**(*c*).

Subsequently, as shown in FIG. **34**(*a*), the first resist pattern **657** is removed by an organic parting agent, for example. In such a case, since the second organic film **655** is not exposed to oxygen plasma, the quality of the second organic film **655** does not degrade.

Then, as shown in FIG. **34**(*b*), a second resist pattern **659**, having openings for forming contact holes, is formed by lithography on the mask pattern **658**. In this modified example of the sixth embodiment, the sizes of the openings of the second resist pattern **659** for forming contact holes are set larger than designed sizes of the contact holes in respective directions vertical and parallel to the wiring grooves for forming second metal interconnects. The reason thereof will be described later.

Next, the second organic film **655** is dry-etched using the second resist pattern **659** and the mask pattern **658** as a mask, thereby forming a patterned second organic film **655**A having openings for forming contact holes as shown in FIG. **34**(*c*). In this case, the second organic film **655** and the second resist pattern **659** are both mainly composed of organic components, the second organic film **655** is etched at a substantially equal rate to that of the second resist pattern **659**. Thus, when the second organic film **655** is dry-etched, the second resist pattern **659** is also removed

simultaneously. It should be noted that part of the second resist pattern **659** may be left in the process step of dry-etching the second organic film **655**. This is because the residual second resist pattern **659** can be removed during a subsequent process step of dry-etching the first organic film **653** (see FIG. **35**(*b*)).

Thereafter, the silicon dioxide film **654** is dry-etched using the patterned second organic film **655**A as a mask, thereby forming a patterned second silicon dioxide film **654**A having openings for forming contact holes as shown in FIG. **35**(*a*).

Then, the patterned second organic film **655**A and the first organic film **653** are dry-etched using the mask pattern **658** and the patterned silicon dioxide film **654**A as respective masks, thereby forming a patterned second organic film **655**B having wiring grooves **660** and a patterned first organic film **653**A having contact holes **661** as shown in FIG. **35**(*b*).

Subsequently, the patterned silicon dioxide film **654**A and the silicon nitride film **652** are dry-etched using the mask pattern **658** and the patterned first organic film **653**A as respective masks, thereby forming a patterned silicon dioxide film **654**B having wiring grooves (see FIG. **35**(*c*)) and a patterned silicon nitride film **652**A having the contact holes (see FIG. **35**(*c*)), and exposing the first metal interconnects **651** within the contact holes **661**. Then, although not shown, an adhesion layer, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **661** and the wiring grooves **660** as in the first embodiment. Thereafter, a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes **661** and the wiring grooves **660**. In this embodiment, the metal film may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed. Finally, respective portions of the adhesion layer, the metal film and the mask pattern **658**, which are deposited on the patterned second organic film **655**B, are removed by a CMP technique, for example. As a result, second metal interconnects **662** and contacts **663**, connecting the first and second metal interconnects **651** and **662** together, are formed as shown in FIG. **35**(*c*).

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **662** through the same process steps as those described above.

In this modified example of the sixth embodiment, the sizes of the openings of the second resist pattern **659** for forming contact holes are set larger than designed sizes of the contact holes in respective directions vertical and parallel to the wiring grooves for forming the second metal interconnects. Accordingly, even if the openings of the second resist pattern **659** for forming contact holes have misaligned with the openings of the mask pattern **658** for forming wiring grooves, the openings of the patterned second organic film **655**A for forming contact holes can be formed to be self-aligned with the openings of the mask pattern **658** for forming wiring grooves. This is because the openings of the patterned second organic film **655**A for forming contact holes are formed in respective regions where the openings of the second resist pattern **659** for forming contact holes overlap with corresponding openings of the mask pattern **658** for forming wiring grooves. Accordingly, the connection between the contacts **663** and the second metal interconnects **662** is ensured.

In addition, the size of the openings of the second resist pattern **659** for forming contact holes is also extended in the direction parallel to the wiring grooves for forming second metal interconnects. Thus, the contact area between the contacts **663** and the second metal interconnects **662** expands.

As a result, the contacts **663** can connect the first and second metal interconnects **651** and **662** together with a lot more certainty.

What is claimed is:

1. A method for forming an interconnection structure, comprising the steps of:

a) forming a first insulating film over lower-level metal interconnects;

b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;

c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

d) forming a thin film over the third insulating film;

e) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;

f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;

g) forming a second resist pattern on the third insulating film, the second resist pattern having openings for forming contact holes;

h) dry-etching the third insulating film under such conditions that the third insulating film and the first and second resist patterns are etched at a relatively high rate and that the second insulating film is etched at a relatively low rate, thereby patterning the third insulating film to have the openings for forming contact holes and removing the first and second resist patterns either entirely or partially with respective lower parts thereof left;

i) dry-etching the second insulating film using the patterned third insulating film as a mask under such conditions that the second insulating film is etched at a relatively high rate and that the first and third insulating films are etched at a relatively low rate, thereby patterning the second insulating film to have the openings for forming contact holes;

j) dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and

k) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

2. The method of claim **1**, further comprising the step of forming a metal adhesion layer over part of the third insulating film exposed inside the wiring grooves and part of the first insulating film exposed inside the contact holes between the steps j) and k).

3. The method of claim **1**, wherein the third insulating film is mainly composed of an organic component.

4. The method of claim 3, wherein the step c) includes forming the third insulating film by a CVD process using a reactive gas containing perfluorodecalin.

5. The method of claim 3, wherein the first insulating film is mainly composed of an organic component.

6. The method of claim 5, further comprising the step of forming an adhesion layer over part of the third insulating film exposed inside the wiring grooves and part of the first insulating film exposed inside the contact holes by a plasma process using a reactive gas containing nitrogen between the steps j) and k).

7. The method of claim 3, wherein the step a) includes forming the first insulating film by a CVD process using a reactive gas containing perfluorodecalin.

8. A method for forming an interconnection structure, comprising the steps of:

a) forming a first insulating film over lower-level metal interconnects;

b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;

c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

d) forming a thin film over the third insulating film;

e) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;

f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;

g) forming a second resist pattern on the third insulating film, the second resist pattern having openings for forming contact holes;

h) dry-etching the third insulating film using the first and second resist patterns as a mask under such conditions that the third insulating film is etched at a relatively high rate and that the second insulating film and the first and second resist patterns are etched at a relatively low rate, thereby patterning the third insulating film to have the openings for forming contact holes;

i) dry-etching the second insulating film using the first and second resist patterns as a mask under such conditions that the second insulating film is etched at a relatively high rate and that the first and third insulating films and the first and second resist patterns are etched at a relatively low rate, thereby patterning the second insulating film to have the openings for forming contact holes;

j) removing the first and second resist patterns;

k) dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and

l) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

9. The method of claim 8, wherein the third insulating film is a low-dielectric-constant SOG film with a siloxane skeleton.

10. A method for forming an interconnection structure, comprising the steps of:

a) forming a first insulating film over lower-level metal interconnects;

b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;

c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

d) forming a fourth insulating film, having a different composition than that of the third insulating film, over the third insulating film;

e) forming a thin film over the fourth insulating film;

f) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;

g) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;

h) removing the first resist pattern and then forming a second resist pattern on the fourth insulating film and the mask pattern, the second resist pattern having openings for forming contact holes;

i) dry-etching the fourth insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the fourth insulating film to have the openings for forming contact holes;

j) dry-etching the third insulating film using the patterned fourth insulating film as a mask, thereby patterning the third insulating film to have the openings for forming contact holes;

k) dry-etching the patterned fourth insulating film and the second insulating film using the mask pattern and the patterned third insulating film as respective masks, thereby forming wiring grooves in the patterned fourth insulating film and patterning the second insulating film to have the openings for forming contact holes;

l) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming the wiring grooves and the contact holes in the patterned third insulating film and the first insulating film, respectively; and

m) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

11. The method of claim 10, wherein at least one of the first and third insulating films is mainly composed of an organic component.

12. The method of claim 10, wherein a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.

13. A method for forming an interconnection structure, comprising the steps of:

a) forming a first insulating film over lower-level metal interconnects;

b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;

c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

d) forming a thin film over the third insulating film;

e) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;

f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;

g) removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes;

h) dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes;

i) dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes;

j) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively; and

k) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

14. The method of claim **13**, wherein at least one of the first and third insulating films is mainly composed of an organic component.

15. The method of claim **13**, wherein a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.

* * * * *

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SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/274,114	03/23/99	216	1763	0819-226

APPLICANT

NOBUO AOI, HYOGO, JAPAN.

CONTINUING DOMESTIC DATA******** none
VERIFIED
L.T.N-E.

371 (NAT'L STAGE) DATA******** none
VERIFIED
L.T.N.E.

FOREIGN APPLICATIONS********
VERIFIED JAPAN 10-079371 03/26/98
L.T.N.E.

IF REQUIRED, FOREIGN FILING LICENSE GRANTED 04/13/99

Foreign Priority claimed 35 USC 119 (a-d) conditions met	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☒yes ☐no ☒yes ☐no ☐Met after Allowance Verified and Acknowledged L.T.N-E (Examiner's Initials) _____ (Initials)	JPX	37	15	4

ADDRESS

GERALD J FERGUSON JR
SIXBEY FRIEDMAN LEEDOM & FERGUSON
8180 GREENSBORO DRIVE
SUITE 800
MCLEAN VA 22102

TITLE

METHOD FOR FORMING INTERCONNECTION STRUCTURE

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PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

04/01/1999 PALLEN 00000052 09274114

01 FC:101 760.00 OP
02 FC:102 78.00 OP

PTO-1556
(5/87)

*U.S. GPO: 1998-433-214/80404

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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 0819-226

First Inventor or Application Identifier: Nobuo AOI

Title: METHOD FOR FORMING INTERCONNECTION STRUCTURE

Express Mail Label No.

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [X] Fee Transmittal Form (e.g., PTO/SB/17)
   (Submit an original, and a duplicate for fee processing)
2. [X] Specification *Total Pages* [91]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 USC 113) *Total Sheets* [37]
4. [X] Oath or Declaration *Total Pages* [2]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 17 completed)
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   i. [ ] DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

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6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission
   (if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement [ ] Power of Attorney
   (when there is an assignee)
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement [ ] Copies of IDS Citations
    (IDS)/PTO-1449
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503)
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14. [ ] *Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
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    Prior application information: Examiner: _____ Group/Art Unit: _____

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[ ] Customer Number or Bar Code Label or [X] Correspondence address below

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Name: Eric J. Robinson
Firm: SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.
Address: 8180 Greensboro Drive, Suite 800
City: McLean State: VA Zip Code: 22102
Country: U.S.A. Telephone (703) 790-9110 FAX (703) 883-0370

Name: Eric J. Robinson Registration No. 38,285

Signature Date: March 23, 1999

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JC408 U.S. PTO
03/23/99
09274114 = 032399
JC530 U.S. PTO
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 0819-226

First Inventor or Application Identifier: Nobuo AOI

Title: METHOD FOR FORMING INTERCONNECTION STRUCTURE

Express Mail Label No.

jc530 U.S. PTO
09/274114
03/23/99

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

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8. [X] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement [ ] Power of Attorney
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Name: Eric J. Robinson Registration No. 38,285

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TOTAL AMOUNT OF PAYMENT	$878.00

Complete If Known	
Application Number	
Filing Date	March 23, 1999
First Named Inventor	Nobuo AOI
Examiner Name	
Group Art Unit	
Attorney Docket Number	0819-228

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:
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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	760	201	380	Utility filing fee	[760]
106	310	206	155	Design filing fee	[ ]
107	480	207	240	Plant filing fee	[ ]
108	760	208	380	Reissue filing fee	[ ]
114	150	214	75	Provisional filing fee	[ ]
				SUBTOTAL (1)	$760.00

2. EXTRA CLAIM FEES

	Extra Claims	Fee from Below	Fee Paid
Total Claims	15 - 20** = 0	X $18.00 =	
Independent Claims	4 - 3** = 1	X $78.00 =	$78.00
Multiple Dependent Claims		=	

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103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim
109	78	209	39	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent
				SUBTOTAL (2) $78.00

FEE CALCULATION (continued)

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105	130	205	65	Surcharge-late filing fee or oath	
127	50	227	25	Surcharge-late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Ext for reply within first month	
116	380	216	190	Ext for reply within second mth	
117	870	217	435	Ext for reply within third mth	
118	1,360	218	680	Ext for reply within fourth mth	
128	1,850	228	925	Ext for reply within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing brief in support of appeal	
121	260	221	130	Request for Oral Hearing	
138	1,510	138	1,510	Petition to institute public use proceeding	
140	110	240	55	Petition to revive-unavoidable	
141	1,210	241	605	Petition to revive-unintentional	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of IDS	
581	40	581	40	Recording each patent assignment per property (times number of properties)	$40.00
146	760	246	380	Filing a submission after final rejection (37 CFR 1.129(a))	
149	760	249	380	For each additional invention to be examined (37 CFR 1.129(b))	
				Other	
				Other	
				*Reduced by Basic Filing Fee Paid	
				SUBTOTAL (3)	$40.00

SUBMITTED BY

Complete (if applicable)

Typed or Printed Name	Eric J. Robinson			Reg. Number	38,285
Signature		Date	March 23, 1999	Deposit Account User ID	19-2380

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Complete If Known	
Application Number	
Filing Date	March 23, 1999
First Named Inventor	Nobuo AOI
Examiner Name	
Group Art Unit	
Attorney Docket Number	0819-226

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107	480	207	240	Plant filing fee	[ ]
108	760	208	380	Reissue filing fee	[ ]
114	150	214	75	Provisional filing fee	[ ]
				SUBTOTAL (1)	$760.00

2. EXTRA CLAIM FEES

	Extra Claims	Fee from Below	Fee Paid
Total Claims	15 - 20** =	0 X $18.00 =	
Independent Claims	4 - 3** =	1 X $78.00 =	$78.00
Multiple Dependent Claims		=	

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FEE CALCULATION (continued)

3. ADDITIONAL FEES

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149	760	249	380	For each additional invention to be examined (37 CFR 1.129(b))	
				Other	
				Other	
				*Reduced by Basic Filing Fee Paid	
				SUBTOTAL (3)	$40.00

SUBMITTED BY				Complete (if applicable)	
Typed or Printed Name	Eric J. Robinson			Reg. Number	38,285
Signature		Date	March 23, 1999	Deposit Account User ID	19-2380

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METHOD FOR FORMING INTERCONNECTION STRUCTURE

BACKGROUND OF THE INVENTION

The present invention relates to a method for forming an interconnection structure in a semiconductor integrated circuit.

As the number of devices, integrated within a single semiconductor integrated circuit, has been tremendously increasing these days, wiring delay has also been increasing noticeably. This is because the larger the number of devices integrated, the larger line-to-line capacitance (i.e., parasitic capacitance between metal interconnects), thus interfering with the performance improvement of a semiconductor integrated circuit. The wiring delay is so-called "RC delay", which is proportional to the product of the resistance of metal interconnection and the line-to-line capacitance.

In other words, to reduce the wiring delay, either the resistance of metal interconnection or the line-to-line capacitance should be reduced.

In order to reduce the interconnection resistance, IBM Corp., Motorola, Inc., etc. have reported semiconductor integrated circuits using copper, not aluminum alloy, as a material for metal interconnects. A copper material has a specific resistance about two-thirds as high as that of an aluminum alloy material. Accordingly, in accordance with

simple calculation, the wiring delay involved with the use of a copper material for metal interconnects can be about two-thirds of that involved with the use of an aluminum alloy material therefor. That is to say, the operating speed can be increased by about 1.5 times.

However, the number of devices, integrated within a single semiconductor integrated circuit, is expected to further increase by leaps and bounds from now on, thus increasing the wiring delay considerably. Therefore, it is concerned that even the use of copper as an alternate metal interconnection material would not be able to catch up with such drastic increase. Also, the specific resistance of copper as a metal interconnection material is just a little bit higher than, but almost equal to, that of gold or silver. Accordingly, even if gold or silver is used instead of copper as a metal interconnection material, the wiring delay can be reduced only slightly.

Under these circumstances, not only reducing interconnection resistance but also suppressing line-to-line capacitance play a key role in further increasing the number of devices that can be integrated within a single semiconductor integrated circuit. And the relative dielectric constant of an interlevel insulating film should be reduced to suppress the line-to-line capacitance. A silicon dioxide film has heretofore been used as a typical material for an interlevel

insulating film. The relative dielectric constant of a silicon dioxide film is, however, about 4 to about 4.5. Thus, it would be difficult to apply a silicon dioxide film to a semiconductor integrated circuit incorporating an even larger number of devices.

In order to solve such a problem, fluorine-doped silicon dioxide film, low-dielectric-constant spin-on-glass (SOG) film, organic polymer film and so on have been proposed as alternate interlevel insulating films with respective relative dielectric constants smaller than that of a silicon dioxide film.

The relative dielectric constant of a fluorine-doped silicon dioxide film is about 3.3 to about 3.7, which is about 20 percent lower than that of a conventional silicon dioxide film. Nevertheless, a fluorine-doped silicon dioxide film is highly hygroscopic, and easily absorbs water in the air, resulting in various problems in practice. For example, when the fluorine-doped silicon dioxide film absorbs water, SiOH groups, having a high relative dielectric constant, are introduced into the film. As a result, the relative dielectric constant of the fluorine-doped silicon dioxide film adversely increases, or the SiOH groups react with the water during a heat treatment to release H_2O gas. In addition, fluorine free radicals, contained in the fluorine-doped silicon dioxide film, segregate near the surface thereof during a

heat treatment and react with Ti, contained in a TiN layer formed thereon as an adhesion layer, to form a TiF film, which easily peels off.

An HSQ (hydrogen silsesquioxane) film, composed of Si, O and H atoms, is an exemplary low-dielectric-constant SOG film. In the HSQ film, the number of the H atoms is about two-thirds of that of the O atoms. However, the HSQ film releases a larger amount of water than a conventional silicon dioxide film. Accordingly, since it is difficult to form a buried interconnection line in the HSQ film, a patterned metal film should be formed as metal interconnects on the HSQ film.

Also, since the HSQ film cannot adhere so strongly to metal interconnects, a CVD oxide film should be formed between the metal interconnects and the HSQ film to improve the adhesion therebetween. However, in such a case, if the CVD oxide film is formed on the metal interconnects, then the substantial line-to-line capacitance is equal to the serial capacitance formed by the HSQ and CVD films. This is because the CVD oxide film with a high dielectric constant exists between the metal interconnects. Accordingly, the resulting line-to-line capacitance is larger as compared with using the HSQ film alone.

An organic polymer film, as well as the low-dielectric-constant SOG film, cannot adhere strongly to metal intercon-

nects, either. Accordingly, a CVD oxide film should be formed as an adhesion layer between the metal interconnects and the organic polymer film, too.

Moreover, an etch rate, at which an organic polymer film is etched, is approximately equal to an ash rate, at which a resist pattern is ashed with oxygen plasma. Accordingly, a usual resist application process is not applicable in such a situation, because the organic polymer film is likely to be damaged during ashing and removing the resist pattern. Therefore, a proposed alternate process includes: forming a CVD oxide film on an organic polymer film; forming a resist film on the CVD oxide film; and then etching the resist film using the CVD oxide film as an etch stopper, or a protective film.

However, during the step of forming the CVD oxide film on the organic polymer film, the surface of the organic polymer film is exposed to a reactive gas containing oxygen. Accordingly, the organic polymer film reacts with oxygen to take in polar groups such as carbonyl groups and ketone groups. As a result, the relative dielectric constant of the organic polymer film disadvantageously increases.

Also, in forming inlaid copper interconnects in the organic polymer film, a TiN adhesion layer, for example, should be formed around wiring grooves formed in the organic polymer film, because the organic polymer film cannot adhere strongly

to the metal interconnects. However, since the TiN film has a high resistance, the effective cross-sectional area of the metal interconnects decreases. Consequently, the intended effect attainable by the use of the copper lines, i.e., reduction in resistance, would be lost.

SUMMARY OF THE INVENTION

An object of the present invention is providing a method for forming an interconnection structure in which an insulating film with a low dielectric constant can be formed by an ordinary resist application process.

A first method for forming an interconnection structure according to the present invention includes the steps of: a) forming a first insulating film over lower-level metal interconnects; b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; d) forming a thin film over the third insulating film; e) forming a first resist pattern, having a plurality of openings for forming wiring grooves, on the thin film; f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves; g) forming a second resist pattern,

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having a plurality of openings for forming contact holes, on the third insulating film; h) dry-etching the third insulating film under such conditions that the third insulating film and the first and second resist patterns are etched at a relatively high rate and that the second insulating film is etched at a relatively low rate, thereby patterning the third insulating film to have the openings for forming contact holes and removing the first and second resist patterns either entirely or partially with respective lower parts thereof left; i) dry-etching the second insulating film using the patterned third insulating film as a mask under such conditions that the second insulating film is etched at a relatively high rate and that the first and third insulating films are etched at a relatively low rate, thereby patterning the second insulating film to have the openings for forming contact holes; j) dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and k) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts con-

Substitute Specification

necting the lower- and upper-level metal interconnects together.

In the first method of the present invention, the third insulating film is dry-etched under such conditions that the third insulating film and the first and second resist patterns are etched at a relatively high rate and that the second insulating film is etched at a relatively low rate, thereby patterning the third insulating film and removing the first and second resist patterns in the step h). Accordingly, it is not necessary to perform the step of ashing and removing the first and second resist patterns with oxygen plasma. In other words, since it is possible to prevent the third insulating film from being damaged during ashing and removing a resist pattern, a low-dielectric-constant insulating film, which would otherwise be damaged easily by oxygen plasma, may be used as the third insulating film. As a result, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

In addition, the second insulating film can be used as an etch stopper while the wiring grooves are formed by dry-etching the third insulating film using the mask pattern as a mask in the step j). Accordingly, the depth of each wiring groove can be equalized with the thickness of the third insulating film. That is to say, the depth of the wiring grooves

can be defined by self-alignment.

Moreover, the composition of the second insulating film is different from that of the third insulating film. Thus, the second insulating film can be used as an etch stopper while the wiring grooves are formed by dry-etching the third insulating film using the mask pattern as a mask in the step j).

In one embodiment of the present invention, the first method preferably further includes the step of forming a metal adhesion layer over part of the third insulating film exposed inside the wiring grooves and part of the first insulating film exposed inside the contact holes between the steps j) and k).

In such an embodiment, the adhesion between the upper-level metal interconnects and the third insulating film and between the contacts and the first insulating film can be improved.

In another embodiment of the present invention, the third insulating film is preferably mainly composed of an organic component.

In such an embodiment, the conditions employed in the step h), i.e., that the third insulating film and the first and second resist patterns are etched at a relatively high rate and that the second insulating film is etched at a relatively low rate, are realized with much more certainty.

In this embodiment, the step c) preferably includes forming the third insulating film by a CVD process using a reactive gas containing perfluorodecalin.

Then, a film mainly composed of an organic component and having a low relative dielectric constant can be formed as the third insulating film with a lot more certainty.

In another embodiment, the first insulating film is also preferably mainly composed of an organic component.

Then, the conditions employed in the step i), i.e., that the second insulating film is etched at a relatively high rate and that the first and third insulating films are etched at a relatively low rate, are realized with much more certainty. At the same time, the conditions employed in the step j), i.e., that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, are also realized with much more certainty.

In an embodiment where the first and third insulating films are both mainly composed of organic components, the first method preferably further includes the step of forming an adhesion layer over part of the third insulating film exposed inside the wiring grooves and part of the first insulating film exposed inside the contact holes by a plasma process using a reactive gas containing nitrogen between the steps j) and k).

In such a case, the adhesion between the upper-level metal interconnects and the third insulating film mainly composed of an organic component, and between the contacts and the first insulating film mainly composed of an organic component can be improved substantially without fail.

In the embodiment where the first insulating film is mainly composed of an organic component, the step a) preferably includes forming the first insulating film by a CVD process using a reactive gas containing perfluorodecalin.

In such a case, a film mainly composed of an organic component and having a low relative dielectric constant can be formed as the first insulating film with a lot more certainty.

A second method for forming an interconnection structure according to the present invention includes the steps of: a) forming a first insulating film over lower-level metal interconnects; b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; d) forming a thin film over the third insulating film; e) forming a first resist pattern, having a plurality of openings for forming wiring grooves, on the thin film; f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for

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forming wiring grooves; g) forming a second resist pattern, having a plurality of openings for forming contact holes, on the third insulating film; h) dry-etching the third insulating film using the first and second resist patterns as a mask under such conditions that the third insulating film is etched at a relatively high rate and that the second insulating film and the first and second resist patterns are etched at a relatively low rate, thereby patterning the third insulating film to have the openings for forming contact holes; i) dry-etching the second insulating film using the first and second resist patterns as a mask under such conditions that the second insulating film is etched at a relatively high rate and that the first and third insulating films and the first and second resist patterns are etched at a relatively low rate, thereby patterning the second insulating film to have the openings for forming contact holes; j) removing the first and second resist patterns; k) dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and l) filling in the wiring grooves and the contact holes with a metal film,

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thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

In the second method of the present invention, even if a damaged layer is formed in respective parts of the first and third insulating films that are exposed inside the openings for forming contact holes in the second insulating film during the step j) of removing the first and second resist patterns, the damaged layer can be removed without fail in the next step k). In this step, the third and first insulating films are dry-etched using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively. Accordingly, low-dielectric-constant insulating films, which would otherwise be damaged easily by oxygen plasma, can be used as the first and third insulating films. As a result, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

In one embodiment of the present invention, the third insulating film is preferably a low-dielectric-constant SOG film with a siloxane skeleton.

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In such an embodiment, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

A third method for forming an interconnection structure according to the present invention includes the steps of: a) forming a first insulating film over lower-level metal interconnects; b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; d) forming a fourth insulating film, having a different composition than that of the third insulating film, over the third insulating film; e) forming a thin film over the fourth insulating film; f) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves; g) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves; h) removing the first resist pattern and then forming a second resist pattern on the fourth insulating film and the mask pattern, the second resist pattern having openings for forming contact holes; i) dry-etching the fourth insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the fourth insulating film to have the openings for

forming contact holes; j) dry-etching the third insulating film using the patterned fourth insulating film as a mask, thereby patterning the third insulating film to have the openings for forming contact holes; k) dry-etching the patterned fourth insulating film and the second insulating film using the mask pattern and the patterned third insulating film as respective masks, thereby forming wiring grooves in the patterned fourth insulating film and patterning the second insulating film to have the openings for forming contact holes; l) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming the wiring grooves and the contact holes in the patterned third insulating film and the first insulating film, respectively; and m) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

In the third method of the present invention, the fourth insulating film exists on the third insulating film during the removal of the first resist pattern in the step h). Accordingly, even if the first resist pattern is removed by oxygen plasma, the third insulating film is not damaged. Also, the second insulating film exists on the first insulating film during dry-etching the third insulating film in the step j).

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Accordingly, the first insulating film is not damaged, either. Thus, low-dielectric-constant insulating films, which would otherwise be damaged easily by oxygen plasma or dry etching, can be used as the first and third insulating films. As a result, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

In one embodiment of the present invention, at least one of the first and third insulating films is preferably mainly composed of an organic component.

In such an embodiment, the relative dielectric constant of the interlevel insulating film can be reduced.

In another embodiment of the present invention, a size of the openings of the second resist pattern for forming contact holes is preferably larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.

In such an embodiment, even if the openings of the second resist pattern for forming contact holes have misaligned with the openings of the mask pattern for forming wiring grooves, the openings of the patterned fourth insulating film for forming contact holes can be formed to be self-aligned with the openings of the mask pattern for forming wiring grooves. This is because the openings of the patterned fourth insulating film for forming contact holes are formed in respective re-

gions where the openings of the second resist pattern for forming contact holes overlap with corresponding openings of the mask pattern for forming wiring grooves. As a result, the connection between the contacts and the upper-level metal interconnects is ensured.

A fourth method for forming an interconnection structure according to the present invention includes the steps of: a) forming a first insulating film over lower-level metal interconnects; b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film; c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film; d) forming a thin film over the third insulating film; e) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves; f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves; g) removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes; h) dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming

contact holes; i) dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes; j) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively; and k) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

In the fourth method of the present invention, the second insulating film exists on the first insulating film during dry-etching the third insulating film in the step h). Accordingly, the first insulating film is not damaged. Thus, low-dielectric-constant insulating films, which would otherwise be damaged easily by oxygen plasma or dry etching, can be used as the first and third insulating films. As a result, an interlevel insulating film with a low dielectric constant can be formed by an ordinary resist application process.

In one embodiment of the present invention, at least one of the first and third insulating films is preferably mainly composed of an organic component.

In such an embodiment, the relative dielectric constant

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of the interlevel insulating film can be reduced.

In another embodiment of the present invention, a size of the openings of the second resist pattern for forming contact holes is preferably larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.

In such an embodiment, even if the openings of the second resist pattern for forming contact holes have misaligned with the openings of the mask pattern for forming wiring grooves, the openings of the patterned third insulating film for forming contact holes can be formed to be self-aligned with the openings of the mask pattern for forming wiring grooves. This is because the openings of the patterned third insulating film for forming contact holes are formed in respective regions where the openings of the second resist pattern for forming contact holes overlap with corresponding openings of the mask pattern for forming wiring grooves. As a result, the connection between the contacts and the upper-level metal interconnects is ensured.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1(a) through 1(c) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the first embodiment of the present invention.

Figures **2(a)** through **2(c)** are cross-sectional views illustrating respective process steps for forming the interconnection structure of the first embodiment.

Figures **3(a)** through **3(c)** are cross-sectional views illustrating respective process steps for forming the interconnection structure of the first embodiment.

Figures **4(a)** through **4(c)** are cross-sectional views illustrating problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

Figures **5(a)** through **5(c)** are cross-sectional views illustrating the problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

Figures **6(a)** through **6(c)** are cross-sectional views illustrating the problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

Figures **7(a)** through **7(c)** are cross-sectional views illustrating measures to solve the problems caused by the misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

Figures **8(a)** through **8(c)** are cross-sectional views illustrating the measures to solve the problems caused by the

misalignment of the second resist pattern during the process of forming the interconnection structure of the first embodiment.

Figures **9(a)** through **9(c)** are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the second embodiment of the present invention.

Figures **10(a)** through **10(c)** are cross-sectional views illustrating respective process steps for forming the interconnection structure of the second embodiment.

Figures **11(a)** through **11(c)** are cross-sectional views illustrating respective process steps for forming the interconnection structure of the second embodiment.

Figures **12(a)** through **12(c)** are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the third embodiment of the present invention.

Figures **13(a)** through **13(c)** are cross-sectional views illustrating respective process steps for forming the interconnection structure of the third embodiment.

Figures **14(a)** through **14(c)** are cross-sectional views illustrating respective process steps for forming the interconnection structure of the third embodiment.

Figures **15(a)** through **15(c)** are cross-sectional views illustrating respective process steps for forming an inter-

connection structure according to a modified example of the third embodiment.

Figures **16(a)** through **16(d)** are cross-sectional views illustrating respective process steps for forming the interconnection structure of the modified example of the third embodiment.

Figures **17(a)** through **17(c)** are cross-sectional views illustrating respective process steps for forming the interconnection structure of the modified example of the third embodiment.

Figures **18(a)** through **18(c)** are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the fourth embodiment of the present invention.

Figures **19(a)** through **19(c)** are cross-sectional views illustrating respective process steps for forming the interconnection structure of the fourth embodiment.

Figures **20(a)** through **20(c)** are cross-sectional views illustrating respective process steps for forming the interconnection structure of the fourth embodiment.

Figures **21(a)** through **21(c)** are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the fifth embodiment of the present invention.

Figures **22(a)** through **22(c)** are cross-sectional views

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illustrating respective process steps for forming the interconnection structure of the fifth embodiment.

Figures **23(a)** through **23(d)** are cross-sectional views illustrating respective process steps for forming the interconnection structure of the fifth embodiment.

Figures **24(a)** through **24(c)** are cross-sectional views illustrating respective process steps for forming an interconnection structure according to a modified example of the fifth embodiment.

Figures **25(a)** through **25(c)** are cross-sectional views illustrating respective process steps for forming the interconnection structure in the modified example of the fifth embodiment.

Figures **26(a)** through **26(d)** are cross-sectional views illustrating respective process steps for forming the interconnection structure in the modified example of the fifth embodiment.

Figures **27(a)** and **27(b)** are perspective views illustrating respective process steps for forming the interconnection structure in the modified example of the fifth embodiment.

Figures **28(a)** and **28(b)** are perspective views illustrating respective process steps for forming the interconnection structure in the modified example of the fifth embodiment.

Figures **29(a)** and **29(b)** are perspective views illustrating respective process steps for forming the interconnection

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structure in the modified example of the fifth embodiment.

Figures 30(a) through 30(c) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to the sixth embodiment of the present invention.

Figures 31(a) through 31(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the sixth embodiment.

Figures 32(a) through 32(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure of the sixth embodiment.

Figures 33(a) through 33(c) are cross-sectional views illustrating respective process steps for forming an interconnection structure according to a modified example of the sixth embodiment.

Figures 34(a) through 34(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure in the modified example of the sixth embodiment.

Figures 35(a) through 35(c) are cross-sectional views illustrating respective process steps for forming the interconnection structure in the modified example of the sixth embodiment.

Figure 36 is a plan view illustrating a positional relationship between the openings of a mask pattern for forming

wiring grooves and the openings of a second resist pattern for forming contact holes in the modified example of the fifth embodiment.

Figure **37(a)** illustrates respective positional relationships between the mask pattern and the second resist pattern and between a first metal interconnect and an associated contact in the modified example of the fifth embodiment; and

Figure **37(b)** illustrates respective positional relationships between the mask pattern and the second resist pattern and between a first metal interconnect and an associated contact in the fifth embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

EMBODIMENT 1

Hereinafter, an exemplary method for forming an interconnection structure according to the first embodiment of the present invention will be described with reference to Figures **1(a)** through **1(c)**, Figures **2(a)** through **2(c)** and Figures **3(a)** through **3(c)**.

First, as shown in Figure **1(a)**, a silicon nitride film **102** is formed over first metal interconnects **101** formed on a semiconductor substrate **100**. The silicon nitride film **102** is formed to be 50 nm thick, for example, and used to protect the first metal interconnects **101** during a subsequent etching process step. Thereafter, a first organic film **103** (first in-

sulating film), mainly composed of an organic component, is formed to be 1 μm thick, for example, on the silicon nitride film **102**. Next, an organic-containing silicon dioxide film **104** (second insulating film), containing an organic component in silicon dioxide, is formed to be 50 nm thick, for example, on the first organic film **103**. Then, a second organic film **105** (third insulating film), mainly composed of an organic component, is formed to be 400 nm thick, for example, on the organic-containing silicon dioxide film **104**. And a titanium nitride film **106** is formed to be 50 nm thick, for example, on the second organic film **105**.

The first and second organic films **103** and **105** may be deposited by any arbitrary technique. For example, these films **103** and **105** may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic films **103** and **105**.

Moreover, the first organic film **103** may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin and organic silane such as hexamethyl disiloxane, arylalkoxy silane or alkylalkoxy silane. In such a case, an organic/inorganic hybrid film can be obtained.

Similarly, the organic-containing silicon dioxide film **104** may also be deposited by any arbitrary technique. For

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instance, the film **104** may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. In such a case, an organic-containing silicon dioxide film **104**, having a structure in which a phenyl group bonded to a silicon atom is introduced into silicon dioxide, can be obtained.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films **103** and **105** and the organic-containing silicon dioxide film **104**, i.e., a film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **106**.

Next, as shown in Figure **1(b)**, a first resist pattern **107**, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film **106**. Thereafter, the titanium nitride film **106** is dry-etched using the first resist pattern **107** as a mask, thereby forming a mask pattern **108** out of the titanium nitride film **106** as shown in Figure **1(c)**.

Subsequently, a second resist pattern **109**, having openings for forming contact holes, is formed by lithography on the second organic film **105** without removing the first resist pattern **107**. Then, the second organic film **105** is dry-etched, thereby forming a patterned second organic film **105A** having the openings for forming contact holes as shown in Figure **2(a)**. In this case, since the second organic film **105** and the first

and second resist patterns **107** and **109** are all mainly composed of organic components, the second organic film **105** is etched at a substantially equal rate to that of the first and second resist patterns **107** and **109**. Thus, when the second organic film **105** is dry-etched, the first and second resist patterns **107** and **109** are also removed simultaneously.

It should be noted that part of the second resist pattern **109** may be left in the process step of dry-etching the second organic film **105**. This is because the residual second resist pattern **109** can be removed during a subsequent process step of forming wiring grooves **111** in the patterned second organic film **105A** (see Figure **2(c)**).

Then, the organic-containing silicon dioxide film **104** is dry-etched using the patterned second organic film **105A** as a mask, thereby forming a patterned organic-containing silicon dioxide film **104A** having the openings for forming contact holes as shown in Figure **2(b)**. In this process step, by selecting such etching conditions that the organic-containing silicon dioxide film **104** is etched at a rate higher than that of the patterned second organic film **105A**, it is possible to prevent the patterned second organic film **105A** from being erroneously etched.

Next, the patterned second organic film **105A** is dry-etched using the mask pattern **108** as a mask, thereby forming the wiring grooves **111** in the patterned second organic film

105A as shown in Figure 2(c). At the same time, the first organic film 103 is also dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned first organic film 103A having the contact holes as shown in Figure 2(c).

Subsequently, the silicon nitride film 102 is dry-etched using the patterned organic-containing silicon dioxide film 104A as a mask, thereby forming a patterned silicon nitride film 102A and exposing the first metal interconnects 101 within the contact holes 110 as shown in Figure 3(a).

Then, as shown in Figure 3(b), an adhesion layer 112, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes 110 and the wiring grooves 111. Thereafter, a metal film 113 is deposited over the entire surface of the substrate to completely fill in the contact holes 110 and the wiring grooves 111. In this embodiment, the metal film 113 may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film 113 may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in Figure 3(c), respective portions of the adhesion layer 112, the metal film 113 and the mask pattern 108, which are deposited on the patterned second organic film 105A, are removed by a CMP technique, for example. As a

result, second metal interconnects **114** and contacts **115**, connecting the first and second metal interconnects **101** and **114**, are formed out of the metal film **113**.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **114** through the same process steps as those described above.

In the first embodiment, the organic-containing silicon dioxide film **104** is formed by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. Accordingly, the film **104** has a structure in which a phenyl group (i.e., an exemplary organic group), bonded to a silicon atom, is introduced into silicon dioxide. Thus, the film **104** can be processed as well as a conventional CVD oxide film, and the relative dielectric constant of the film **104** is as low as that of the conventional CVD oxide film. In addition, the film **104** can adhere strongly to organic film, oxide film and metal film.

After the mask pattern **108** has been formed out of the titanium nitride film **106**, the second resist pattern **109** is formed without removing the first resist pattern **107**, and the first and second resist patterns **107** and **109** are removed while the second organic film **105** is dry-etched. Thus, it is no longer necessary to ash and remove the first and second resist patterns **107** and **109** with oxygen plasma. That is to

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say, it is possible to prevent the second organic film **105** from being damaged during the step of ashing and removing a resist pattern. Accordingly, although the second organic film **105** with a low relative dielectric constant is used as an interlevel insulating film, an ordinary resist application process is applicable to this embodiment.

Moreover, the wiring grooves **111** are formed by dry-etching the patterned second organic film **105A** using the mask pattern **108** as a mask and using the patterned organic-containing silicon dioxide film **104A** as an etch stopper. Accordingly, the depth of the wiring grooves **111** matches with the thickness of the second organic film **105**. That is to say, the depth of the wiring grooves **111** can be defined by self-alignment.

Hereinafter, problems caused by the misalignment of the second resist pattern **109** with the first resist pattern **107** and the measured taken to solve the problems will be described.

First, it will be described with reference to Figures **4(a)** through **4(c)**, Figures **5(a)** through **5(c)** and Figures **6(a)** through **6(c)** what problems are caused if the second resist pattern **109** has misaligned.

As in the first embodiment, a silicon nitride film **102** is first formed to be 50 nm thick, for example, over first metal interconnects **101** formed on a semiconductor substrate

100 as shown in Figure 4(a). Thereafter, a first organic film 103, mainly composed of an organic component, is formed to be 1 μm thick, for example, on the silicon nitride film 102.

Next, an organic-containing silicon dioxide film 104, containing an organic component in silicon dioxide, is formed to be 50 nm thick, for example, on the first organic film 103. Then, a second organic film 105, mainly composed of an organic component, is formed to be 400 nm thick, for example, on the organic-containing silicon dioxide film 104. And a titanium nitride film 106 is formed to be 50 nm thick, for example, on the second organic film 105.

Next, as shown in Figure 4(b), a first resist pattern 107, having openings for forming wiring grooves, is formed on the titanium nitride film 106. Thereafter, the titanium nitride film 106 is dry-etched using the first resist pattern 107 as a mask, thereby forming a mask pattern 108 out of the titanium nitride film 106 as shown in Figure 4(c).

Subsequently, a second resist pattern 109, having openings for forming contact holes, is formed on the second organic film 105 without removing the first resist pattern 107. As can be seen if Figures 5(a) and 1(c) are compared with each other, the second resist pattern 109 has misaligned with the first resist pattern 107 in this case.

Then, the second organic film 105 is dry-etched, thereby forming a patterned second organic film 105A having the open-

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ings for forming contact holes as shown in Figure **5(a)**. As in the first embodiment, since the second organic film **105** and the first and second resist patterns **107** and **109** are all mainly composed of organic components, the first and second resist patterns **107** and **109** are removed simultaneously with the dry-etching of the second organic film **105**. In this case, since the second resist pattern **109** has misaligned with the first resist pattern **107**, the diameter of the openings for forming contact holes, which are provided in the second organic film **105A**, is smaller than desired.

Then, the organic-containing silicon dioxide film **104** is dry-etched using the patterned second organic film **105A** as a mask, thereby forming a patterned organic-containing silicon dioxide film **104A** having the openings for forming contact holes as shown in Figure **5(c)**.

Next, the patterned second organic film **105A** is dry-etched using the mask pattern **108** as a mask, thereby forming the wiring grooves **111** in the patterned second organic film **105A** as shown in Figure **6(a)**. At the same time, the first organic film **103** is also dry-etched using the patterned organic-containing silicon dioxide film **104A** as a mask, thereby forming a patterned first organic film **103A** having the contact holes **110** as shown in Figure **6(a)**. Subsequently, the silicon nitride film **102** is dry-etched using the patterned organic-containing silicon dioxide film **104A** as a mask, thereby form-

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ing a patterned silicon nitride film **102A** and exposing the first metal interconnects **101** within the contact holes **110** as shown in Figure **6(b)**.

Then, an adhesion layer **112**, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **110** and the wiring grooves **111**. Thereafter, a metal film is deposited over the entire surface of the substrate and respective portions of the adhesion layer **112**, the metal film and the mask pattern **108**, which are deposited on the patterned second organic film **105A**, are removed by a CMP technique, for example. As a result, second metal interconnects **114** are certainly formed. However, since the diameter of the contact holes **110** is smaller than desired, the contact holes **110** cannot be completely filled in with the metal film, and the first and second metal interconnects **101** and **112** cannot be connected to each other, resulting in a contact failure.

Next, it will be described with reference to Figures **7(a)** through **7(c)** and Figures **8(a)** through **8(c)** what measures should be taken to solve the problems caused by the misalignment of the second resist pattern **109**.

First, a second resist pattern **109**, having openings for forming contact holes, is formed through the same process steps as those described with reference to Figures **4(a)** through **4(c)** and Figure **5(a)**. In this case, the second re-

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sist pattern **109** has also misaligned with the first resist pattern **107** (see Figure **5(a)**).

Thus, as shown in Figure **7(a)**, the first resist pattern **107** and the mask pattern **108** are dry-etched using the second resist pattern **109** as a mask. In this manner, portions of the first resist pattern **107**, not overlapping with the second resist pattern **109**, are removed and each opening of the mask pattern **108** is expanded to be equal to or larger than each opening for forming wiring grooves or each opening for forming contact holes. As a result, the pattern for the openings of the second resist pattern for forming contact holes **109** can be transferred to the first resist pattern **107** and the mask pattern **108**.

Then, the second organic film **105** is dry-etched, thereby forming a patterned second organic film **105A** having the openings for forming contact holes as shown in Figure **7(b)**. In this case, since the second organic film **105** and the first and second resist patterns **107** and **109** are all mainly composed of organic components, the first and second resist patterns **107** and **109** are removed simultaneously with the dry-etching of the second organic film **105**.

Then, the organic-containing silicon dioxide film **104** is dry-etched using the patterned second organic film **105A** as a mask, thereby forming a patterned organic-containing silicon dioxide film **104A** having the openings for forming contact

holes as shown in Figure 7(c).

As described above, the second resist pattern **109** has misaligned with the first resist pattern **107**. However, in this case, the pattern for the openings of the second resist pattern for forming contact holes **109** has been successfully transferred to the first resist pattern **107** and the mask pattern **108**. Thus, the diameter of the openings for forming contact holes, which have been formed in the patterned second organic film **105A** and the patterned organic-containing silicon dioxide film **104A**, is a predetermined size.

Next, the patterned second organic film **105A** is dry-etched using the mask pattern **108** as a mask, thereby forming the wiring grooves **111** in the patterned second organic film **105A** as shown in Figure **8(a)**. At the same time, the first organic film **103** is also dry-etched using the patterned organic-containing silicon dioxide film **104A** as a mask, thereby forming a patterned first organic film **103A** having the contact holes **110** as shown in Figure **8(a)**. Subsequently, the silicon nitride film **102** is dry-etched using the patterned organic-containing silicon dioxide film **104A** as a mask, thereby forming a patterned silicon nitride film **102A** and exposing the first metal interconnects **101** within the contact holes **110** as shown in Figure **8(b)**.

Then, an adhesion layer **112**, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall

faces of the contact holes **110** and the wiring grooves **111**. Thereafter, a metal film is deposited over the entire surface of the substrate and respective portions of the adhesion layer **112**, the metal film and the mask pattern **108**, which are deposited on the patterned second organic film **105A**, are removed by a CMP technique, for example. As a result, second metal interconnects **114** and contacts **115** are formed out of the titanium nitride film **112** and the metal film as shown in Figure **8(c)**.

EMBODIMENT 2

Next, an exemplary method for forming an interconnection structure according to the second embodiment of the present invention will be described with reference to Figures **9(a)** through **9(c)**, Figures **10(a)** through **10(c)** and Figures **11(a)** through **11(c)**.

First, as shown in Figure **9(a)**, a silicon nitride film **202** is formed to be 50 nm thick, for example, over first metal interconnects **201** formed on a semiconductor substrate **200**. Thereafter, a first organic film **203** (first insulating film), mainly composed of an organic component, is formed to be 1 μm thick, for example, on the silicon nitride film **202**. Next, an organic-containing silicon dioxide film **204** (second insulating film), containing an organic component in silicon dioxide, is formed to be 50 nm thick, for example, on the fir-

st organic film **203**. Then, a second organic film **205** (third insulating film), mainly composed of an organic component, is formed to be 400 nm thick, for example, on the organic-containing silicon dioxide film **204**. And a titanium nitride film **206** is formed to be 50 nm thick, for example, on the second organic film **205**.

The first and second organic films **203** and **205** may be deposited by any arbitrary technique. For example, these films **203** and **205** may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic films **203** and **205**.

Similarly, the organic-containing silicon dioxide film **204** may also be deposited by any arbitrary technique. For instance, the film **204** may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films **203** and **205** and the organic-containing silicon dioxide film **204**, i.e., a film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **206**.

Next, as shown in Figure **9(b)**, a first resist pattern **207**, having openings for forming wiring grooves, is formed by

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lithography on the titanium nitride film **206**. Thereafter, the titanium nitride film **206** is dry-etched using the first resist pattern **207** as a mask, thereby forming a mask pattern **208** out of the titanium nitride film **206** as shown in Figure **9(c)**.

Subsequently, a second resist pattern **209**, having openings for forming contact holes, is formed by lithography on the second organic film **205** without removing the first resist pattern **207**. Then, the second organic film **205** is dry-etched, thereby forming a patterned second organic film **205A** having the openings for forming contact holes as shown in Figure **10(a)**. In this case, since the second organic film **205** and the first and second resist patterns **207** and **209** are all mainly composed of organic components, the second organic film **205** is etched at a rate substantially equal to that of the first and second resist patterns **207** and **209**. Accordingly, when the second organic film **205** is dry-etched, the first and second resist patterns **207** and **209** are also removed simultaneously.

If the second resist pattern **209** may have been misaligned with the first resist pattern **207**, then the first resist pattern **207** and the mask pattern **208** should be dry-etched using the second resist pattern **209** as a mask. In this manner, parts of the first resist pattern **207**, not overlapping with the second resist pattern **209**, are removed and the openings of the mask pattern **208** are expanded to be equal to or larger than the openings for forming wiring grooves and

contact holes as described in the first embodiment.

Then, the organic-containing silicon dioxide film **204** is dry-etched using the patterned second organic film **205A** as a mask, thereby forming a patterned organic-containing silicon dioxide film **204A** having the openings for forming contact holes as shown in Figure **10(b)**. Next, the patterned second organic film **205A** is dry-etched using the mask pattern **208** as a mask, thereby forming the wiring grooves **211** in the patterned second organic film **205A** as shown in Figure **10(c)**. At the same time, the first organic film **203** is also dry-etched using the patterned organic-containing silicon dioxide film **204A** as a mask, thereby forming a patterned first organic film **203A** having the contact holes **210** as also shown in Figure **10(c)**.

Subsequently, the silicon nitride film **202** is dry-etched using the patterned organic-containing silicon dioxide film **204A** as a mask, thereby forming a patterned silicon nitride film **202A** and exposing the first metal interconnects **201** within the contact holes **210** as shown in Figure **11(a)**.

Then, the patterned first and second organic films **203A** and **205A** are subjected to plasma processing using ammonium gas. As a result, as shown in Figure **11(b)**, an adhesion layer **212**, including amino and amide groups, is deposited on the wall faces of the patterned first organic film **203A** exposed inside the contact holes **210** and on the wall faces of

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the patterned second organic film **205A** exposed inside the wiring grooves **211**. Thereafter, a metal film **213** is deposited over the entire surface of the substrate to completely fill in the contact holes **210** and the wiring grooves **211**. In this embodiment, the metal film **213** may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film **213** may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in Figure **11(c)**, respective portions of the metal film **213** and the mask pattern **208**, which are deposited on the patterned second organic film **205A**, are removed by a CMP technique, for example. As a result, second metal interconnects **214** and contacts **215** are formed out of the metal film **213**.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **214** through the same process steps as those described above.

EMBODIMENT 3

Next, an exemplary method for forming an interconnection structure according to the third embodiment of the present invention will be described with reference to Figures **12(a)** through **12(c)**, Figures **13(a)** through **13(c)** and Figures **14(a)**

through **14(c)**.

First, as shown in Figure **12(a)**, a silicon nitride film **302** is formed over first metal interconnects **301** formed on a semiconductor substrate **300**. The silicon nitride film **302** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **301** during a subsequent etching process step. Thereafter, a first organic-containing silicon dioxide film **303** (first insulating film), containing an organic component in silicon dioxide, is formed to be 1μm thick, for example, on the silicon nitride film **302**. Next, a low-dielectric-constant SOG film **304** (second insulating film), having a siloxane skeleton, is deposited to be 400 nm thick, for example, on the first organic-containing silicon dioxide film **303**. Then, a second organic-containing silicon dioxide film **305** (third insulating film), containing an organic component in silicon dioxide, is formed to be 50 nm thick, for example, on the low-dielectric-constant SOG film **304**. And a titanium nitride film **306** is formed to be 50 nm thick, for example, on the second organic-containing silicon dioxide film **305**.

The first and second organic-containing silicon dioxide films **303** and **305** may be deposited by any arbitrary technique. For example, these films **303** and **305** may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. Also, an HSQ film may be used as the low-

dielectric-constant SOG film **304** with a siloxane skeleton.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic-containing silicon dioxide films **303** and **305** and the low-dielectric-constant SOG film **304**, i.e., a film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **306**.

Next, as shown in Figure **12(b)**, a first resist pattern **307**, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film **306**. Thereafter, the titanium nitride film **306** is dry-etched using the first resist pattern **307** as a mask, thereby forming a mask pattern **308** out of the titanium nitride film **306** as shown in Figure **12(c)**.

Subsequently, as shown in Figure **13(a)**, the first resist pattern **307** is removed and then a second resist pattern **309**, having openings for forming contact holes, is formed on the second organic-containing silicon dioxide film **305**. Then, the second organic-containing silicon dioxide film **305**, the low-dielectric-constant SOG film **304** and the first organic-containing silicon dioxide film **303** are sequentially dry-etched using the second resist pattern **309** as a mask. As a result, a patterned second organic-containing silicon dioxide film **305A**, a patterned low-dielectric-constant SOG film **304A** and a patterned first organic-containing silicon dioxide film **303A** having contact holes **310** are formed as shown in Figure

13(b).

Next, as shown in Figure 13(c), the second resist pattern **309** is removed and the patterned second organic-containing silicon dioxide film **305A** is dry-etched using the mask pattern **308** as a mask, thereby forming openings for forming wiring grooves in the patterned second organic-containing silicon dioxide film **305A**. Thereafter, the patterned low-dielectric-constant SOG film **304A** is dry-etched using the mask pattern **308** and the patterned second organic-containing silicon dioxide film **305A** having the openings for wiring grooves as a mask, thereby forming the wiring grooves **311**. In forming the wiring grooves **311**, by selecting such etching conditions that the first organic-containing silicon dioxide film **303A** is etched at a rate sufficiently lower than that of the low-dielectric-constant SOG film **304A**, sufficient selectivity can be secured for the patterned first organic-containing silicon dioxide film **303A**. Accordingly, the depth of the wiring grooves **311** can be determined univalently at the sum of the thicknesses of the second organic-containing silicon dioxide film **305** and the low-dielectric-constant SOG film **304**.

If the second resist pattern **309** may have been misaligned with the first resist pattern **307**, the mask pattern **308** should be dry-etched using the second resist pattern **309** as a mask before the second organic-containing silicon dioxide film **305** is dry-etched using the second resist pattern

309 as a mask. That is to say, if the mask pattern **308** is partially exposed inside the openings of the second resist pattern **309** for forming contact holes because of the misalignment of the second resist pattern **309** with the first resist pattern **307**, then the mask pattern **308** is dry-etched using the second resist pattern **309** as a mask. In this manner, the openings of the mask pattern **308** are expanded to include the openings for forming wiring grooves and contact holes.

Subsequently, the silicon nitride film **302** is dry-etched using the patterned first organic-containing silicon dioxide film **303A** as a mask, thereby forming a patterned silicon nitride film **302A** and exposing the first metal interconnects **301** within the contact holes **310** as shown in Figure **14(a)**.

Then, as shown in Figure **14(b)**, an adhesion layer **312**, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **310** and the wiring grooves **311**. Thereafter, a metal film **313** is deposited over the entire surface of the substrate to completely fill in the contact holes **310** and the wiring grooves **311**. In this embodiment, the metal film **313** may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film **313** may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in Figure **14(c)**, respective portions of the adhesion layer **312**, the metal film **313** and the mask pattern **308**, which are deposited on the patterned second organic-containing silicon dioxide film **305A**, are removed by a CMP technique, for example. As a result, second metal interconnects **314** and contacts **315**, connecting the first and second metal interconnects **301** and **314**, are formed out of the metal film **313**.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **314** through the same process steps as those described above.

In the third embodiment, while the first resist pattern **307** is ashed and removed with oxygen plasma, the low-dielectric-constant SOG film **304** is not exposed to the oxygen plasma, because the second organic-containing silicon dioxide film **305** exists on the low-dielectric-constant SOG film **304**.

Also, in this embodiment, after the second organic-containing silicon dioxide film **305**, the low-dielectric-constant SOG film **304** and the first organic-containing silicon dioxide film **303** have been sequentially dry-etched using the second resist pattern **309** as a mask, the second resist pattern **309** is ashed and removed with oxygen plasma. Accordingly, the regions of the patterned low-dielectric-constant SOG film **304A**, which are exposed inside the openings for form-

ing contact holes, are exposed to oxygen plasma and damaged. However, the damaged layer, formed in the patterned low-dielectric-constant SOG film **304A**, can be removed when the wiring grooves **311** are formed in the patterned low-dielectric-constant SOG film **304A**, and does not have harmful effects on subsequent process steps.

Accordingly, the low-dielectric-constant SOG film **304** may be made of a material degradable with oxygen plasma. For example, in general, if an HSQ film is exposed to oxygen plasma, the Si-H bonds thereof are oxidized and the content of water and the relative dielectric constant thereof both increase to deteriorate the reliability and performance of the device. However, according to the third embodiment, the patterned low-dielectric-constant SOG film **304A**, in which the wiring grooves **311** have already been formed, is not affected by oxygen plasma. Thus, even if an HSQ film is used as an interlevel insulating film, the deterioration in reliability and performance of the device can be avoided.

MODIFIED EXAMPLE OF EMBODIMENT 3

Next, an exemplary method for forming an interconnection structure according to a modified example of the third embodiment of the present invention will be described with reference to Figures **15(a)** through **15(c)**, Figures **16(a)** through **16(c)** and Figures **17(a)** through **17(c)**.

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First, as shown in Figure **15(a)**, a silicon nitride film **352** is formed over first metal interconnects **351** formed on a semiconductor substrate **350**. The silicon nitride film **352** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **351** during a subsequent etching process step. Thereafter, a first silicon dioxide film **353** (first insulating film) is formed to be 1 μm thick, for example, on the silicon nitride film **352**. Next, an organic film **354** (second insulating film) is deposited to be 400 nm thick, for example, on the first silicon dioxide film **353**. Then, a second silicon dioxide film **355** (third insulating film) is formed to be 50 nm thick, for example, on the organic film **354**. And a titanium nitride film **356** is formed to be 50 nm thick, for example, on the second silicon dioxide film **355**.

The first and second silicon dioxide films **353** and **355** may be deposited by any arbitrary technique. For example, these films **353** and **355** may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane.

It should be noted that a thin film showing high etch selectivity with respect to the first and second silicon dioxide films **353** and **355** and the organic film **354**, i.e., a film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **356**.

Next, as shown in Figure **15(b)**, a first resist pattern **357**, having openings for forming wiring grooves, is formed by

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lithography on the titanium nitride film **356**. Thereafter, the titanium nitride film **356** is dry-etched using the first resist pattern **357** as a mask, thereby forming a mask pattern **358** out of the titanium nitride film **356** as shown in Figure **15(c)**.

Subsequently, as shown in Figure **16(a)**, the first resist pattern **357** is removed and then a second resist pattern **359**, having openings for forming contact holes, is formed on the second silicon dioxide film **355**. Then, the second silicon dioxide film **355** and the organic film **354** are sequentially dry-etched using the second resist pattern **359** as a mask, thereby forming a patterned second silicon dioxide film **355A** and a patterned organic film **354A** having openings **360** for forming contact holes as shown in Figure **16(b)**. In this case, the second resist pattern **359** is removed during the step of etching the organic film **354**.

Next, as shown in Figure **16(c)**, the first silicon dioxide film **353** is dry-etched using the patterned second silicon dioxide film **355A** and the patterned organic film **354A** as a mask, thereby forming a patterned first silicon dioxide film **353A** having contact holes **361**. In this etching process step, the mask pattern **358** is transferred to the patterned second silicon dioxide film **355A**. Accordingly, openings for forming wiring grooves are formed in the patterned second silicon dioxide film **355A**.

Thereafter, as shown in Figure **16(d)**, the patterned or-

ganic film **354A** is dry-etched using the mask pattern **358** and the patterned second silicon dioxide film **355A** having the openings for forming wiring grooves as a mask, thereby forming the wiring grooves **362**. In forming the wiring grooves **362**, by selecting such etching conditions that the first silicon dioxide film **353A** is etched at a rate sufficiently lower than that of the organic film **354A**, sufficient selectivity can be secured for the patterned first silicon dioxide film **353A**. Accordingly, the depth of the wiring grooves **362** can be determined univalently at the sum of the thicknesses of the second silicon dioxide film **355** and the organic film **354**.

If the second resist pattern **359** may have been misaligned with the first resist pattern **357**, then the mask pattern **358** should be dry-etched using the second resist pattern **359** as a mask before the second silicon dioxide film **355** is dry-etched using the second resist pattern **359** as a mask. That is to say, if the mask pattern **358** is partially exposed inside the openings of the second resist pattern **359** for forming contact holes because of the misalignment of the second resist pattern **359** with the first resist pattern **357**, then the mask pattern **358** is dry-etched using the second resist pattern **359** as a mask. In this manner, the openings of the mask pattern **358** are expanded to include the openings for forming wiring grooves and contact holes.

Subsequently, the silicon nitride film **352** is dry-etched

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using the patterned first silicon dioxide film **353A** as a mask, thereby forming a patterned silicon nitride film **352A** and exposing the first metal interconnects **351** within the contact holes **361** as shown in Figure **17(a)**.

Then, as shown in Figure **17(b)**, an adhesion layer **363**, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **361** and the wiring grooves **362**. Thereafter, a metal film **364** is deposited over the entire surface of the substrate to completely fill in the contact holes **361** and the wiring grooves **362**. In this embodiment, the metal film **364** may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film **364** may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in Figure **17(c)**, respective portions of the adhesion layer **363**, the metal film **364** and the mask pattern **358**, which are deposited on the patterned second silicon dioxide film **355A**, are removed by a CMP technique, for example. As a result, second metal interconnects **365** and contacts **366**, connecting the first and second metal interconnects **351** and **365**, are formed out of the metal film **364**.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **365**

through the same process steps as those described above.

In this modified example of the third embodiment, while the first resist pattern **357** is ashed and removed by oxygen plasma, the organic film **354** is not exposed to the oxygen plasma, because the second silicon dioxide film **355** exists on the organic film **354**.

Also, in this example, the second resist pattern **359** is removed while the second silicon dioxide film **355** and the organic film **354** are dry-etched using the second resist pattern **359** as a mask. Accordingly, since there is no need to ash and remove the second resist pattern **359** with oxygen plasma, the organic film **354** is not exposed to oxygen plasma.

EMBODIMENT 4

Next, an exemplary method for forming an interconnection structure according to the fourth embodiment of the present invention will be described with reference to Figures **18(a)** through **18(c)**, Figures **19(a)** through **19(c)** and Figures **20(a)** through **20(c)**.

First, as shown in Figure **18(a)**, a silicon nitride film **402** is formed over first metal interconnects **401** formed on a semiconductor substrate **400**. The silicon nitride film **402** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **401** during a subsequent etching process step. Thereafter, a first low-dielectric-constant

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SOG film **403** (first insulating film), having a siloxane skeleton, is formed to be 1 μm thick, for example, on the silicon nitride film **402**. Next, an organic-containing silicon dioxide film **404** (second insulating film), containing an organic component in silicon dioxide, is deposited to be 50 nm thick, for example, on the first low-dielectric-constant SOG film **403**. Then, a second low-dielectric-constant SOG film **405** (third insulating film), having a siloxane skeleton, is formed to be 400 nm thick, for example, on the organic-containing silicon dioxide film **404**. And a titanium nitride film **406** is formed to be 50 nm thick, for example, on the second low-dielectric-constant SOG film **405**.

The first and second low-dielectric-constant SOG films **403** and **405** may be HSQ films, for example. The organic-containing silicon dioxide film **404** may be deposited by any arbitrary technique. For example, the film **404** may be deposited by a CVD process using a reactive gas mainly composed of phenyltrimethoxy silane. Then, an organic-containing silicon dioxide film **404**, having a structure in which a phenyl group bonded to a silicon atom is introduced into silicon dioxide, can be obtained.

It should be noted that a thin film showing high etch selectivity with respect to the first and second low-dielectric-constant SOG films **403** and **405** and the organic-containing silicon dioxide film **404**, i.e., a film etched at a

sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **406**.

Next, as shown in Figure **18(b)**, a first resist pattern **407**, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film **406**. Thereafter, the titanium nitride film **406** is dry-etched using the first resist pattern **407** as a mask, thereby forming a mask pattern **408** out of the titanium nitride film **406** as shown in Figure **18(c)**.

Subsequently, a second resist pattern **409**, having openings for forming contact holes, is formed by lithography on the second low-dielectric-constant SOG film **405** without removing the first resist pattern **407**. Then, the second low-dielectric-constant SOG film **405** and the organic-containing silicon dioxide film **404** are sequentially dry-etched using the second resist pattern **409** as a mask, thereby forming a patterned second low-dielectric-constant SOG film **405A** and a patterned organic-containing silicon dioxide film **404A** as shown in Figure **19(a)**.

Next, the first and second resist patterns **407** and **409** are ashed and removed with oxygen plasma. As a result, a damaged layer **410** is unintentionally formed in respective portions of the patterned second low-dielectric-constant SOG film **405A** and the first low-dielectric-constant SOG film **403**, which are exposed inside the openings for forming contact holes, as shown in Figure **19(b)**.

Then, the patterned second low-dielectric-constant SOG film **405A** is dry-etched using the mask pattern **408** as a mask, thereby forming wiring grooves **412** in the patterned second low-dielectric-constant SOG film **405A** as shown in Figure **19(c)**. At the same time, the first low-dielectric-constant SOG film **403** is dry-etched using the patterned organic-containing silicon dioxide film **404A** as a mask, thereby forming a patterned first low-dielectric-constant SOG film **403A** having contact holes **411** as shown in Figure **19(c)**. By performing this dry-etching process step, the damaged layer **410** can be removed from the patterned second low-dielectric-constant SOG films **405A** and the first low-dielectric-constant SOG film **403**.

Subsequently, the silicon nitride film **402** is dry-etched using the patterned organic-containing silicon dioxide film **404A** as a mask, thereby forming a patterned silicon nitride film **402A** and exposing the first metal interconnects **401** within the contact holes **411** as shown in Figure **20(a)**.

Then, as shown in Figure **20(b)**, an adhesion layer **413**, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **411** and the wiring grooves **412**. Thereafter, a metal film **414** is deposited over the entire surface of the substrate to completely fill in the contact holes **411** and the wiring grooves **412**. In this embodiment, the metal film **414** may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel,

cobalt, tungsten, or an alloy thereof may be used. Also, the metal film **414** may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed.

Finally, as shown in Figure **20(c)**, respective portions of the adhesion layer **413**, the metal film **414** and the mask pattern **408**, which are deposited on the patterned second low-dielectric-constant SOG film **405A**, are removed by a CMP technique, for example. As a result, second metal interconnects **415** and contacts **416**, connecting the first and second metal interconnects **401** and **415**, are formed out of the metal film **414**.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **415** through the same process steps as those described above.

In the fourth embodiment, while the first and second resist patterns **407** and **409** are ashed and removed with oxygen plasma, a damaged layer **410** is formed in the first low-dielectric-constant SOG film **403** and the patterned second low-dielectric-constant SOG film **405A**. But the damaged layer **410** can be removed while the contact holes **411** and the wiring grooves **412** are formed.

Accordingly, the first and second low-dielectric-constant SOG films **403** and **405** may be made of a material degradable with oxygen plasma. For example, in general, if an

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HSQ film is exposed to oxygen plasma, Si-H bonds thereof are oxidized and the content of water and the relative dielectric constant thereof both increase to deteriorate the reliability and performance of the device. However, according to the fourth embodiment, the patterned first low-dielectric-constant SOG film **403A**, in which the contact holes **411** have already been formed, and the patterned second low-dielectric-constant SOG film **405A**, in which the wiring grooves **412** have already been formed, are not affected by oxygen plasma any more. Thus, even if an HSQ film is used as an interlevel insulating film, the deterioration in reliability and performance of the device can be avoided.

EMBODIMENT 5

Next, an exemplary method for forming an interconnection structure according to the fifth embodiment of the present invention will be described with reference to Figures **21(a)** through **21(c)**, Figures **22(a)** through **22(c)** and Figures **23(a)** through **23(d)**.

First, as shown in Figure **21(a)**, a silicon nitride film **502** is formed over first metal interconnects **501** formed on a semiconductor substrate **500**. The silicon nitride film **502** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **501** during a subsequent etching process step. Thereafter, a first organic film **503** (first

insulating film), mainly composed of an organic component, is deposited to be 400 nm thick, for example, on the silicon nitride film **502**. Then, a first silicon dioxide film **504** (second insulating film) is deposited to be 100 nm thick, for example, on the first organic film **503**. Subsequently, a second organic film **505** (third insulating film), mainly composed of an organic component, is deposited to be 300 nm thick, for example, on the first silicon dioxide film **504**. Next, a second silicon dioxide film **506** (fourth insulating film) is deposited to be 200 nm thick, for example, on the second organic film **505**. And a titanium nitride film **507** (thin film) is deposited to be 50 nm thick, for example, on the second silicon dioxide film **506**.

The first and second organic films **503** and **505** may be deposited by any arbitrary technique. For example, these films **503** and **505** may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic films **503** and **505**. More specifically, the organic films **503** and **505** may be made of polytetrafluoroethylene, oxygen-containing polytetrafluoroethylene, polyimide fluoride or polyaryl ether.

The first and second silicon dioxide films **504** and **506** may also be deposited by any arbitrary technique. For exam-

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ple, these films **504** and **506** may be deposited by a plasma CVD process.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films **503** and **505** and the first and second silicon dioxide films **504** and **506**, i.e., a thin film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **507**.

Next, as shown in Figure **21(b)**, a first resist pattern **508**, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film **507**. Thereafter, the titanium nitride film **507** is dry-etched using the first resist pattern **508** as a mask, thereby forming a mask pattern **509**, having openings for forming wiring grooves, out of the titanium nitride film **507** as shown in Figure **21(c)**.

Subsequently, as shown in Figure **22(a)**, the first resist pattern **508** is removed by oxygen plasma, for example. In this case, even if the first resist pattern **508** is ashed and removed using oxygen plasma, the quality of the second organic film **505** does not degrade, because the second silicon dioxide film **506** exists on the second organic film **505** mainly composed of an organic component.

Then, as shown in Figure **22(b)**, a second resist pattern **510**, having openings for forming contact holes, is formed by lithography on the mask pattern **509**. Thereafter, the second

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silicon dioxide film **506** is dry-etched using the second resist pattern **510** and the mask pattern **509** as a mask, thereby forming a patterned second silicon dioxide film **506A** having openings for forming contact holes as shown in Figure **22(c)**.

Next, the second organic film **505** is dry-etched using the patterned second silicon dioxide film **506A** as a mask, thereby forming a patterned second organic film **505A** having openings for forming contact holes as shown in Figure **23(a)**. In this case, the second organic film **505** and the second resist pattern **510** are both mainly composed of organic components, the second organic film **505** is etched at a substantially equal rate to that of the second resist pattern **510**. Thus, when the second organic film **505** is dry-etched, the second resist pattern **510** is also removed simultaneously. The patterned second silicon dioxide film **506A** functions as an etch stopper during dry-etching the second resist pattern **510**.

It should be noted that part of the second resist pattern **510** may be left in the process step of dry-etching the second organic film **505**. This is because the residual second resist pattern **510** can be removed during a subsequent process step of dry-etching the first organic film **503** (see Figure **23(c)**).

Thereafter, the patterned second silicon dioxide film **506A** and the first silicon dioxide film **504** are dry-etched using the mask pattern **509** and the patterned second organic film

505A as respective masks, thereby forming a patterned second silicon dioxide film **506B** having openings for forming wiring grooves and a patterned first silicon dioxide film **504A** having openings for forming contact holes as shown in Figure **23(b)**.

Then, the patterned second organic film **505A** and the first organic film **503** are dry-etched using the mask pattern **509** and the patterned first silicon dioxide film **504A** as respective masks, thereby forming a patterned second organic film **505B** having wiring grooves **511** and a patterned first organic film **503A** having contact holes **512** as shown in Figure **23(c)**.

Subsequently, the silicon nitride film **502** is dry-etched using the patterned first silicon dioxide film **504A** as a mask, thereby forming a patterned silicon nitride film **502A** (see Figure **23(d)**) and exposing the first metal interconnects **501** within the contact holes **512**. Then, although not shown, an adhesion layer, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **512** and the wiring grooves **511** as in the first embodiment. Thereafter, a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes **512** and the wiring grooves **511**. In this embodiment, the metal film may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film may be deposited by any arbitrary technique. For instance, plating,

CVD or sputtering may be employed. Finally, respective portions of the adhesion layer, the metal film and the mask pattern **509**, which are deposited on the patterned second silicon dioxide film **506B**, are removed by a CMP technique, for example. As a result, second metal interconnects **513** and contacts **514**, connecting the first and second metal interconnects **501** and **513** together, are formed as shown in Figure **23(d)**.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **513** through the same process steps as those described above.

In the fifth embodiment, while the first resist pattern **508** is being removed by oxygen plasma, for example, the quality of the second organic film **505** does not degrade. This is because the second silicon dioxide film **506** exists on the second organic film **505**, which is likely to be damaged by oxygen plasma.

Also, in this embodiment, the first silicon dioxide film **504** functions as an etch stopper during dry-etching the second organic film **505**. Accordingly, it is possible to prevent the quality of the first organic film **503** from being degraded.

MODIFIED EXAMPLE OF EMBODIMENT 5

Next, a method for forming an interconnection structure

according to a modified example of the fifth embodiment will be described with reference to Figures **24(a)** through **24(c)**, Figures **25(a)** through **25(c)**, Figures **26(a)** through **26(d)**, Figures **27(a)** and **27(b)**, Figures **28(a)** and **28(b)** and Figures **29(a)** and **29(b)**.

First, as shown in Figure **24(a)**, a silicon nitride film **552** is formed over first metal interconnects **551** formed on a semiconductor substrate **550**. The silicon nitride film **552** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **551** during a subsequent etching process step. Thereafter, a first organic film **553** (first insulating film), mainly composed of an organic component, is deposited to be 400 nm thick, for example, on the silicon nitride film **552**. Then, a first silicon dioxide film **554** (second insulating film) is formed to be 100 nm thick, for example, on the first organic film **553**. Subsequently, a second organic film **555** (third insulating film), mainly composed of an organic component, is deposited to be 300 nm thick, for example, on the first silicon dioxide film **554**. Next, a second silicon dioxide film **556** (fourth insulating film) is deposited to be 200 nm thick, for example, on the second organic film **555**. And a titanium nitride film **557** is deposited to be 50 nm thick, for example, on the second silicon dioxide film **556**.

The first and second organic films **553** and **555** and the first and second silicon dioxide films **554** and **566** may be de-

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posited by any arbitrary technique as in the fifth embodiment. Also, a thin film showing high etch selectivity with respect to the first and second organic films **553** and **555** and the first and second silicon dioxide films **554** and **556** may be used instead of the titanium nitride film **557**.

Next, as shown in Figure **24(b)**, a first resist pattern **558**, having openings for forming wiring grooves, is formed on the titanium nitride film **557**. Thereafter, the titanium nitride film **557** is dry-etched using the first resist pattern **558** as a mask, thereby forming a mask pattern **559**, having openings for forming wiring grooves, out of the titanium nitride film **557** as shown in Figure **24(c)**.

Subsequently, as shown in Figures **25(a)** and **27(a)**, the first resist pattern **558** is removed. Then, a second resist pattern **560**, having openings for forming contact holes, is formed on the mask pattern **559** as shown in Figure **25(b)**. in this modified example of the fifth embodiment, the sizes of the openings of the second resist pattern **560** for forming contact holes are set larger than designed sizes of the contact holes in respective directions vertical and parallel to wiring grooves for forming second metal interconnects. The reason thereof will be described later.

Then, the second silicon dioxide film **556** is dry-etched using the second resist pattern **560** and the mask pattern **559** as a mask, thereby forming a patterned second silicon dioxide

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film **556A** having openings for forming contact holes as shown in Figures **25(c)** and **27(b)**.

As described above, the sizes of the openings of the second resist pattern **560** for forming contact holes are set larger than designed sizes of the contact holes in respective directions vertical and parallel to wiring grooves for forming second metal interconnects. Accordingly, even if the openings of the second resist pattern **560** for forming contact holes have misaligned with the openings of the mask pattern **559** for forming wiring grooves, the openings of the patterned second silicon dioxide film **556A** for forming contact holes can be formed to be self-aligned with the openings of the mask pattern **559** for forming wiring grooves. This is because the openings of the patterned second silicon dioxide film **556A** for forming contact holes are formed in respective regions where the openings of the second resist pattern **560** for forming contact holes overlap with corresponding openings of the mask pattern **559** for forming wiring grooves.

In addition, the size of the openings of the second resist pattern **560** for forming contact holes is also extended in the direction parallel to the wiring grooves for forming second metal interconnects. Thus, the contact area between contacts **564** to be formed later and second metal interconnects **563** (see Figure **26(d)**) expands. As a result, the contacts **564** can connect the first and second metal interconnects **551** and

563 together with a lot more certainty.

Next, the second organic film **555** is dry-etched using the patterned second silicon dioxide film **556A** as a mask, thereby forming a patterned second organic film **555A** having openings for forming contact holes as shown in Figures **26(a)** and **28(a)**. In this case, the second organic film **555** and the second resist pattern **560** are both mainly composed of organic components, the second organic film **555** is etched at a substantially equal rate to that of the second resist pattern **560**. Thus, when the second organic film **555** is dry-etched, the second resist pattern **560** is also removed simultaneously. It should be noted that part of the second resist pattern **560** may be left in the process step of dry-etching the second organic film **555**. This is because the residual second resist pattern **560** can be removed during a subsequent process step of dry-etching the first organic film **553** (see Figure **26(c)**).

Thereafter, the patterned second silicon dioxide film **556A** and the first silicon dioxide film **554** are dry-etched using the mask pattern **559** and the patterned second organic film **555A** as respective masks, thereby forming a patterned second silicon dioxide film **556B** having wiring grooves and a patterned first silicon dioxide film **554A** having openings for forming contact holes as shown in Figures **26(b)** and **28(b)**.

Then, the patterned second organic film **555A** is dry-etched using the mask pattern **559** and the patterned second

silicon dioxide film **556B** as a mask, and the first organic film **553** is dry-etched using the patterned first silicon dioxide film **554A** as a mask, thereby forming a patterned second organic film **555B** having wiring grooves **561** and a patterned first organic film **553A** having contact holes **562** as shown in Figures **26(c)** and **29(a)**.

Subsequently, the silicon nitride film **552** is dry-etched using the patterned first silicon dioxide film **554A** as a mask, thereby forming a patterned silicon nitride film **552A** (see Figure **26(d)**) having contact holes, and exposing the first metal interconnects **551** within the contact holes **562**. Then, although not shown, an adhesion layer, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **562** and the wiring grooves **561** as in the first embodiment. Thereafter, a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes **562** and the wiring grooves **561**. Finally, respective portions of the adhesion layer, the metal film and the mask pattern **559**, which are deposited on the patterned second silicon dioxide film **556B**, are removed by a CMP technique, for example. As a result, second metal interconnects **563** and contacts **564**, connecting the first and second metal interconnects **551** and **563** together, are formed as shown in Figures **26(d)** and **29(b)**.

It should be noted that a multilevel interconnection

structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **563** through the same process steps as those described above.

According to this modified example of the fifth embodiment, the sizes of the openings of the second resist pattern **560** for forming contact holes are set larger than designed sizes of the contact holes in respective directions vertical and parallel to the wiring grooves for forming the second metal interconnects. Thus, even if the openings of the second resist pattern **560** for forming contact holes have misaligned with the openings of the mask pattern **559** for forming wiring grooves, the openings of the patterned second silicon dioxide film **556A** for forming contact holes can be formed to be self-aligned with the openings of the mask pattern **559** for forming wiring grooves. This is because the openings of the patterned second silicon dioxide film **556A** for forming contact holes are formed in respective regions where the openings of the second resist pattern **560** for forming contact holes overlap with corresponding openings of the mask pattern **559** for forming wiring grooves. Accordingly, the connection between the contacts **564** and the second metal interconnects **563** is ensured.

In addition, the size of the openings of the second resist pattern **560** for forming contact holes is also extended in the direction parallel to the wiring grooves for forming the second metal interconnects. Thus, the contact area between

contacts **564** and the second metal interconnects **563** expands. As a result, the contacts **564** can connect the first and second metal interconnects **551** and **563** together with a lot more certainty.

Figure **36** illustrates a positional relationship between the openings of the mask pattern **559** for forming wiring grooves and those of the second resist pattern **560** for forming contact holes in this modified example of the fifth embodiment. As shown in Figure **36**, the size of the openings of the second resist pattern **560** for forming contact holes are larger than the designed size.

Figure **37(a)** illustrates respective positional relationships between the mask pattern **559** and the second resist pattern **560** and between a first metal interconnect **551** and a contact **564** in this modified example of the fifth embodiment. Specifically, the upper part of Figure **37(a)** illustrates a positional relationship between an opening of the mask pattern **559** for forming a wiring groove and an associated opening of the second resist pattern **560** for forming a contact hole. The middle part of Figure **37(a)** illustrates the cross section of the upper part taken along the line **A-A**. And the lower part of Figure **37(a)** illustrates a positional relationship between a first metal interconnect **551** and an associated contact **564**. Figure **37(b)** illustrates respective positional relationships between the mask pattern **509** and the second re-

sist pattern **510** and between a first metal interconnect **501** and a contact **514** in the fifth embodiment. Specifically, the upper part of Figure **37(b)** illustrates a positional relationship between an opening of the mask pattern **509** for forming a wiring groove and an associated opening of the second resist pattern **510** for forming a contact hole. The middle part of Figure **37(b)** illustrates the cross section of the upper part taken along the line **B-B**. And the lower part of Figure **37(b)** illustrates a positional relationship between a first metal interconnect **501** and an associated contact **514**.

Setting the size of an opening of the second resist pattern **510** for forming a contact hole at the designed size thereof as in the fifth embodiment, if the opening of the second resist pattern **510** for forming a contact hole has misaligned with an associated opening of the mask pattern **509** for forming a wiring groove, then the contact area (indicated by hatching) between the contact **514** and the first metal interconnect **501** greatly decreases as can be seen from Figure **37(b)**. In contrast, setting the size of an opening of the second resist pattern **560** for forming a contact hole larger than the designed size thereof as in this modified example of the fifth embodiment, even if the opening of the second resist pattern **560** for forming a contact hole has misaligned with an associated opening of the mask pattern **559** for forming a wiring groove, the contact area (indicated by hatching) between

the contact **564** and the first metal interconnect **551** does not decrease so much as can be seen from Figure **37(a)**.

EMBODIMENT 6

Next, an exemplary method for forming an interconnection structure according to the sixth embodiment of the present invention will be described with reference to Figures **30(a)** through **30(c)**, Figures **31(a)** through **31(c)** and Figures **32(a)** through **32(c)**.

First, as shown in Figure **30(a)**, a silicon nitride film **602** is formed over first metal interconnects **601** formed on a semiconductor substrate **600**. The silicon nitride film **602** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **601** during a subsequent etching process step. Thereafter, a first organic film **603** (first insulating film), mainly composed of an organic component, is deposited to be 400 nm thick, for example, on the silicon nitride film **602**. Then, a silicon dioxide film **604** (second insulating film) is deposited to be 100 nm thick, for example, on the first organic film **603**. Subsequently, a second organic film **605** (third insulating film), mainly composed of an organic component, is deposited to be 300 nm thick, for example, on the silicon dioxide film **604**. And a titanium nitride film **606** (thin film) is deposited to be 50 nm thick, for example, on the second organic film **605**.

The first and second organic films **603** and **605** may be deposited by any arbitrary technique. For example, these films **603** and **605** may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic films **603** and **605**. More specifically, the organic films **603** and **605** may be made of polytetrafluoroethylene, oxygen-containing polytetrafluoroethylene, polyimide fluoride or polyaryl ether.

The silicon dioxide film **604** may also be deposited by any arbitrary technique. For example, the film **604** may be deposited by a plasma CVD process.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films **603** and **605** and the silicon dioxide film **604**, i.e., a thin film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **606**.

Next, as shown in Figure **30(b)**, a first resist pattern **607**, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film **606**. Thereafter, the titanium nitride film **606** is dry-etched using the first resist pattern **607** as a mask, thereby forming a mask pattern **608**, having openings for forming wiring grooves, out of the titani-

um nitride film **606** as shown in Figure **30(c)**.

Subsequently, as shown in Figure **31(a)**, the first resist pattern **607** is removed using an organic parting agent, for example. In such a case, since the second organic film **605** is not exposed to oxygen plasma, the quality of the second organic film **605** does not degrade.

Then, as shown in Figure **31(b)**, a second resist pattern **609**, having openings for forming contact holes, is formed by lithography on the mask pattern **608**. Then, the second organic film **605** is dry-etched using the second resist pattern **609** and the mask pattern **608** as a mask, thereby forming a patterned second organic film **605A** having openings for forming contact holes as shown in Figure **31(c)**. In this case, the second organic film **605** and the second resist pattern **609** are both mainly composed of organic components, the second organic film **605** is etched at a substantially equal rate to that of the second resist pattern **609**. Thus, when the second organic film **605** is dry-etched, the second resist pattern **609** is also removed simultaneously.

It should be noted that part of the second resist pattern **609** may be left in the process step of dry-etching the second organic film **605**. This is because the residual second resist pattern **609** can be removed during a subsequent process step of dry-etching the first organic film **603** (see Figure **32(b)**).

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Thereafter, the silicon dioxide film **604** is dry-etched using the patterned second organic film **605A** as a mask, thereby forming a patterned silicon dioxide film **604A** having openings for forming contact holes as shown in Figure **32(a)**.

Then, the patterned second organic film **605A** and the first organic film **603** are dry-etched using the mask pattern **608** and the patterned silicon dioxide film **604A** as respective masks, thereby forming a patterned second organic film **605B** having wiring grooves **610** and a patterned first organic film **603A** having contact holes **611** as shown in Figure **32(b)**.

Subsequently, the patterned silicon dioxide film **604A** and the silicon nitride film **602** are dry-etched using the mask pattern **608** and the patterned first organic film **603A** as respective masks, thereby forming a patterned silicon dioxide film **604B** having wiring grooves (see Figure **32(c)**) and a patterned silicon nitride film **602A** having the contact holes (see Figure **32(c)**), and exposing the first metal interconnects **601** within the contact holes **611**. Then, although not shown, an adhesion layer, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **611** and the wiring grooves **610** as in the first embodiment. Thereafter, a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes **611** and the wiring grooves **610**. In this embodiment, the metal film may be made of any arbitrary metal. For example,

copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed. Finally, respective portions of the adhesion layer, the metal film and the mask pattern **608**, which are deposited on the patterned second organic film **605B**, are removed by a CMP technique, for example. As a result, second metal interconnects **612** and contacts **613**, connecting the first and second metal interconnects **601** and **612** together, are formed as shown in Figure **32(c)**.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **612** through the same process steps as those described above.

In the sixth embodiment, a patterned second organic film **605B**, having wiring grooves **610**, and a patterned first organic film **603A**, having contact holes **611**, are formed by a single dry-etching process using the mask pattern **608**, having the openings for forming wiring grooves, and the patterned silicon dioxide film **604A** as respective masks. That is to say, the wiring grooves **610** and the contact holes **611** can be formed during the same etching process step. Accordingly, a dual damascene structure can be formed with the increase in number of process steps suppressed.

Also, in the sixth embodiment, since the first resist

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pattern **607** is removed by an organic parting agent, for example, the quality of the second organic film **605** does not degrade.

Furthermore, in this embodiment, the silicon dioxide film **604** functions as an etch stopper during dry-etching the second organic film **605**. Accordingly, it is possible to prevent the quality of the first organic film **603** from being degraded.

MODIFIED EXAMPLE OF EMBODIMENT 6

Next, a method for forming an interconnection structure according to a modified example of the sixth embodiment will be described with reference to Figures **33(a)** through **33(c)**, Figures **34(a)** through **34(c)** and Figures **35(a)** through **35(c)**.

First, as shown in Figure **33(a)**, a silicon nitride film **652** is formed over first metal interconnects **651** formed on a semiconductor substrate **650**. The silicon nitride film **652** is formed to be 50 nm thick, for example, and to protect the first metal interconnects **651** during a subsequent etching process step. Thereafter, a first organic film **653** (first insulating film), mainly composed of an organic component, is deposited to be 400 nm thick, for example, on the silicon nitride film **652**. Then, a silicon dioxide film **654** (second insulating film) is deposited to be 100 nm thick, for example, on the first organic film **653**. Subsequently, a second organic

film **655** (third insulating film), mainly composed of an organic component, is deposited to be 300 nm thick, for example, on the silicon dioxide film **654**. And a titanium nitride film **656** (thin film) is deposited to be 50 nm thick, for example, on the second organic film **655**.

The first and second organic films **653** and **655** may be deposited by any arbitrary technique. For example, these films **653** and **655** may be deposited by a plasma CVD process using a reactive gas mainly composed of perfluorodecalin. Also, hydrocarbon films or fluorine-containing hydrocarbon films, formed by plasma CVD, coating or thermal CVD, may be used as the first and second organic films **653** and **655**. More specifically, the organic films **653** and **655** may be made of polytetrafluoroethylene, oxygen-containing polytetrafluoroethylene, polyimide fluoride or polyaryl ether.

The silicon dioxide film **654** may also be deposited by any arbitrary technique. For example, the film **654** may be deposited by a plasma CVD process.

It should be noted that a thin film showing high etch selectivity with respect to the first and second organic films **653** and **655** and the silicon dioxide film **654**, i.e., a thin film etched at a sufficiently low rate (e.g., silicon nitride film), may be used instead of the titanium nitride film **656**.

Next, as shown in Figure **33(b)**, a first resist pattern

657, having openings for forming wiring grooves, is formed by lithography on the titanium nitride film **656**. Thereafter, the titanium nitride film **656** is dry-etched using the first resist pattern **657** as a mask, thereby forming a mask pattern **658**, having openings for forming wiring grooves, out of the titanium nitride film **656** as shown in Figure **33(c)**.

Subsequently, as shown in Figure **34(a)**, the first resist pattern **657** is removed by an organic parting agent, for example. In such a case, since the second organic film **655** is not exposed to oxygen plasma, the quality of the second organic film **655** does not degrade.

Then, as shown in Figure **34(b)**, a second resist pattern **659**, having openings for forming contact holes, is formed by lithography on the mask pattern **658**. In this modified example of the sixth embodiment, the sizes of the openings of the second resist pattern **659** for forming contact holes are set larger than designed sizes of the contact holes in respective directions vertical and parallel to the wiring grooves for forming second metal interconnects. The reason thereof will be described later.

Next, the second organic film **655** is dry-etched using the second resist pattern **659** and the mask pattern **658** as a mask, thereby forming a patterned second organic film **655A** having openings for forming contact holes as shown in Figure **34(c)**. In this case, the second organic film **655** and the second re-

sist pattern **659** are both mainly composed of organic components, the second organic film **655** is etched at a substantially equal rate to that of the second resist pattern **659**. Thus, when the second organic film **655** is dry-etched, the second resist pattern **659** is also removed simultaneously. It should be noted that part of the second resist pattern **659** may be left in the process step of dry-etching the second organic film **655**. This is because the residual second resist pattern **659** can be removed during a subsequent process step of dry-etching the first organic film **653** (see Figure **35(b)**).

Thereafter, the silicon dioxide film **654** is dry-etched using the patterned second organic film **655A** as a mask, thereby forming a patterned second silicon dioxide film **654A** having openings for forming contact holes as shown in Figure **35(a)**.

Then, the patterned second organic film **655A** and the first organic film **653** are dry-etched using the mask pattern **658** and the patterned silicon dioxide film **654A** as respective masks, thereby forming a patterned second organic film **655B** having wiring grooves **660** and a patterned first organic film **653A** having contact holes **661** as shown in Figure **35(b)**.

Subsequently, the patterned silicon dioxide film **654A** and the silicon nitride film **652** are dry-etched using the mask pattern **658** and the patterned first organic film **653A** as respective masks, thereby forming a patterned silicon dioxide film **654B** having wiring grooves (see Figure **35(c)**) and a pat-

terned silicon nitride film **652A** having the contact holes (see Figure **35(c)**), and exposing the first metal interconnects **651** within the contact holes **661**. Then, although not shown, an adhesion layer, made of titanium nitride, is deposited to be 50 nm thick, for example, on the wall faces of the contact holes **661** and the wiring grooves **660** as in the first embodiment. Thereafter, a metal film is deposited over the entire surface of the substrate to completely fill in the contact holes **661** and the wiring grooves **660**. In this embodiment, the metal film may be made of any arbitrary metal. For example, copper, aluminum, gold, silver, nickel, cobalt, tungsten, or an alloy thereof may be used. Also, the metal film may be deposited by any arbitrary technique. For instance, plating, CVD or sputtering may be employed. Finally, respective portions of the adhesion layer, the metal film and the mask pattern **658**, which are deposited on the patterned second organic film **655B**, are removed by a CMP technique, for example. As a result, second metal interconnects **662** and contacts **663**, connecting the first and second metal interconnects **651** and **662** together, are formed as shown in Figure **35(c)**.

It should be noted that a multilevel interconnection structure may be formed by forming respective films, interconnects and contacts on the second metal interconnects **662** through the same process steps as those described above.

In this modified example of the sixth embodiment, the

sizes of the openings of the second resist pattern **659** for forming contact holes are set larger than designed sizes of the contact holes in respective directions vertical and parallel to the wiring grooves for forming the second metal interconnects. Accordingly, even if the openings of the second resist pattern **659** for forming contact holes have misaligned with the openings of the mask pattern **658** for forming wiring grooves, the openings of the patterned second organic film **655A** for forming contact holes can be formed to be self-aligned with the openings of the mask pattern **658** for forming wiring grooves. This is because the openings of the patterned second organic film **655A** for forming contact holes are formed in respective regions where the openings of the second resist pattern **659** for forming contact holes overlap with corresponding openings of the mask pattern **658** for forming wiring grooves. Accordingly, the connection between the contacts **663** and the second metal interconnects **662** is ensured.

In addition, the size of the openings of the second resist pattern **659** for forming contact holes is also extended in the direction parallel to the wiring grooves for forming second metal interconnects. Thus, the contact area between the contacts **663** and the second metal interconnects **662** expands. As a result, the contacts **663** can connect the first and second metal interconnects **651** and **662** together with a lot more certainty.

WHAT IS CLAIMED IS:

1. A method for forming an interconnection structure, comprising the steps of:

a) forming a first insulating film over lower-level metal interconnects;

b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;

c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

d) forming a thin film over the third insulating film;

e) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;

f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;

g) forming a second resist pattern on the third insulating film, the second resist pattern having openings for forming contact holes;

h) dry-etching the third insulating film under such conditions that the third insulating film and the first and second resist patterns are etched at a relatively high rate and that the second insulating film is etched at a relatively low

rate, thereby patterning the third insulating film to have the openings for forming contact holes and removing the first and second resist patterns either entirely or partially with respective lower parts thereof left;

i) dry-etching the second insulating film using the patterned third insulating film as a mask under such conditions that the second insulating film is etched at a relatively high rate and that the first and third insulating films are etched at a relatively low rate, thereby patterning the second insulating film to have the openings for forming contact holes;

j) dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and

k) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

2. The method of Claim 1, further comprising the step of forming a metal adhesion layer over part of the third insulat-

ing film exposed inside the wiring grooves and part of the first insulating film exposed inside the contact holes between the steps j) and k).

3. The method of Claim 1, wherein the third insulating film is mainly composed of an organic component.

4. The method of Claim 3, wherein the step c) includes forming the third insulating film by a CVD process using a reactive gas containing perfluorodecalin.

5. The method of Claim 3, wherein the first insulating film is mainly composed of an organic component.

6. The method of Claim 5, further comprising the step of forming an adhesion layer over part of the third insulating film exposed inside the wiring grooves and part of the first insulating film exposed inside the contact holes by a plasma process using a reactive gas containing nitrogen between the steps j) and k).

7. The method of Claim 3, wherein the step a) includes forming the first insulating film by a CVD process using a reactive gas containing perfluorodecalin.

8. A method for forming an interconnection structure, comprising the steps of:

a) forming a first insulating film over lower-level metal interconnects;

b) forming a second insulating film, having a different composition than that of the first insulating film, over the

first insulating film;

c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

d) forming a thin film over the third insulating film;

e) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;

f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;

g) forming a second resist pattern on the third insulating film, the second resist pattern having openings for forming contact holes;

h) dry-etching the third insulating film using the first and second resist patterns as a mask under such conditions that the third insulating film is etched at a relatively high rate and that the second insulating film and the first and second resist patterns are etched at a relatively low rate, thereby patterning the third insulating film to have the openings for forming contact holes;

i) dry-etching the second insulating film using the first and second resist patterns as a mask under such conditions that the second insulating film is etched at a relatively high rate and that the first and third insulating films and

the first and second resist patterns are etched at a relatively low rate, thereby patterning the second insulating film to have the openings for forming contact holes;

j) removing the first and second resist patterns;

k) dry-etching the third and first insulating films using the mask pattern and the patterned second insulating film as respective masks under such conditions that the first and third insulating films are etched at a relatively high rate and that the mask pattern and the second insulating film are etched at a relatively low rate, thereby forming wiring grooves and contact holes in the third and first insulating films, respectively; and

l) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

9. The method of Claim 8, wherein the third insulating film is a low-dielectric-constant SOG film with a siloxane skeleton.

10. A method for forming an interconnection structure, comprising the steps of:

a) forming a first insulating film over lower-level metal interconnects;

b) forming a second insulating film, having a different composition than that of the first insulating film, over the

first insulating film;

c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

d) forming a fourth insulating film, having a different composition than that of the third insulating film, over the third insulating film;

e) forming a thin film over the fourth insulating film;

f) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;

g) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;

h) removing the first resist pattern and then forming a second resist pattern on the fourth insulating film and the mask pattern, the second resist pattern having openings for forming contact holes;

i) dry-etching the fourth insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the fourth insulating film to have the openings for forming contact holes;

j) dry-etching the third insulating film using the patterned fourth insulating film as a mask, thereby patterning the third insulating film to have the openings for forming

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contact holes;

k) dry-etching the patterned fourth insulating film and the second insulating film using the mask pattern and the patterned third insulating film as respective masks, thereby forming wiring grooves in the patterned fourth insulating film and patterning the second insulating film to have the openings for forming contact holes;

l) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming the wiring grooves and the contact holes in the patterned third insulating film and the first insulating film, respectively; and

m) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

11. The method of Claim 10, wherein at least one of the first and third insulating films is mainly composed of an organic component.

12. The method of Claim 10, wherein a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.

13. A method for forming an interconnection structure, comprising the steps of:

a) forming a first insulating film over lower-level metal interconnects;

b) forming a second insulating film, having a different composition than that of the first insulating film, over the first insulating film;

c) forming a third insulating film, having a different composition than that of the second insulating film, over the second insulating film;

d) forming a thin film over the third insulating film;

e) forming a first resist pattern on the thin film, the first resist pattern having openings for forming wiring grooves;

f) etching the thin film using the first resist pattern as a mask, thereby forming a mask pattern out of the thin film to have the openings for forming wiring grooves;

g) removing the first resist pattern and then forming a second resist pattern on the third insulating film and the mask pattern, the second resist pattern having openings for forming contact holes;

h) dry-etching the third insulating film using the second resist pattern and the mask pattern as a mask, thereby patterning the third insulating film to have the openings for forming contact holes;

i) dry-etching the second insulating film using the patterned third insulating film as a mask, thereby patterning the second insulating film to have the openings for forming contact holes;

j) dry-etching the patterned third insulating film and the first insulating film using the mask pattern and the patterned second insulating film as respective masks, thereby forming wiring grooves and contact holes in the patterned third insulating film and the first insulating film, respectively; and

k) filling in the wiring grooves and the contact holes with a metal film, thereby forming upper-level metal interconnects and contacts connecting the lower- and upper-level metal interconnects together.

14. The method of Claim 13, wherein at least one of the first and third insulating films is mainly composed of an organic component.

15. The method of Claim 13, wherein a size of the openings of the second resist pattern for forming contact holes is larger than a designed size of the contact holes in a direction vertical to a direction in which the upper-level metal interconnects extend.

ABSTRACT OF THE DISCLOSURE

In a method for forming an interconnection structure, first, second and third insulating films and a thin film are sequentially formed over lower-level metal interconnects. Then, the thin film is masked with a first resist pattern and etched to form a mask pattern with openings for interconnects. Next, the third insulating film is masked with a second resist pattern and dry-etched such that the third insulating film and the first and second resist patterns are etched at a high rate and that the second insulating film is etched at a low rate to form openings for contact holes in the third insulating film and remove the first and second resist patterns. Then, the second insulating film is masked with the third insulating film and dry-etched such that the second insulating film is etched at a high rate and that the first and third insulating films are etched at a low rate to form the openings for contact holes in the second insulating film. Then, the third and first insulating films are masked with the mask pattern and the second insulating film, respectively, and dry-etched such that the first and third insulating films are etched at a high rate and that the mask pattern and the second insulating film are etched at a low rate to form wiring grooves and contact holes in the third and first insulating films, respectively. Finally, upper-level metal interconnects and contacts are formed.

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Fig. 1(a)

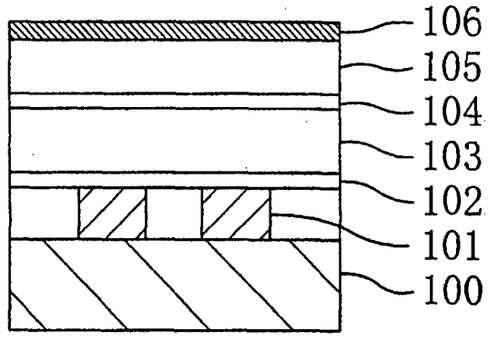

Fig. 1(b)

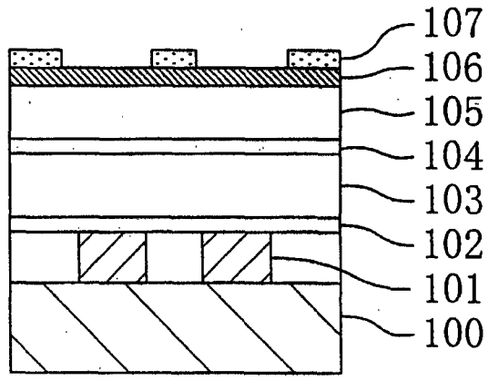

Fig. 1(c)

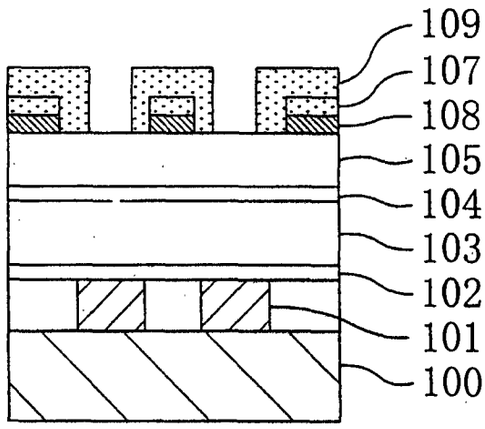

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Fig. 2(a)

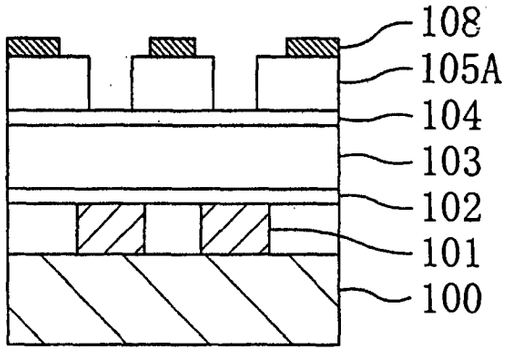

Fig. 2(b)

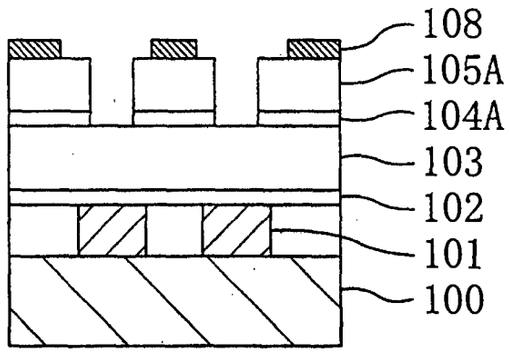

Fig. 2(c)

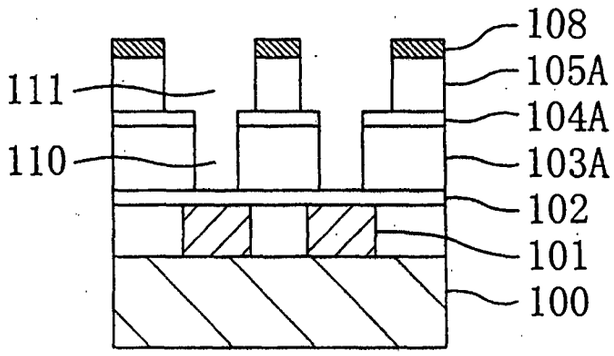

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Fig. 3(a)

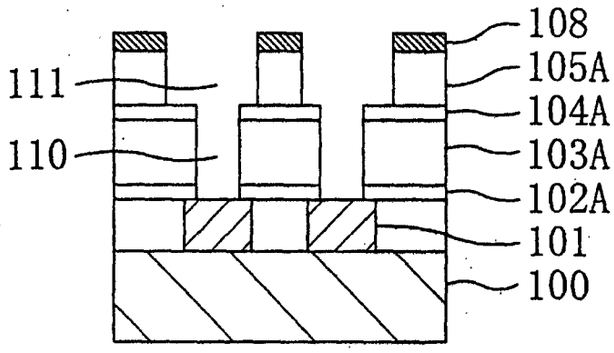

Fig. 3(b)

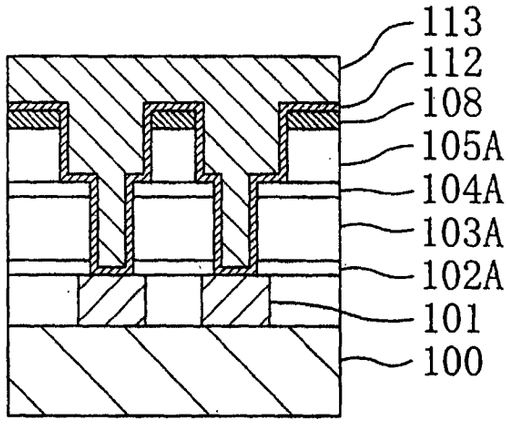

Fig. 3(c)

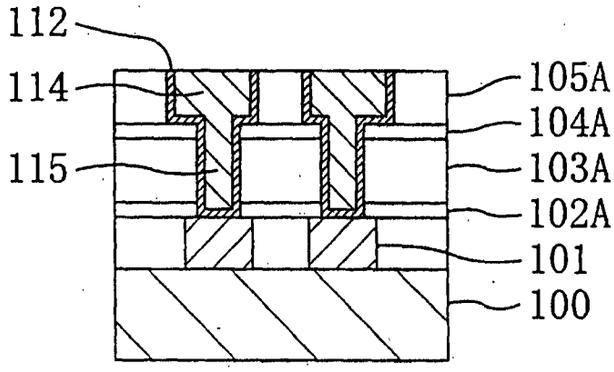

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Fig. 4(a)

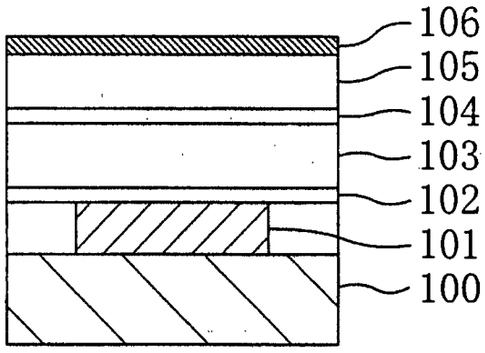

Fig. 4(b)

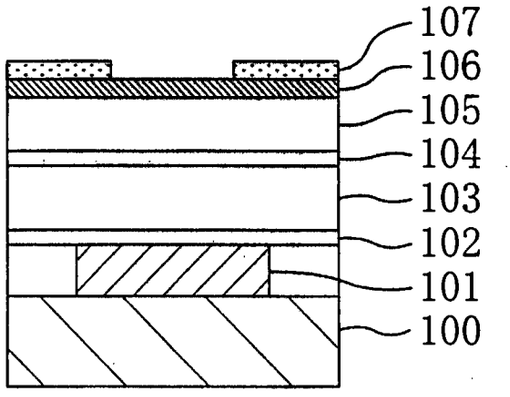

Fig. 4(c)

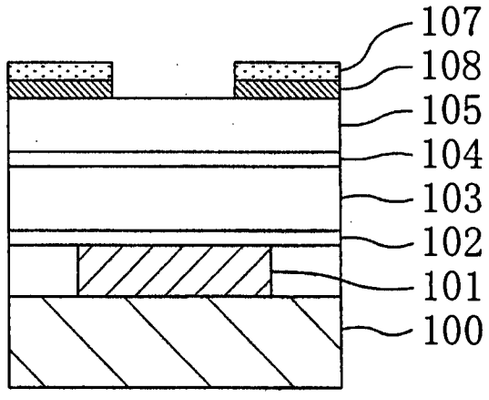

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Fig. 5(a)

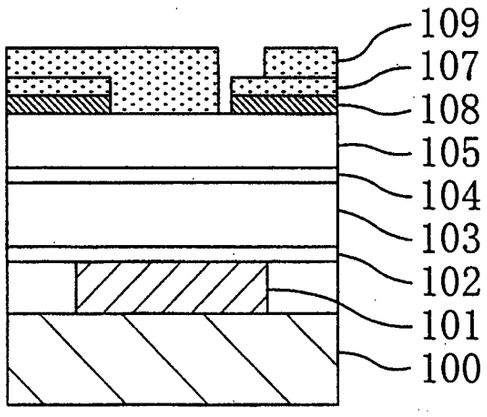

Fig. 5(b)

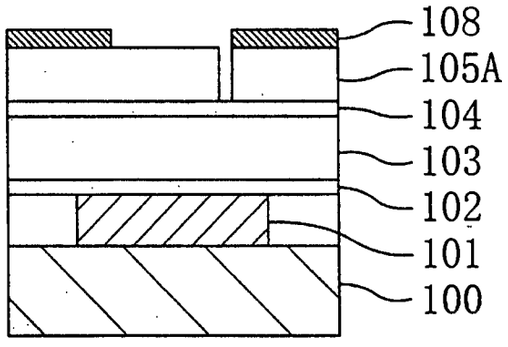

Fig. 5(c)

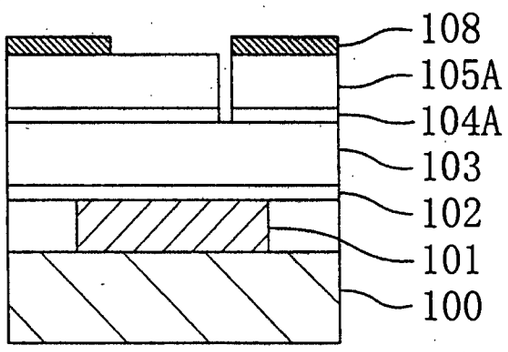

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Fig. 6(a)

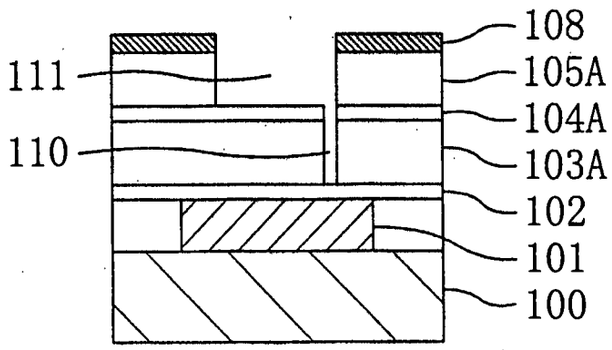

Fig. 6(b)

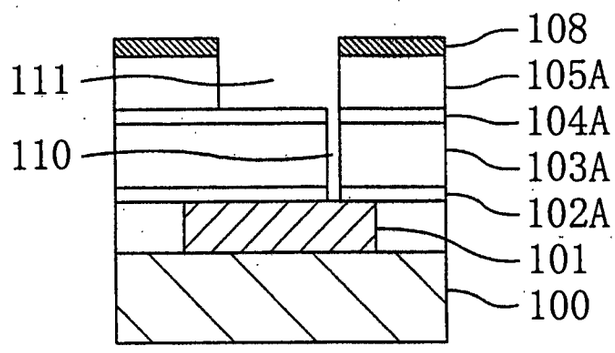

Fig. 6(c)

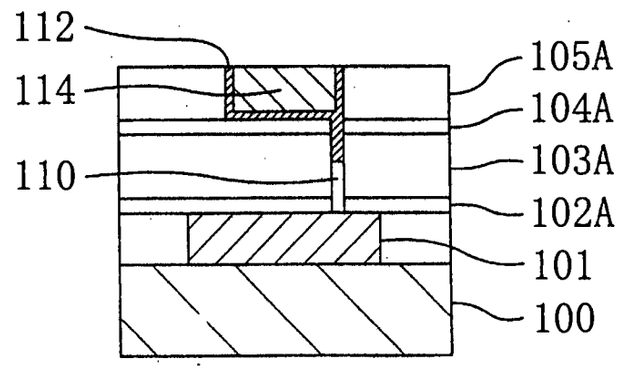

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Fig. 7(a)

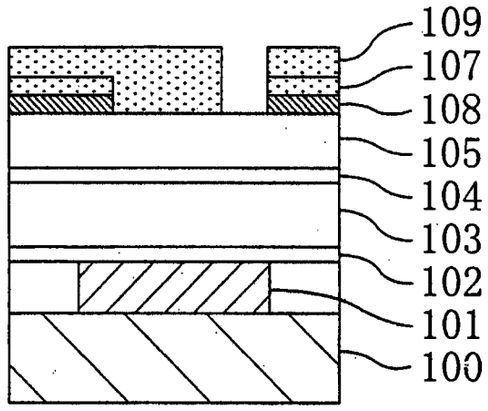

Fig. 7(b)

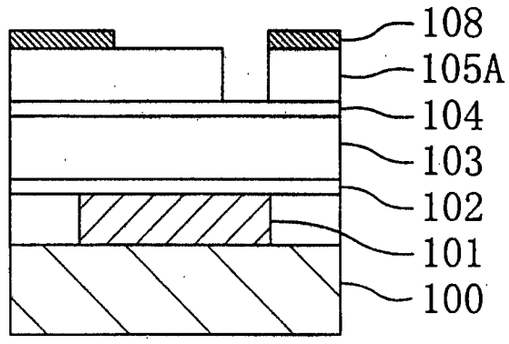

Fig. 7(c)

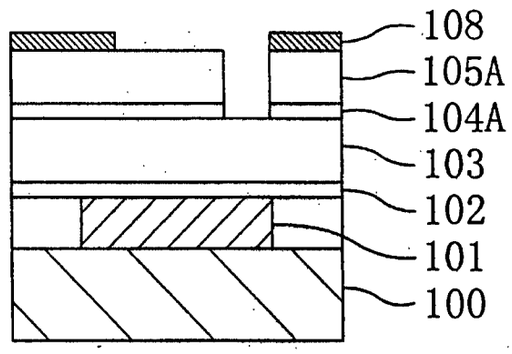

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Fig. 8(a)

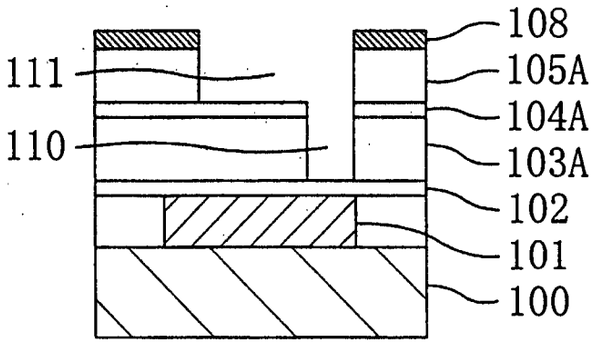

Fig. 8(b)

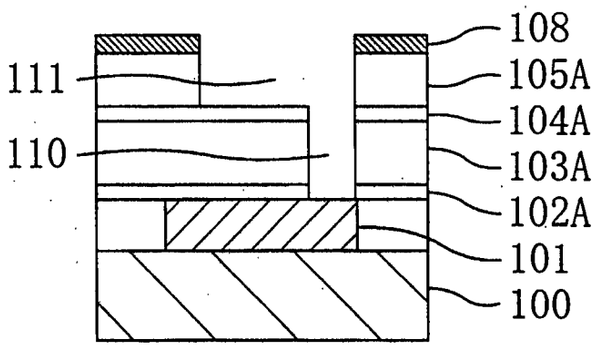

Fig. 8(c)

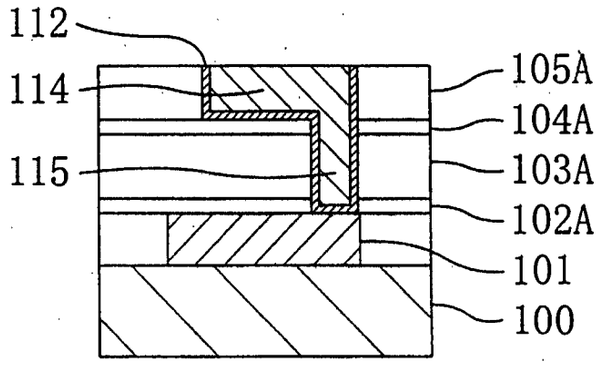

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Fig. 9(a)

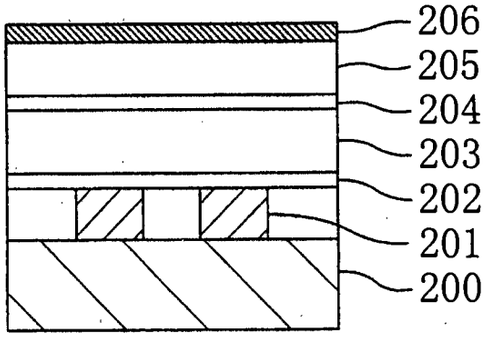

Fig. 9(b)

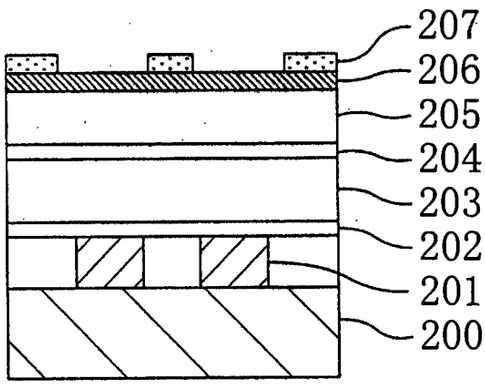

Fig. 9(c)

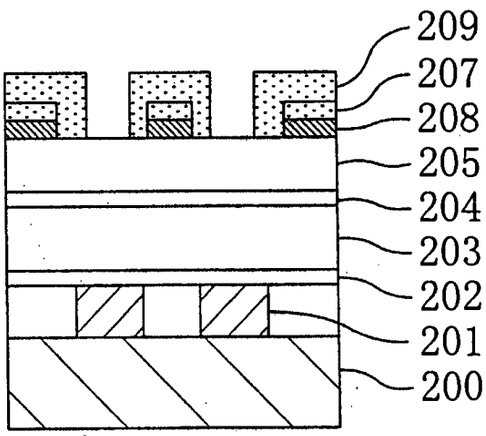

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Fig. 10(a)

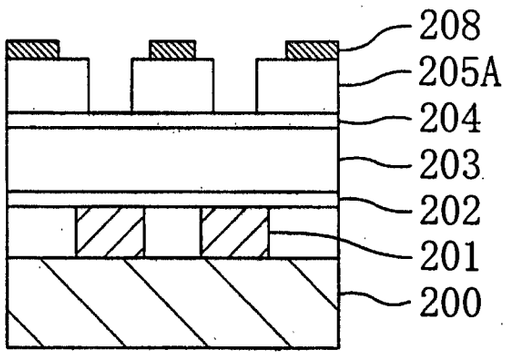

Fig. 10(b)

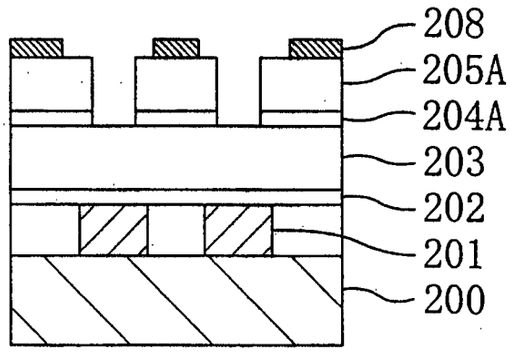

Fig. 10(c)

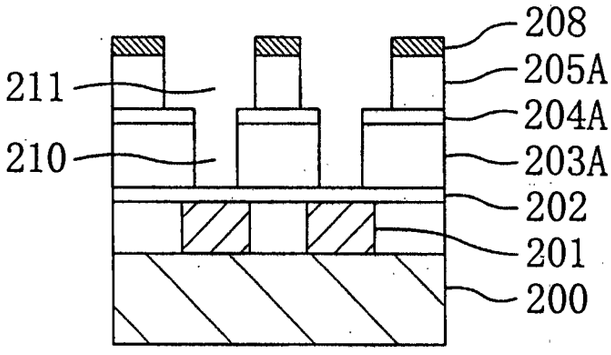

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Fig. 11(a)

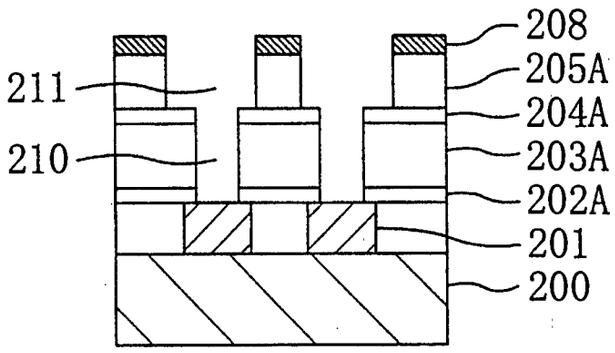

Fig. 11(b)

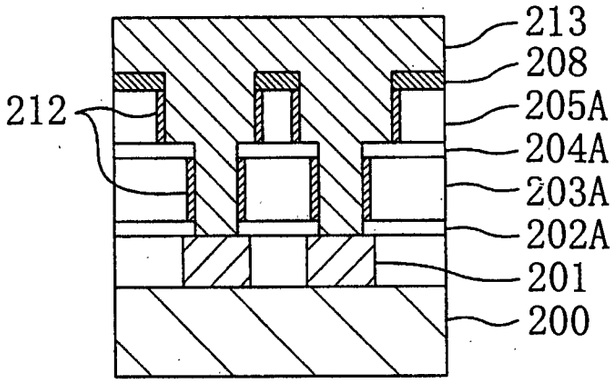

Fig. 11(c)

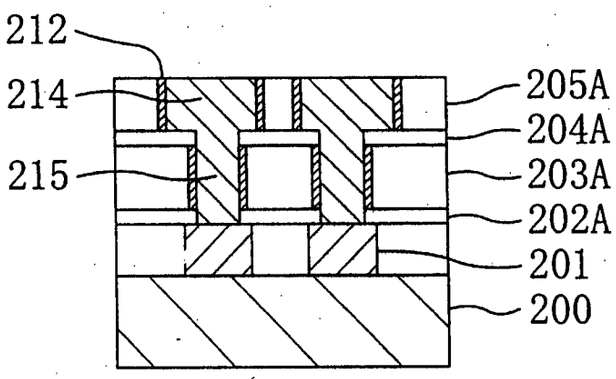

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Fig. 12(a)

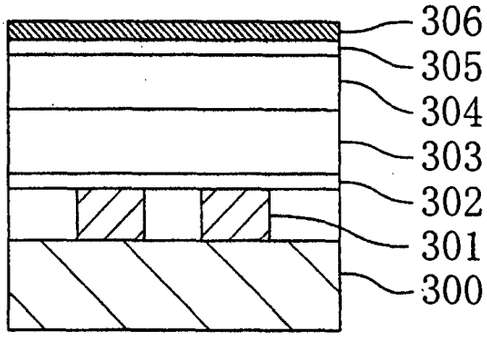

Fig. 12(b)

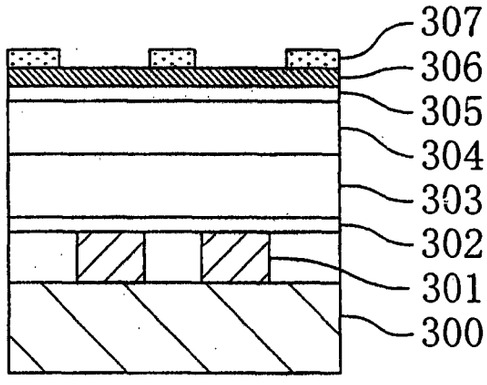

Fig. 12(c)

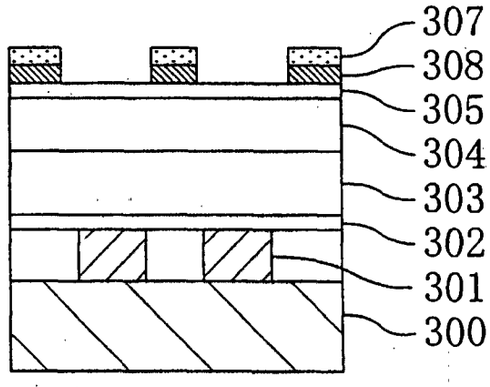

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Fig. 13(a)

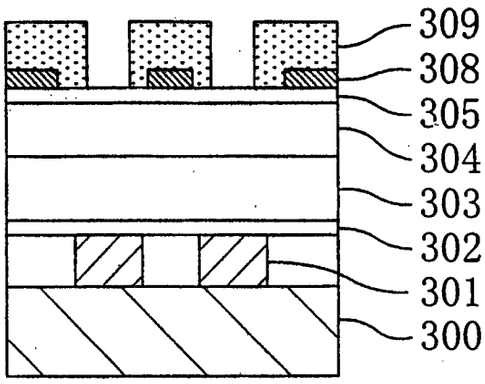


Fig. 13(b)

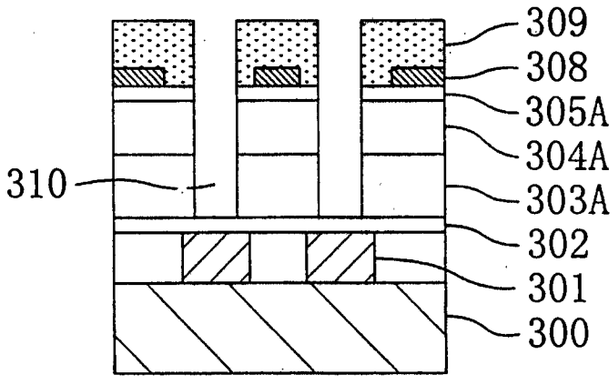
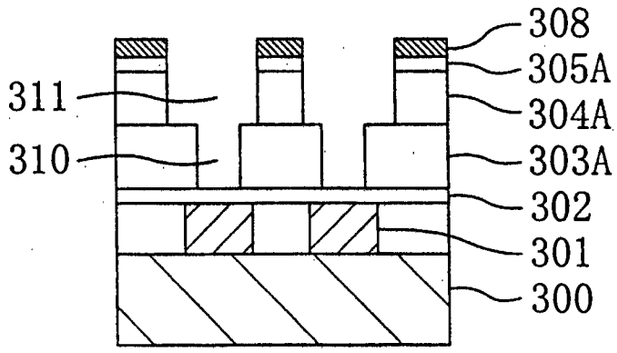


Fig. 13(c)



PRINT OF DRAWINGS
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Fig. 14(a)

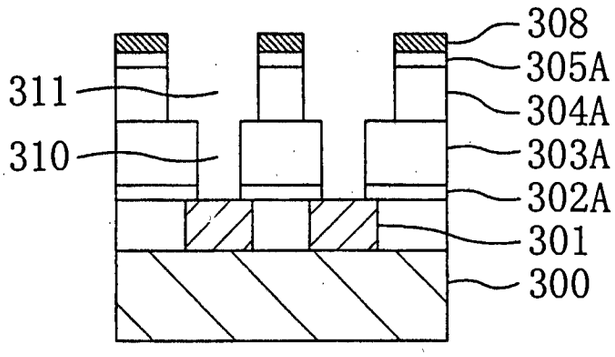


Fig. 14(b)

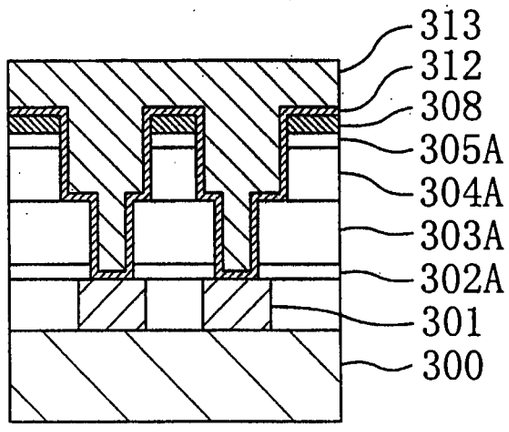
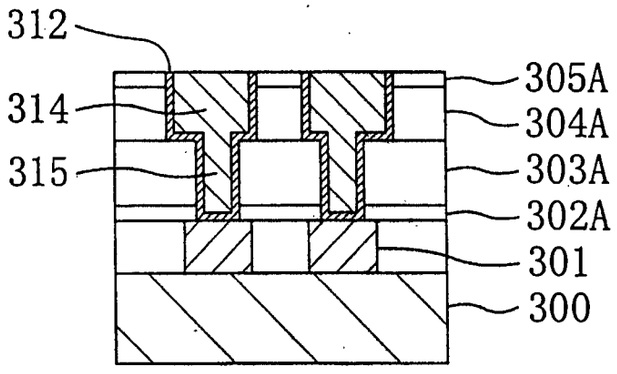


Fig. 14(c)



PRINT OF DRAWINGS
AS ORIGINALLY FILE

Fig. 15(a)

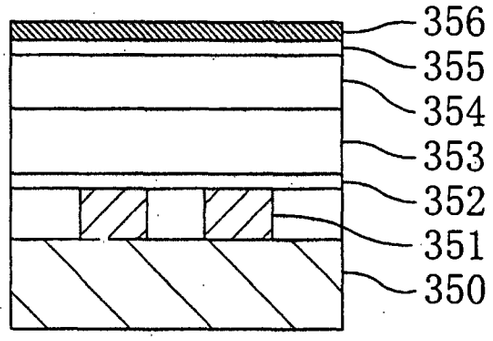


Fig. 15(b)

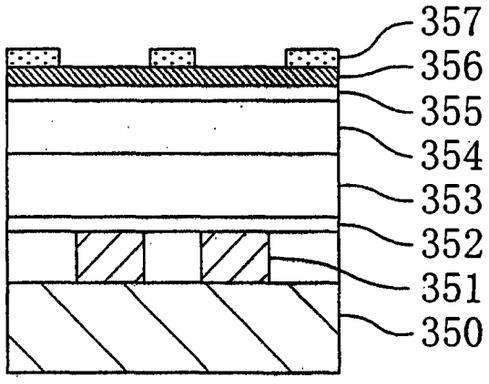
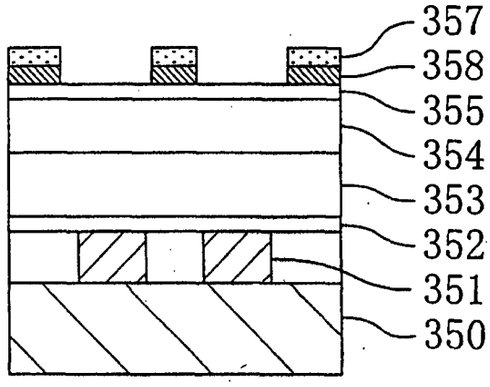


Fig. 15(c)



PRINT OF DRAWINGS
AS ORIGINALLY FILE

Fig. 16(a)

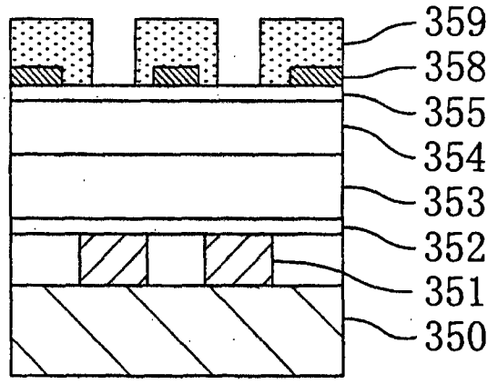


Fig. 16(b)

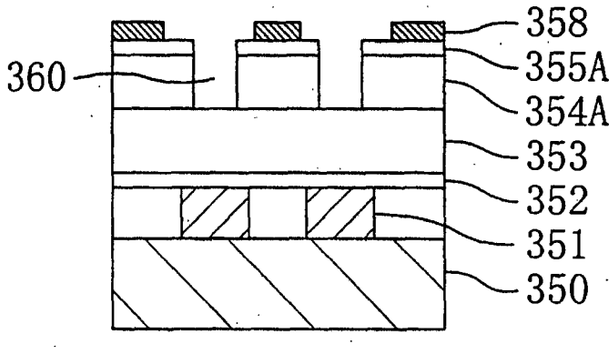


Fig. 16(c)

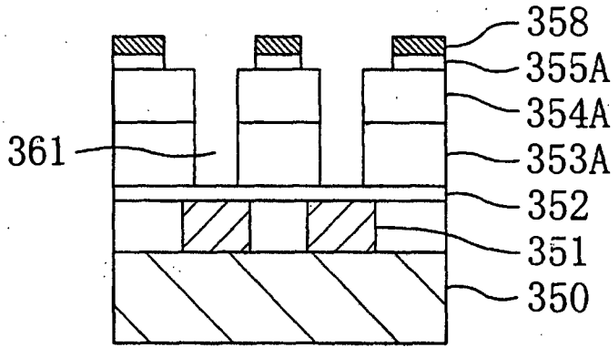
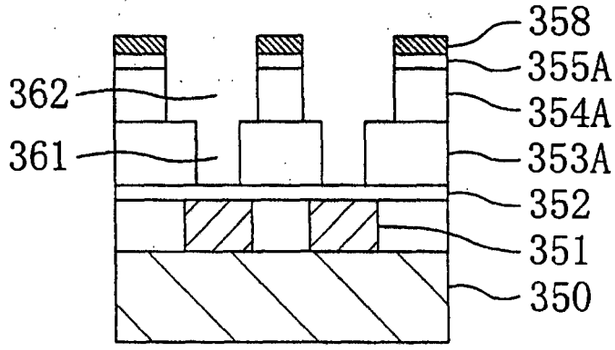


Fig. 16(d)



PRINT OF DRAWINGS
AS ORIGINALLY FILE

Fig. 17(a)

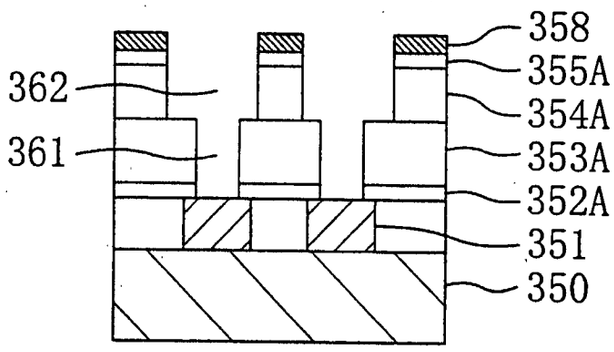


Fig. 17(b)

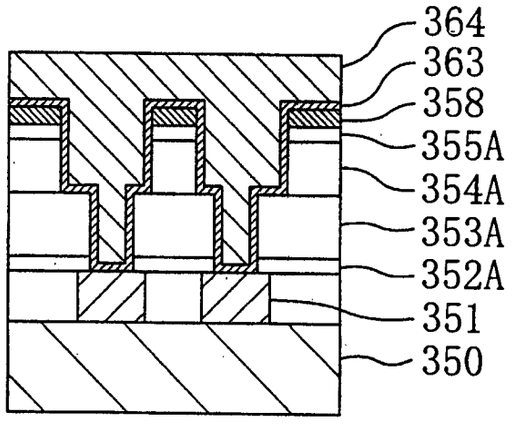


Fig. 17(c)

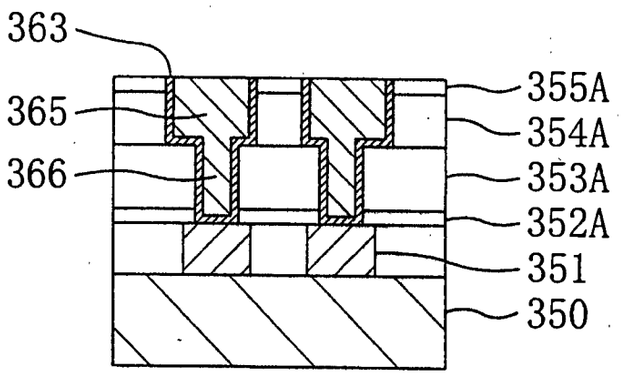


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Fig. 18(a)

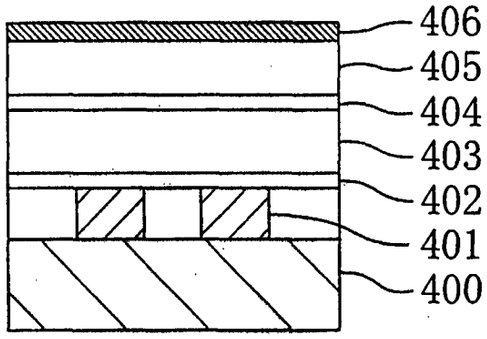

Fig. 18(b)

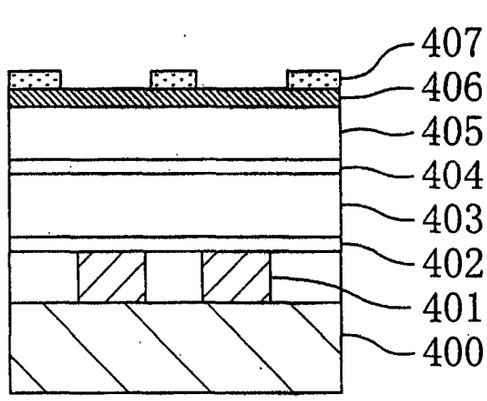

Fig. 18(c)

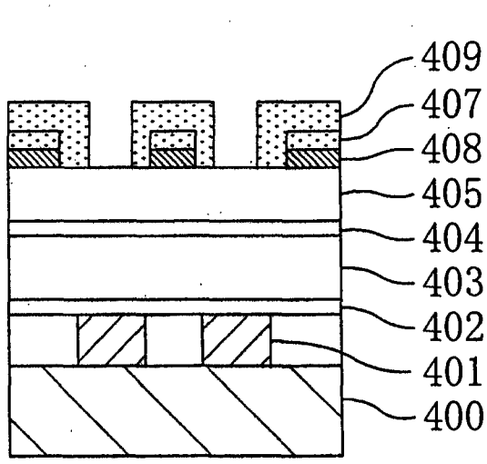

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Fig. 19(a)

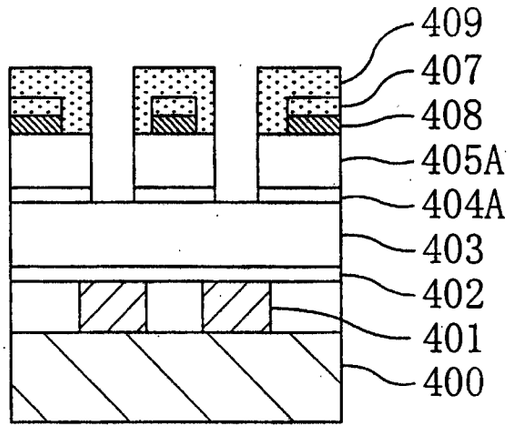


Fig. 19(b)

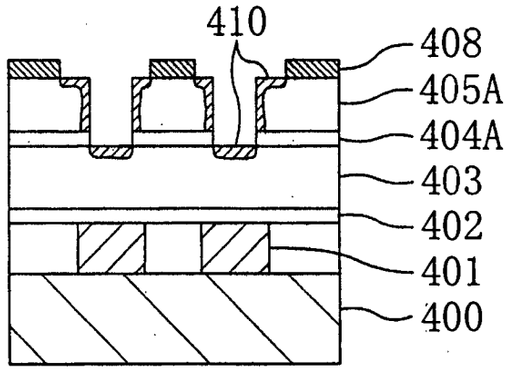
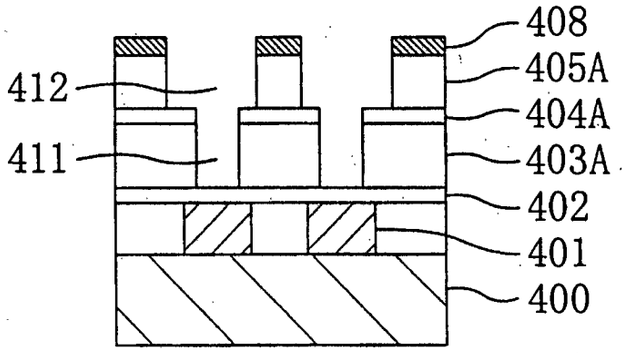


Fig. 19(c)



PRINT OF DRAWINGS
AS ORIGINALLY FILE

Fig. 20(a)

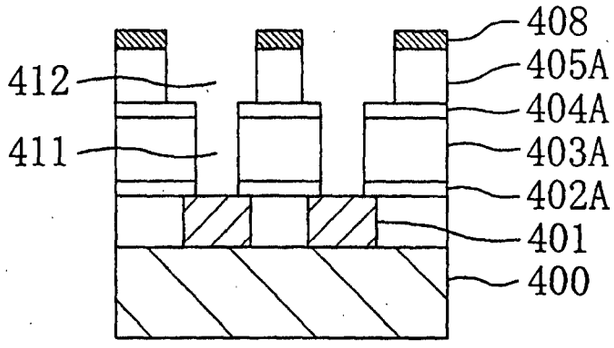


Fig. 20(b)

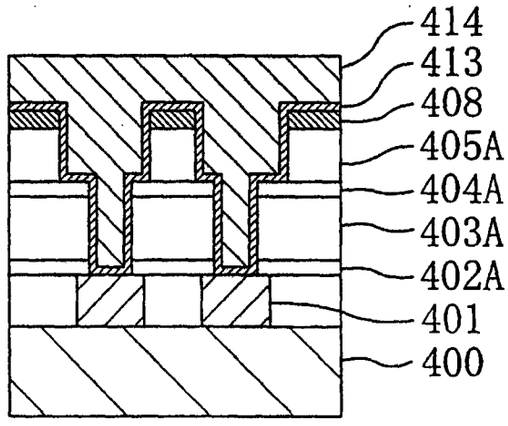
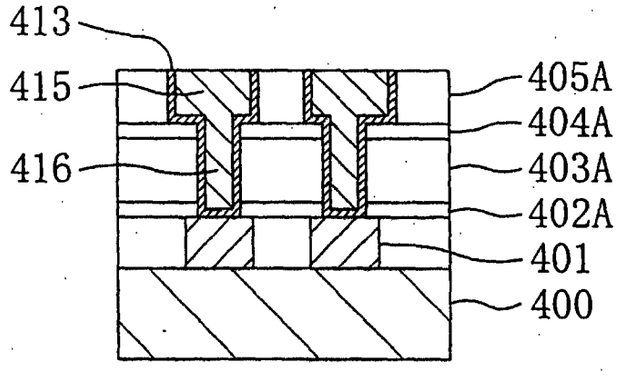


Fig. 20(c)



PRINT OF DRAWINGS
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Fig. 21(a)

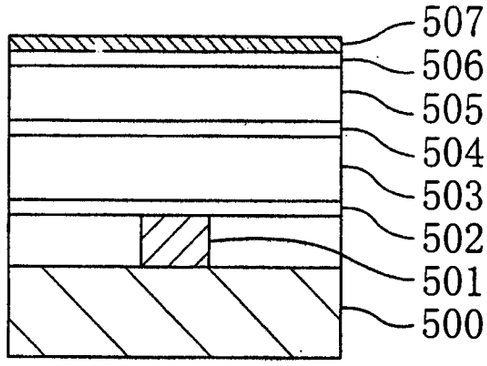


Fig. 21(b)

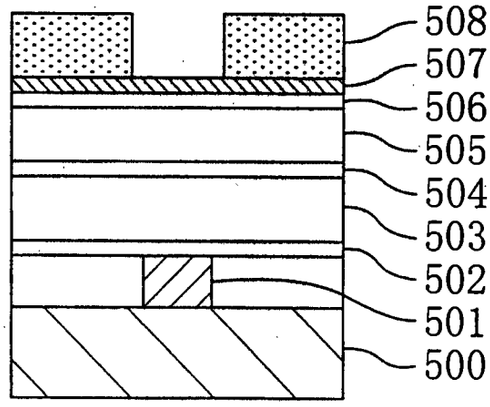
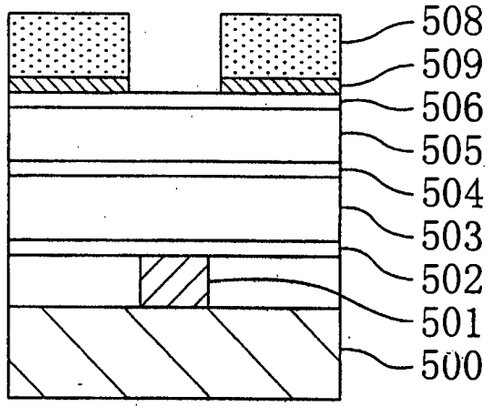


Fig. 21(c)



PRINT OF DRAWINGS
AS ORIGINALLY FILE

Fig. 22(a)

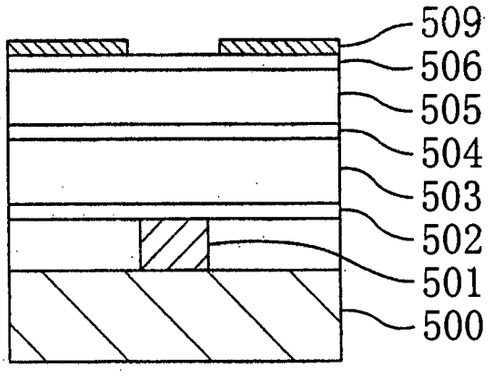


Fig. 22(b)

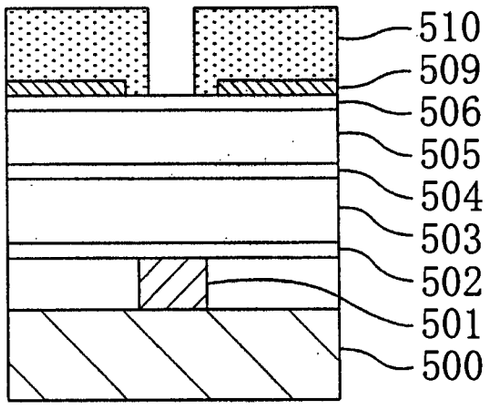
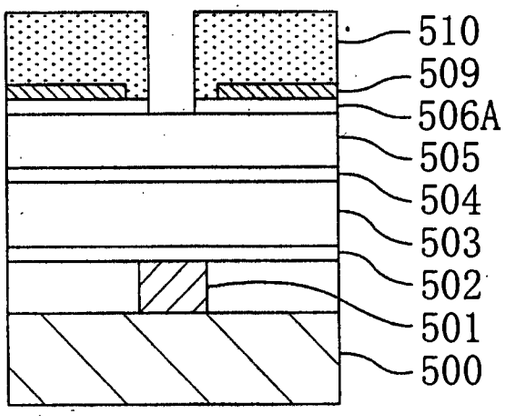


Fig. 22(c)



PRINT OF DRAWINGS
AS ORIGINALLY FILE

Fig. 23(a)

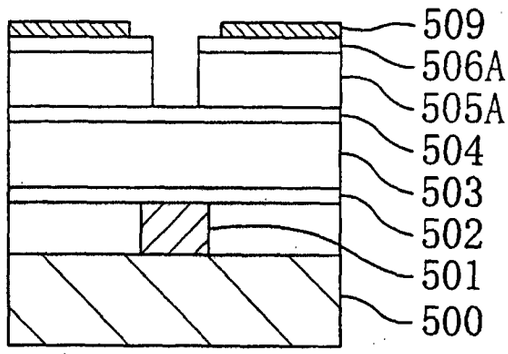


Fig. 23(b)

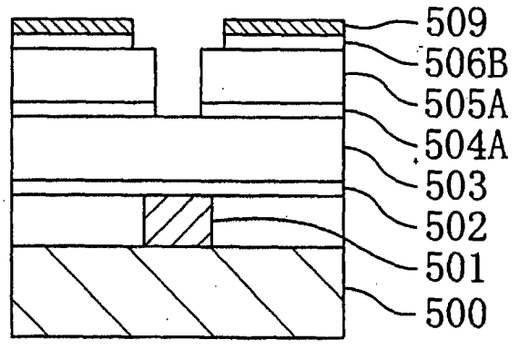


Fig. 23(c)

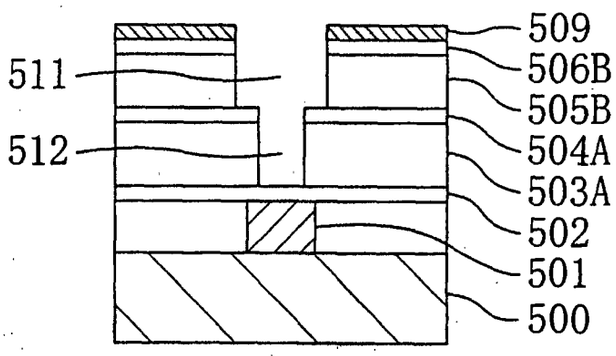


Fig. 23(d)

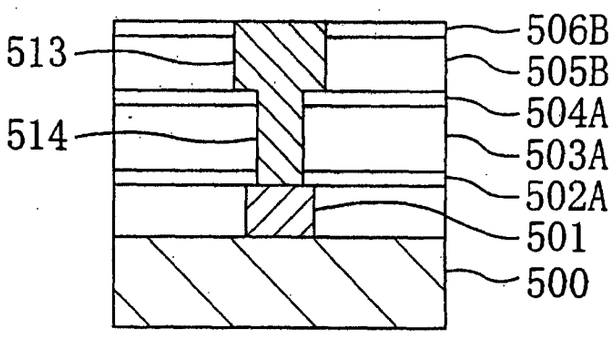


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Fig. 24(a)

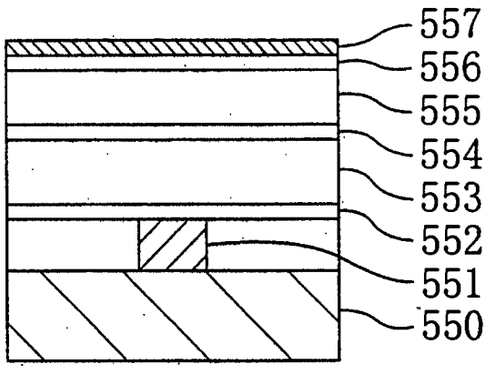

Fig. 24(b)

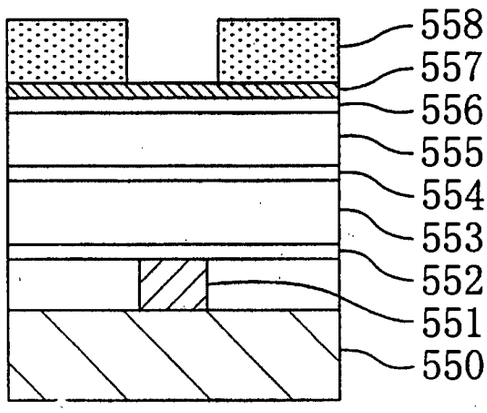

Fig. 24(c)

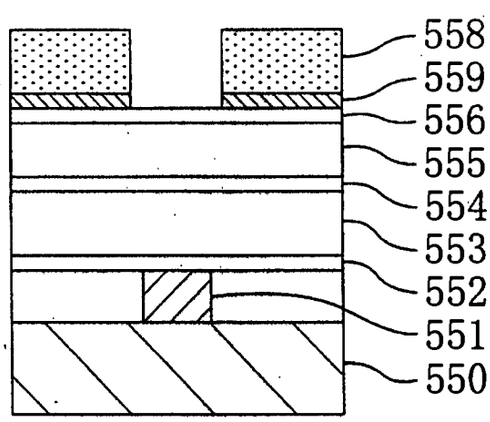

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Fig. 25(a)

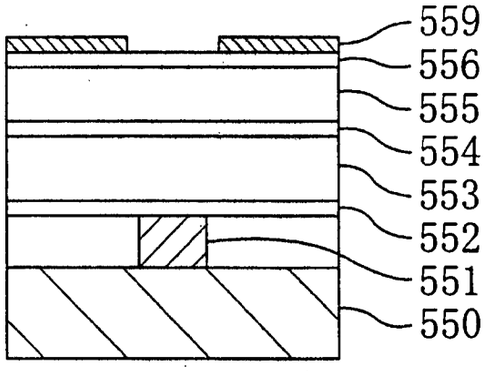


Fig. 25(b)

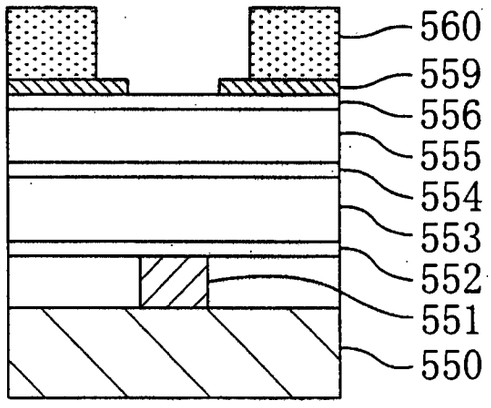
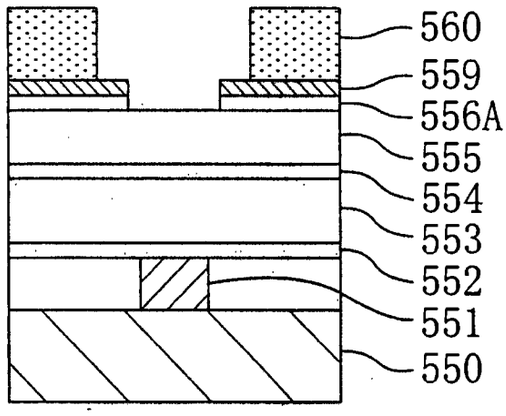


Fig. 25(c)



PRINT OF DRAWINGS
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Fig. 26(a)

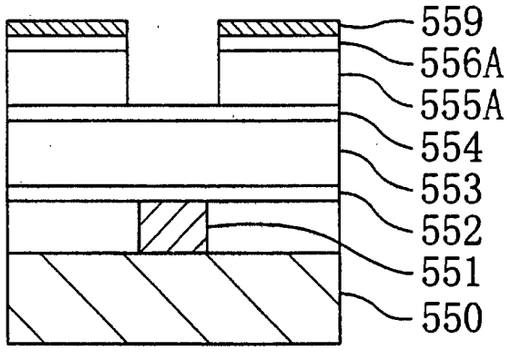

Fig. 26(b)

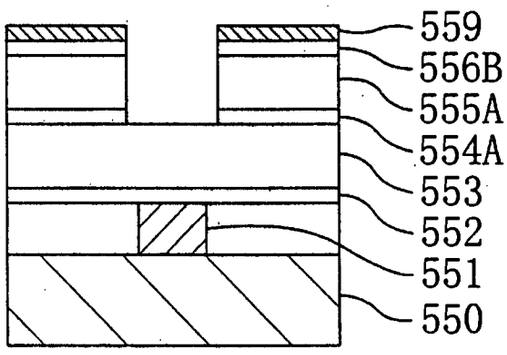

Fig. 26(c)

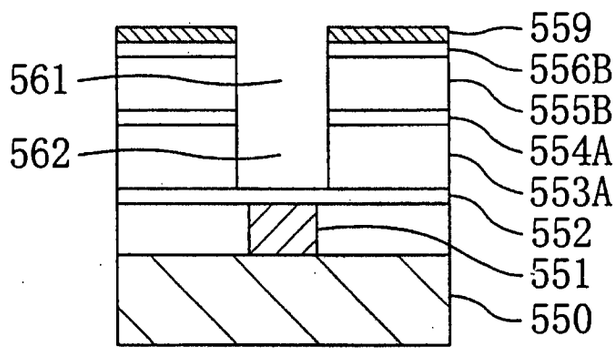

Fig. 26(d)

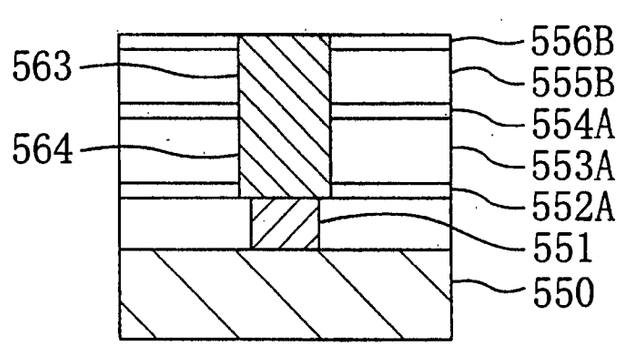

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Fig. 27(a)

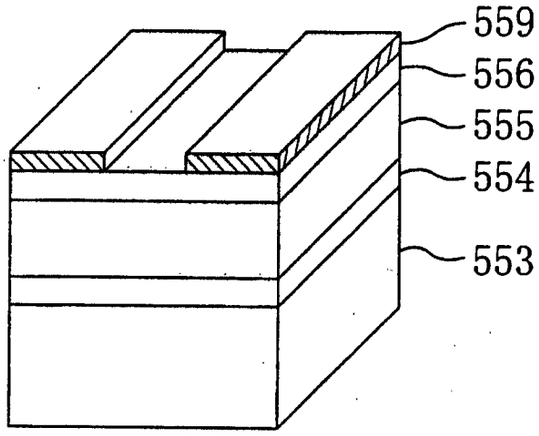

Fig. 27(b)

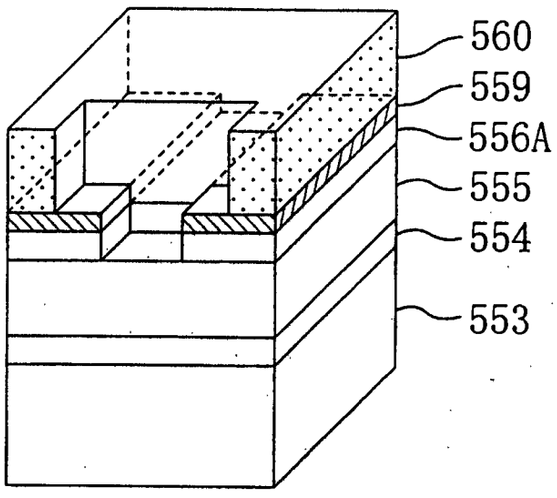

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Fig. 28(a)

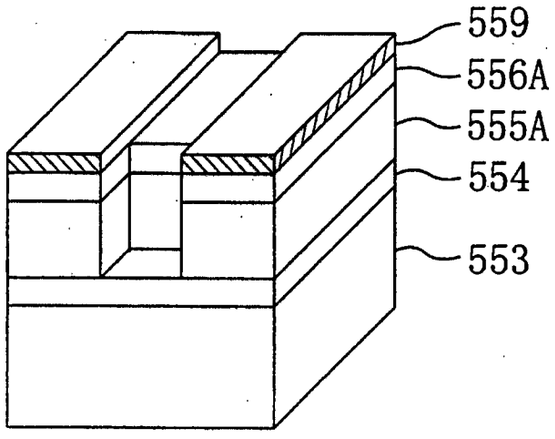
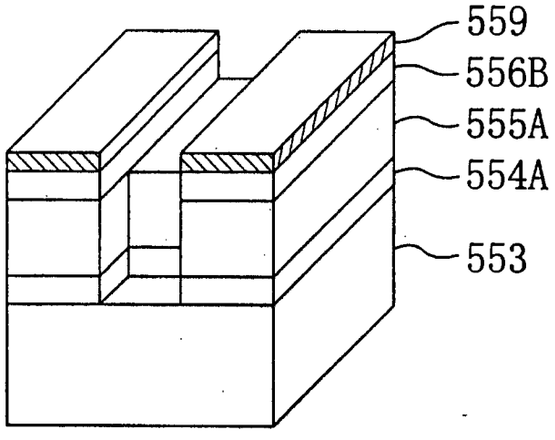


Fig. 28(b)



PRINT OF DRAWINGS
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Fig. 29(a)

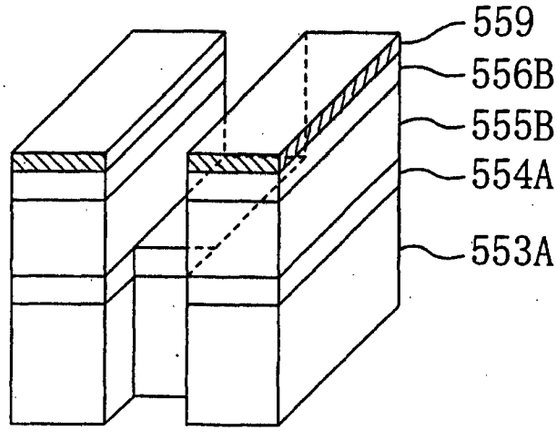

Fig. 29(b)

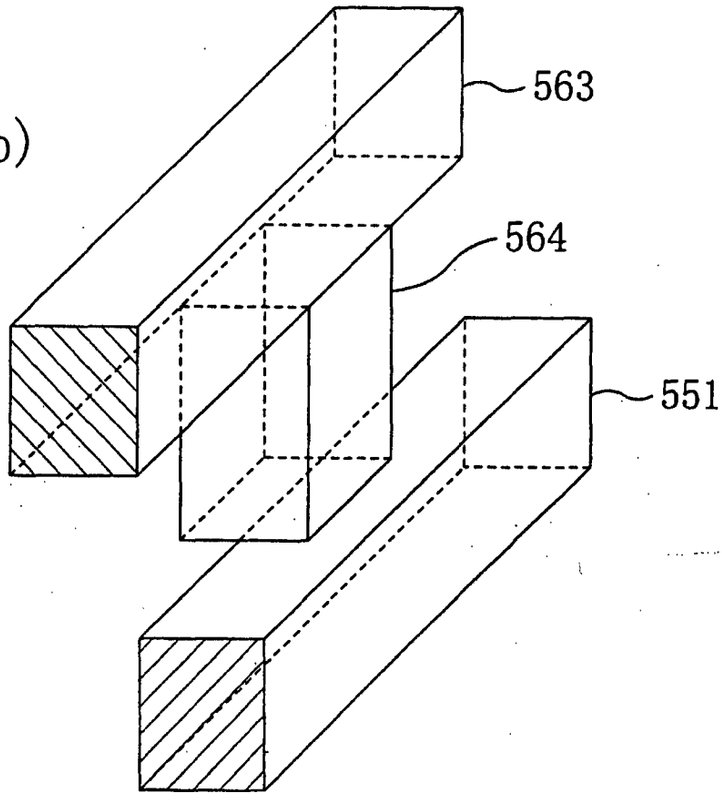

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Fig. 30(a)

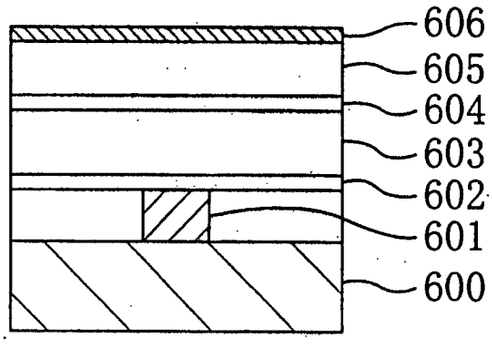


Fig. 30(b)

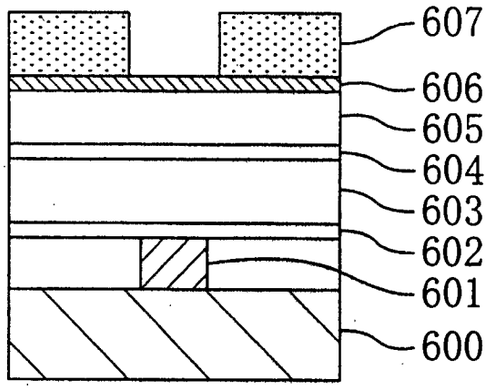
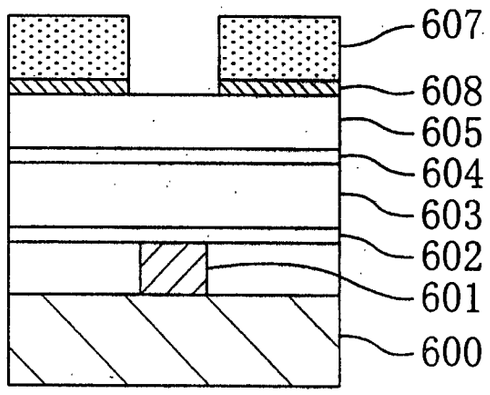


Fig. 30(c)



PRINT OF DRAWINGS
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Fig. 31(a)

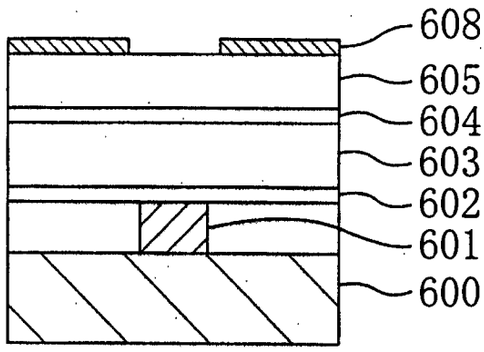


Fig. 31(b)

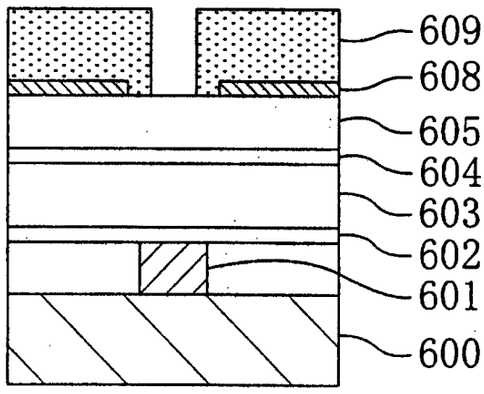
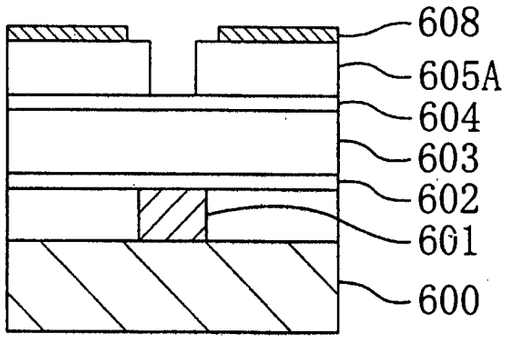


Fig. 31(c)



PRINT OF DRAWINGS
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Fig. 32(a)

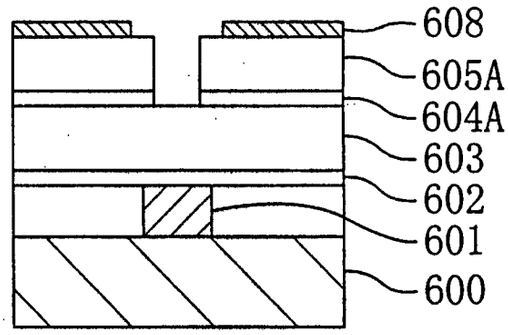


Fig. 32(b)

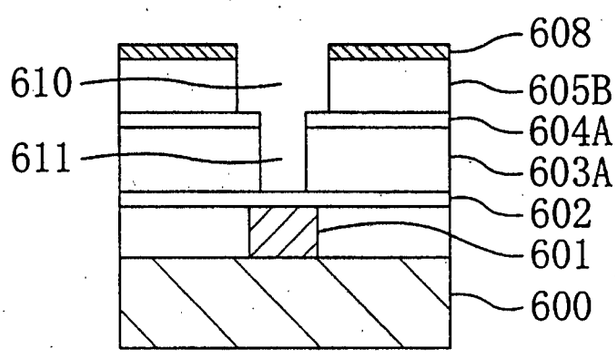
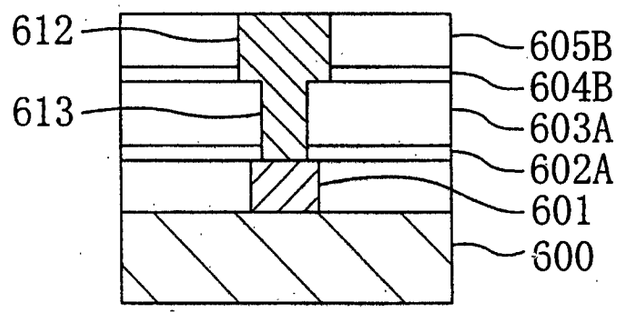


Fig. 32(c)



PRINT OF DRAWINGS
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Fig. 33(a)

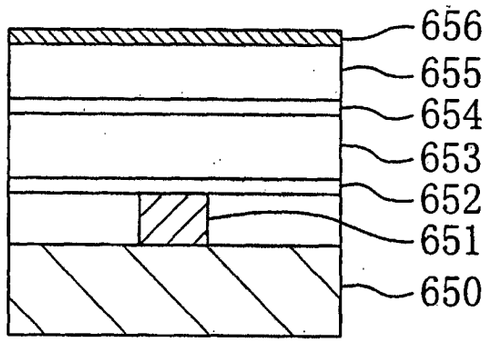

Fig. 33(b)

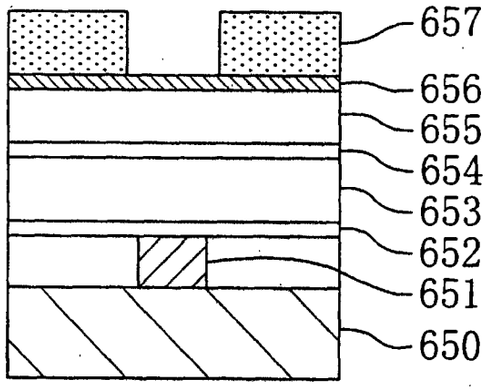

Fig. 33(c)

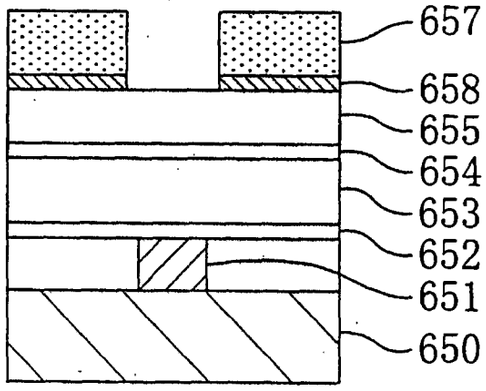

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Fig. 34(a)

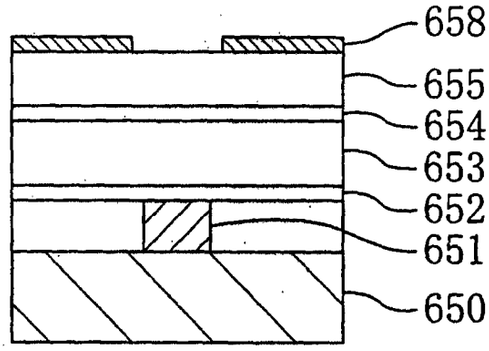

Fig. 34(b)

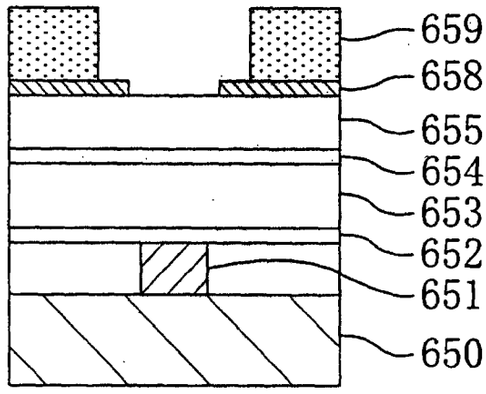

Fig. 34(c)

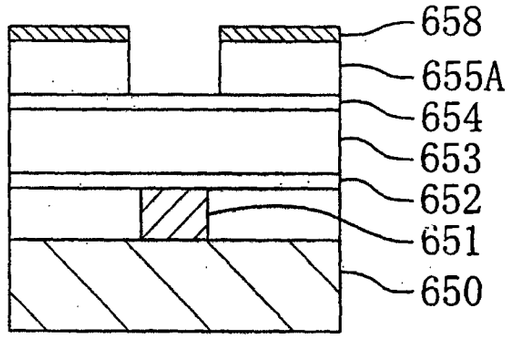

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Fig. 35(a)

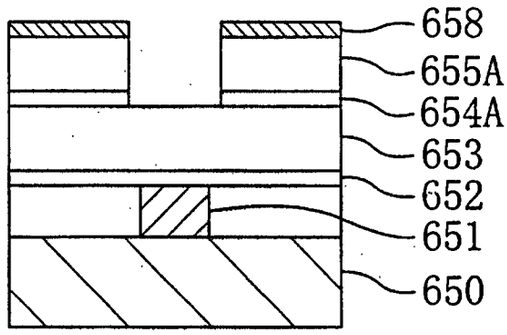

Fig. 35(b)

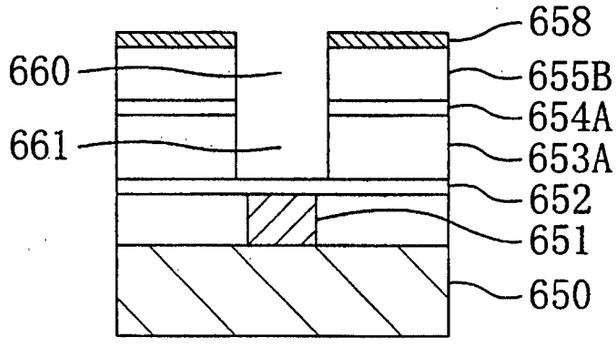

Fig. 35(c)

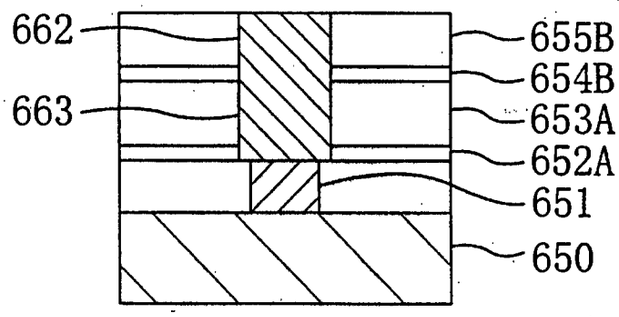

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Fig. 36

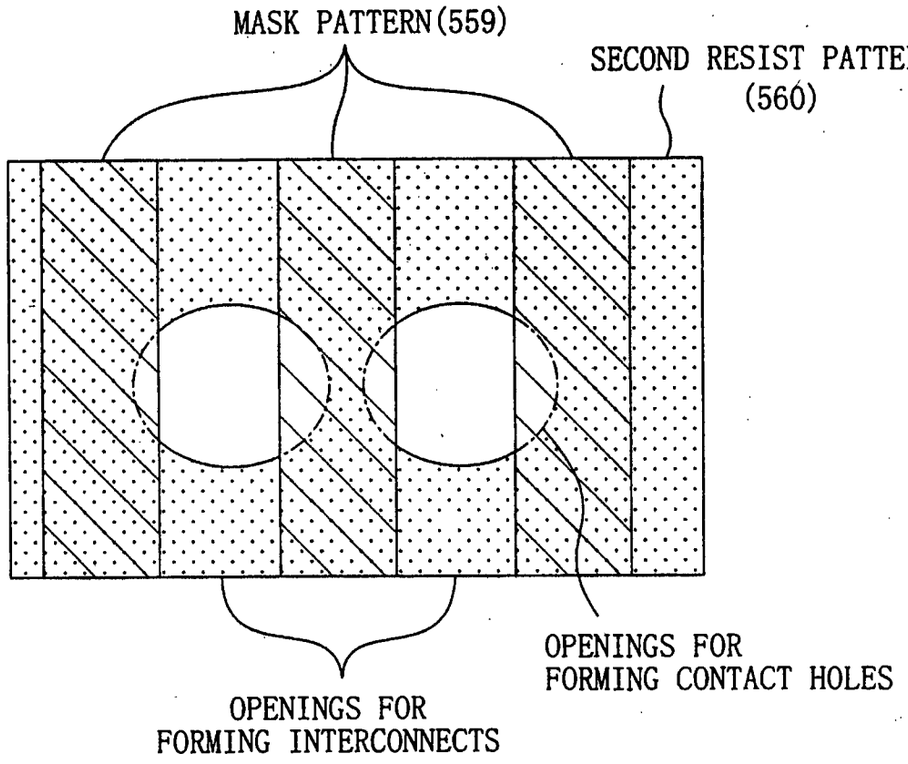

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Fig. 37(a)

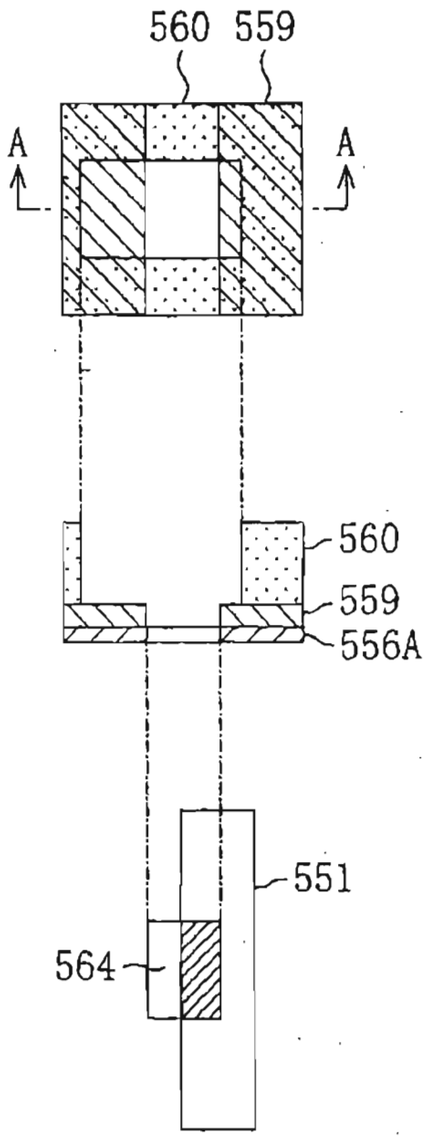

Fig. 37(b)

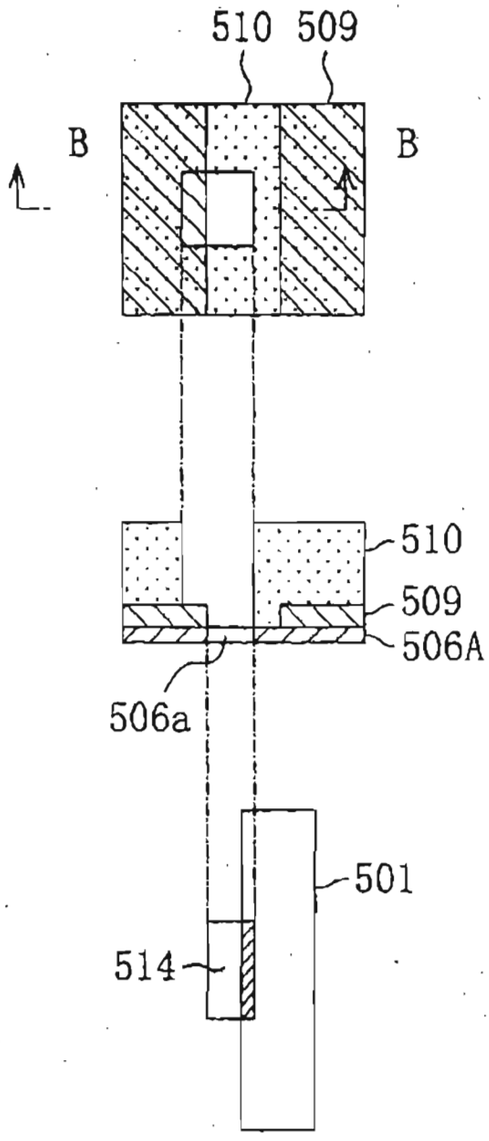

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Fig. 1(a)

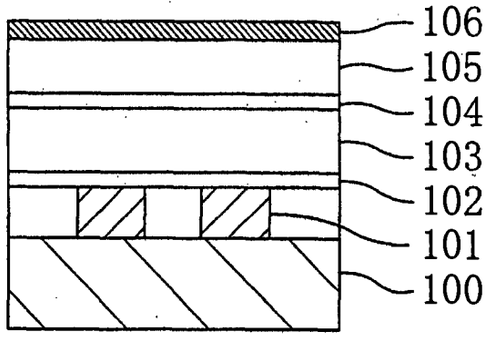

Fig. 1(b)

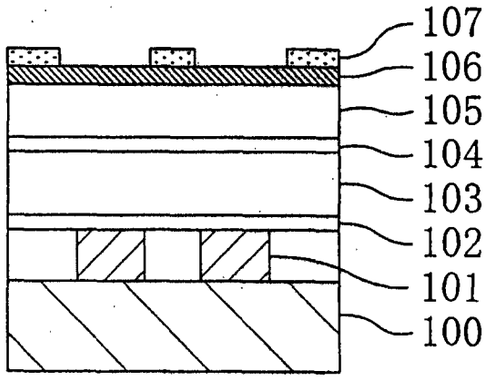

Fig. 1(c)

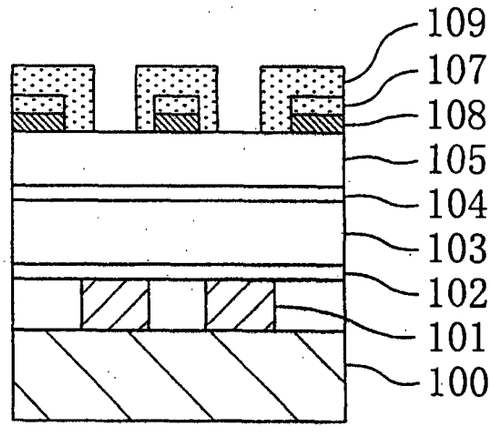

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Fig. 2(a)

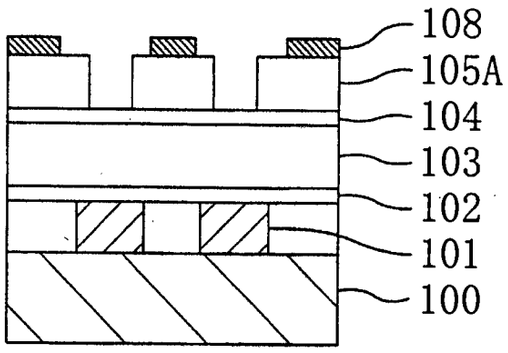


Fig. 2(b)

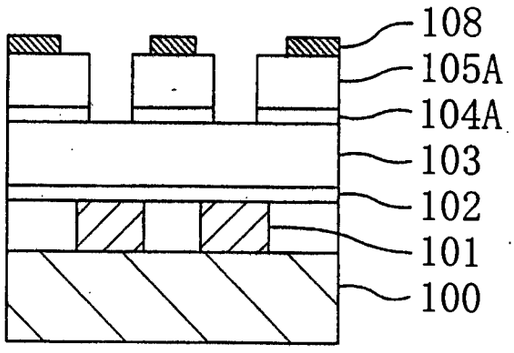
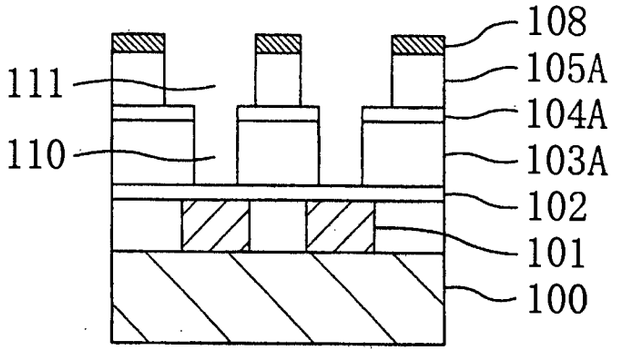


Fig. 2(c)



PRINT OF DRAWINGS
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Fig. 3(a)

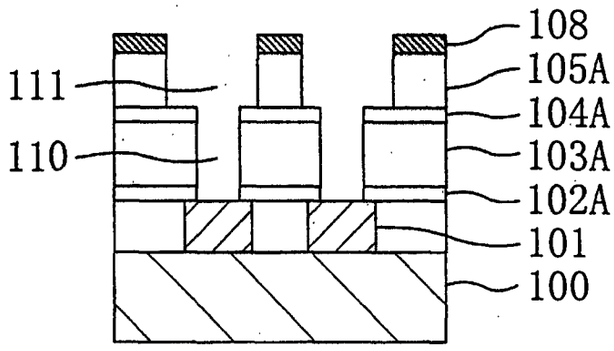

Fig. 3(b)

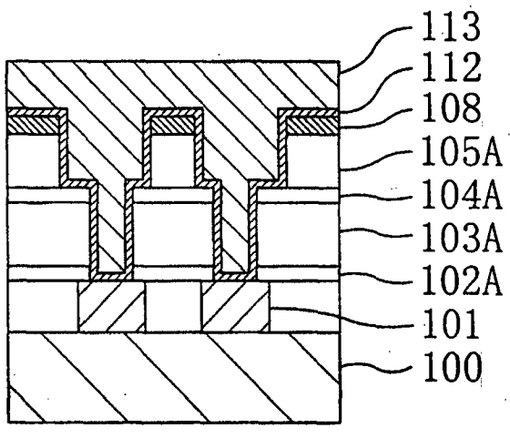

Fig. 3(c)

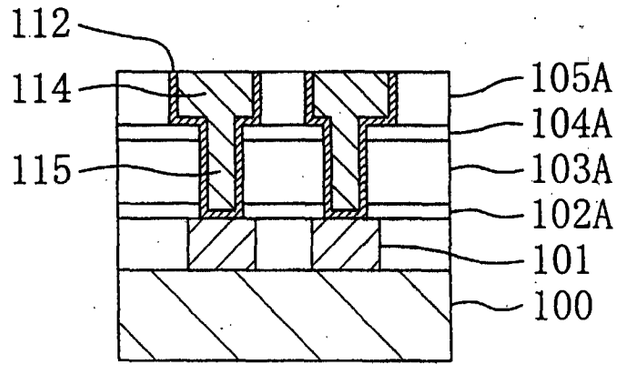

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Fig. 4(a)

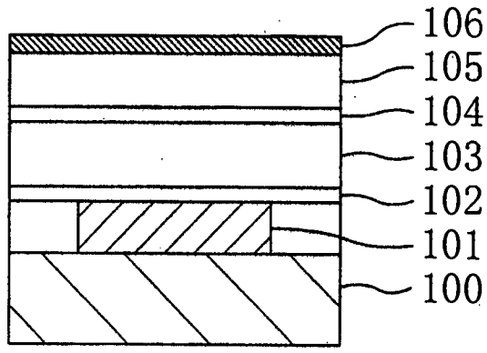

Fig. 4(b)

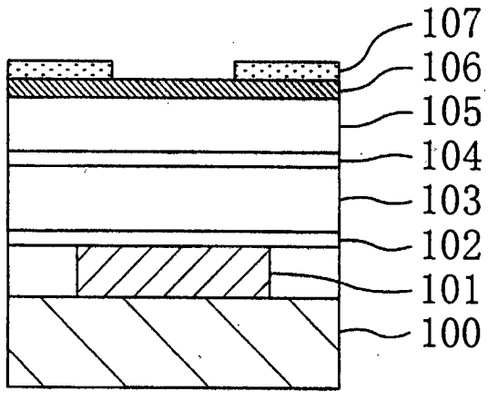

Fig. 4(c)

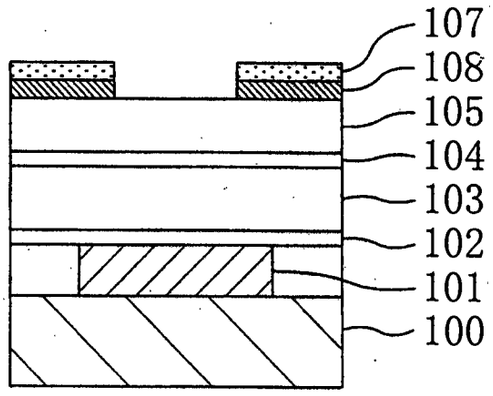

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Fig. 5(a)

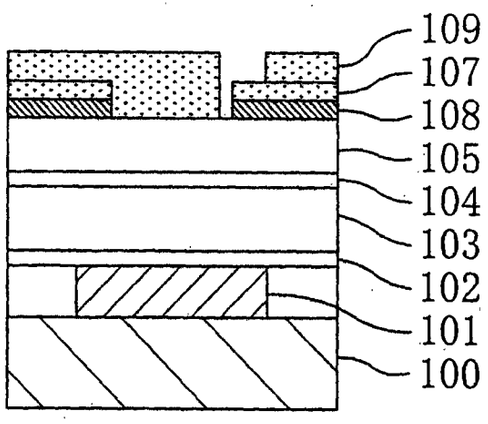

Fig. 5(b)

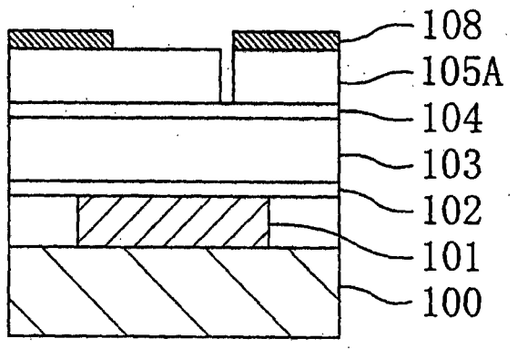

Fig. 5(c)

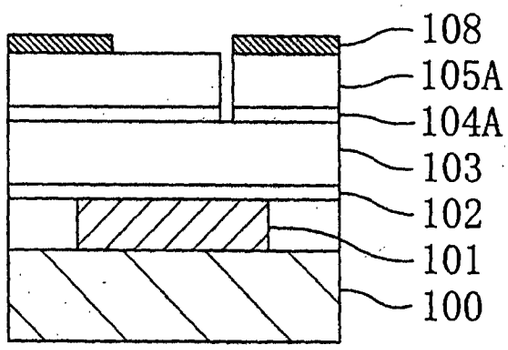

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Fig. 6(a)

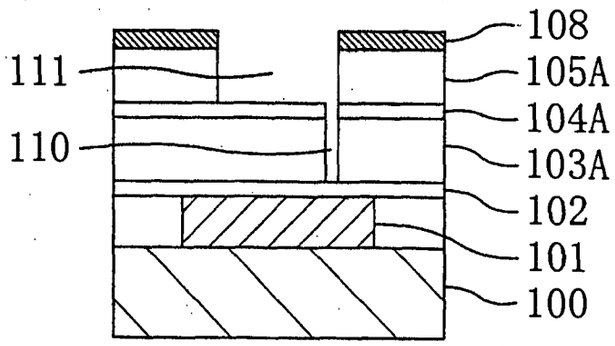

Fig. 6(b)

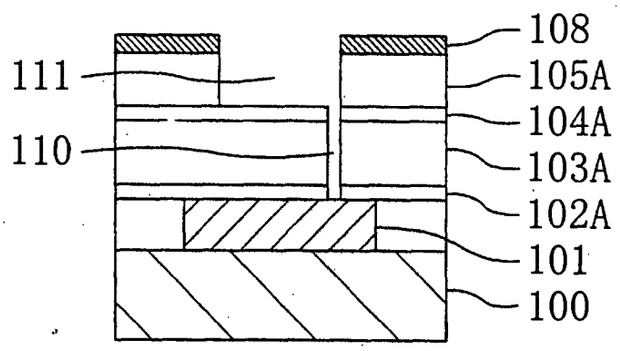

Fig. 6(c)

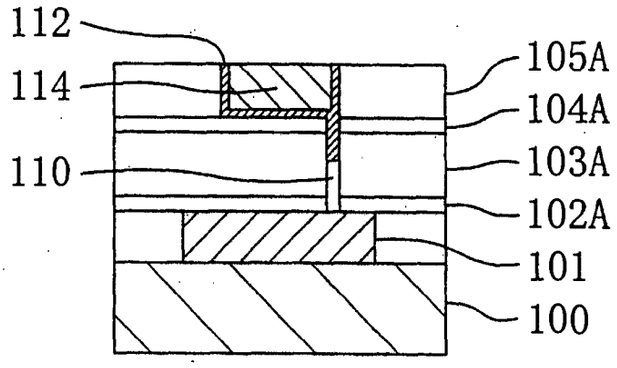

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Fig. 7(a)

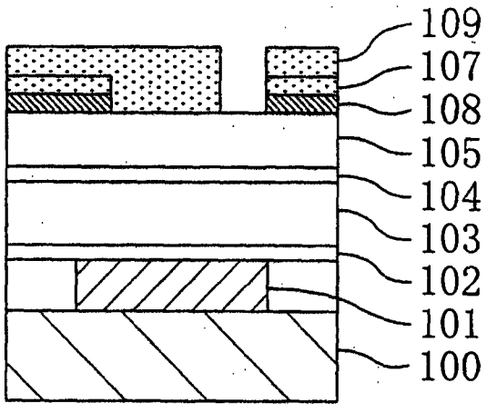

Fig. 7(b)

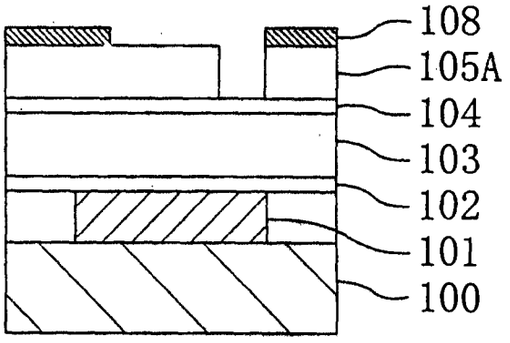

Fig. 7(c)

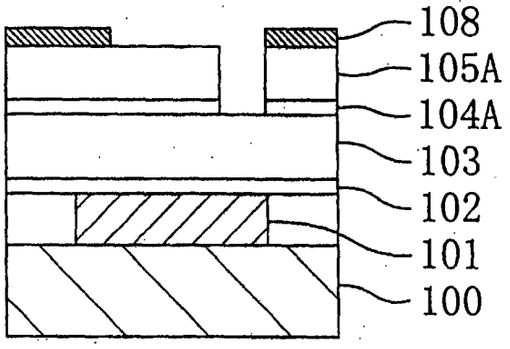

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Fig. 8(a)

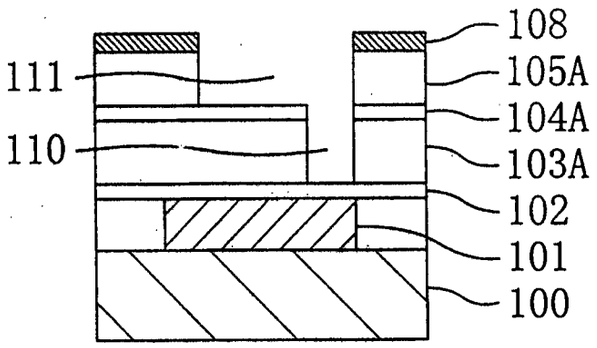

Fig. 8(b)

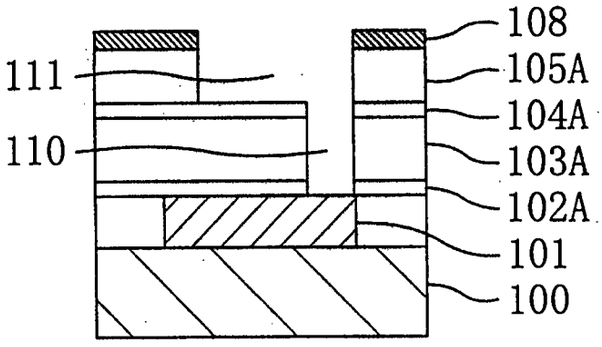

Fig. 8(c)

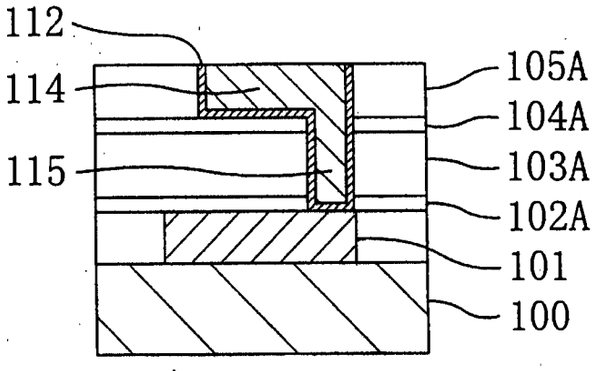

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Fig. 9(a)

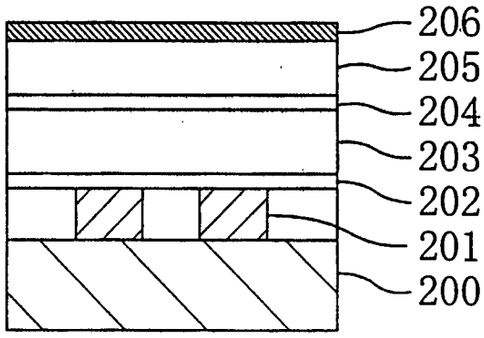

Fig. 9(b)

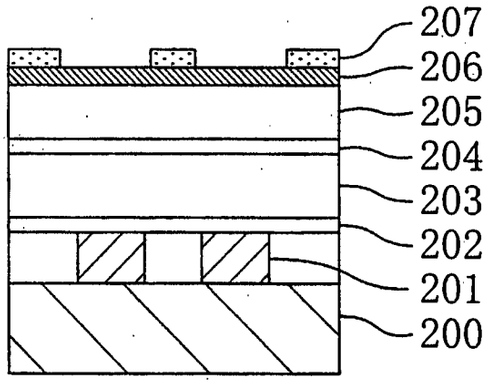

Fig. 9(c)

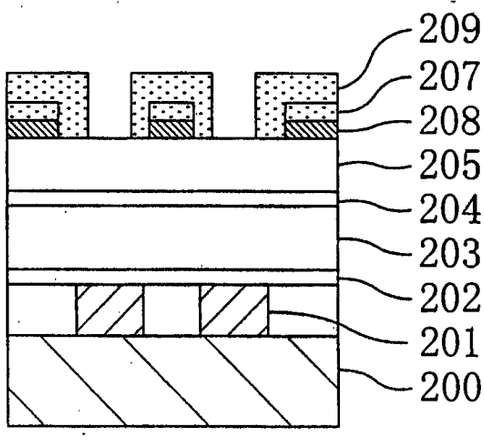

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Fig. 10(a)

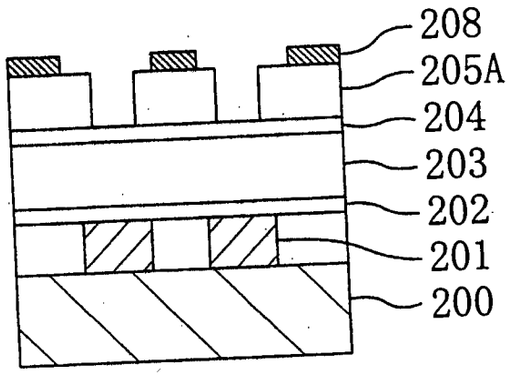

Fig. 10(b)

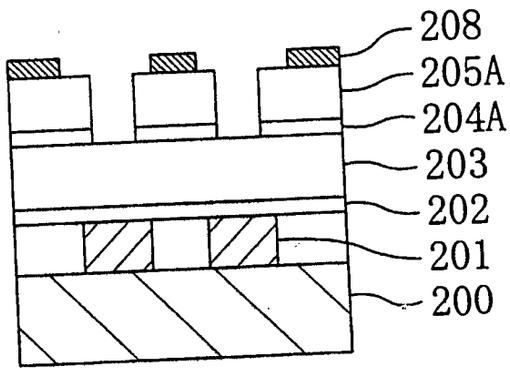

Fig. 10(c)

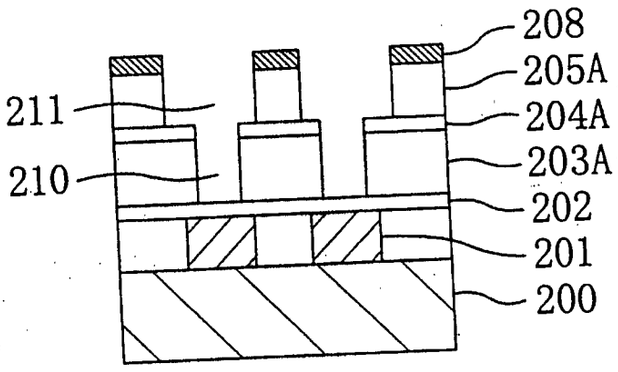

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Fig. 11(a)

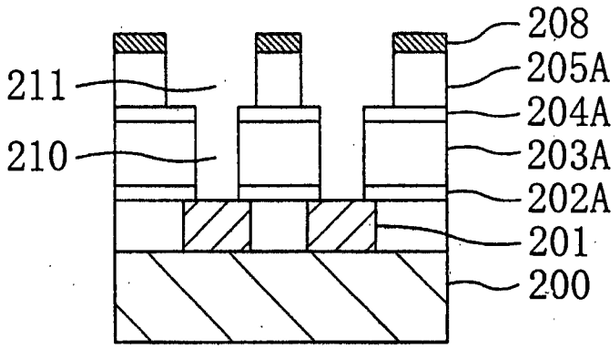

Fig. 11(b)

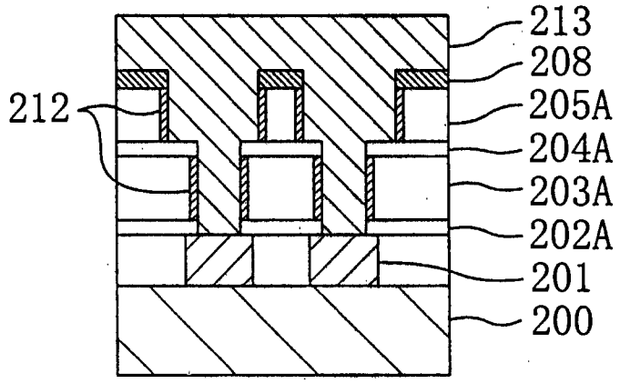

Fig. 11(c)

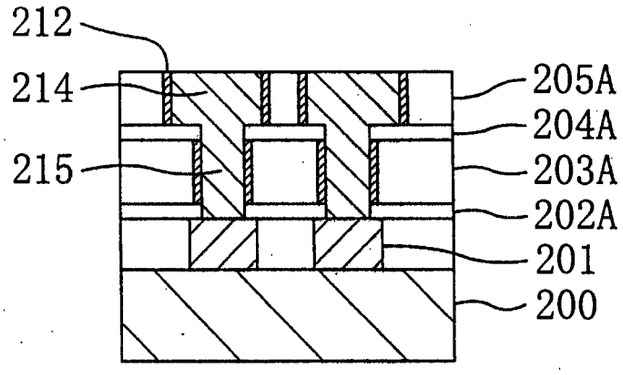

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Fig. 12(a)

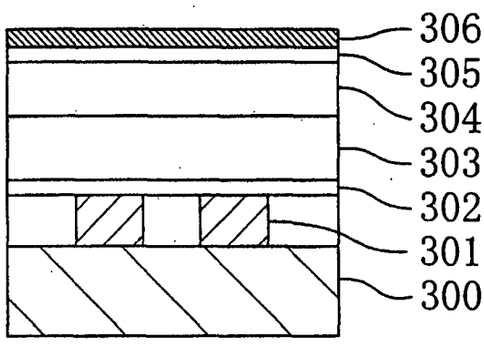


Fig. 12(b)

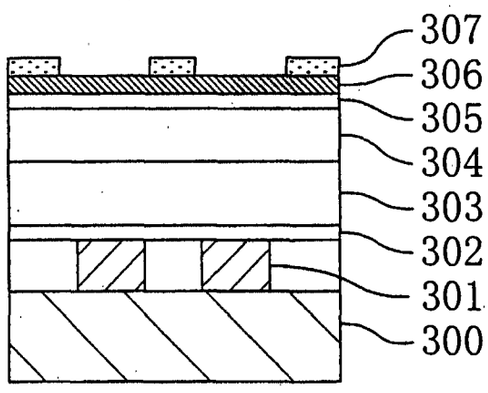
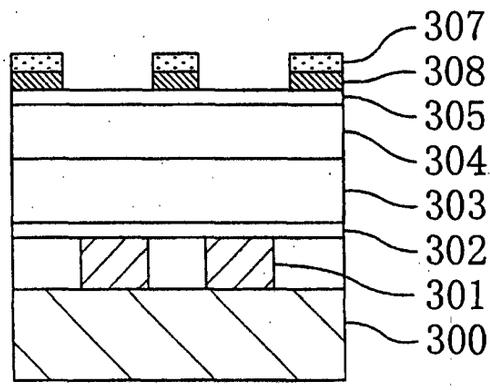


Fig. 12(c)



PRINT OF DRAWINGS
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Fig. 13(a)

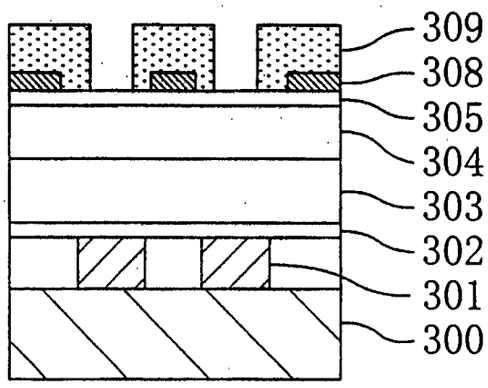


Fig. 13(b)

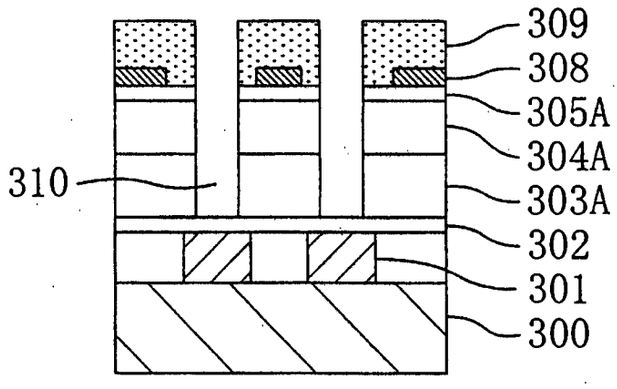
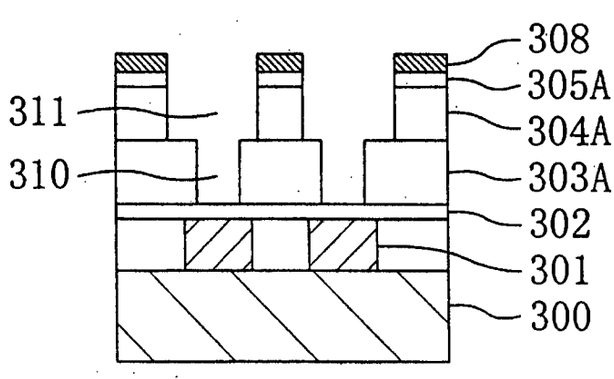


Fig. 13(c)



PRINT OF DRAWINGS
AS ORIGINALLY FILE

Fig. 14(a)

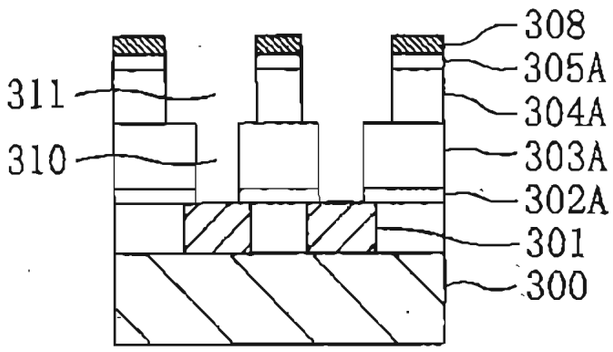


Fig. 14(b)

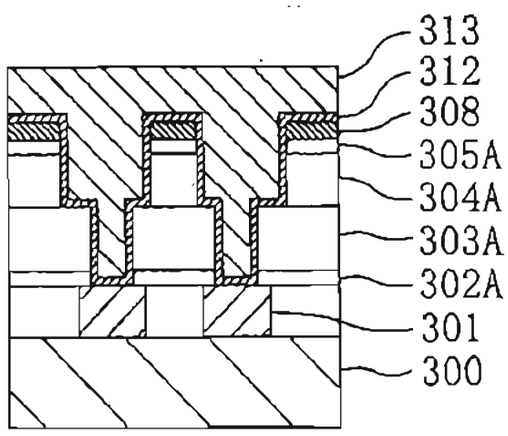
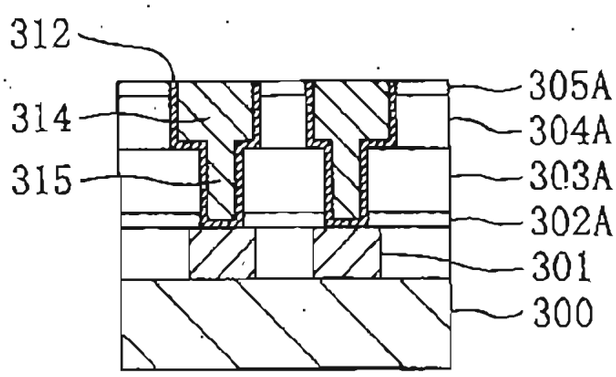


Fig. 14(c)



PRINT OF DRAWINGS
AS ORIGINALLY FILE

Fig. 15(a)

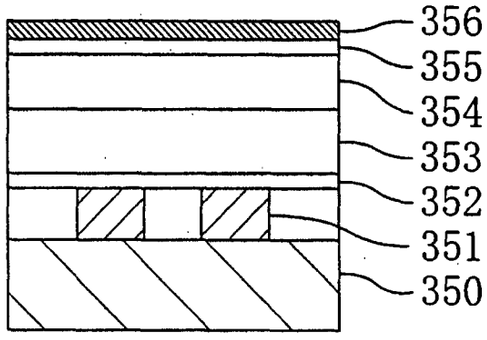


Fig. 15(b)

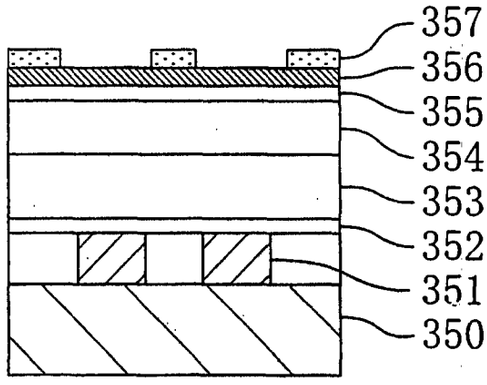
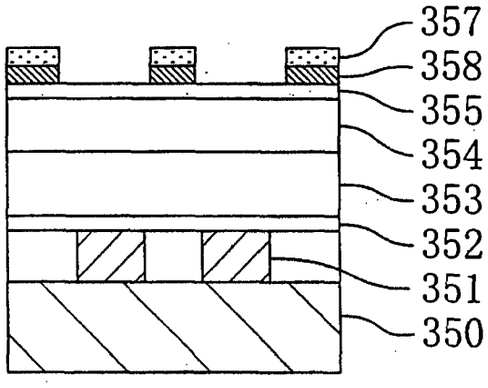


Fig. 15(c)



PRINT OF DRAWINGS
AS ORIGINALLY FILE

Fig. 16(a)

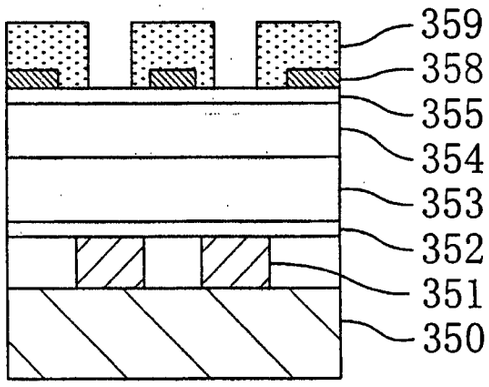


Fig. 16(b)

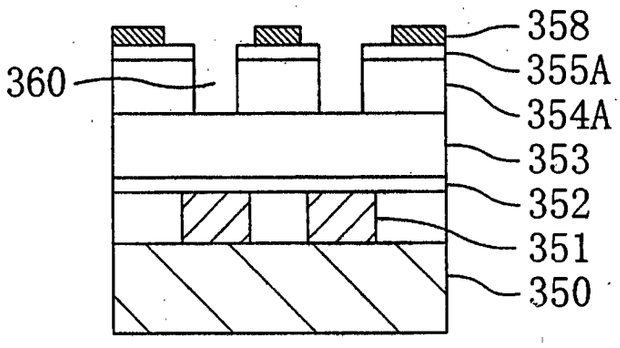


Fig. 16(c)

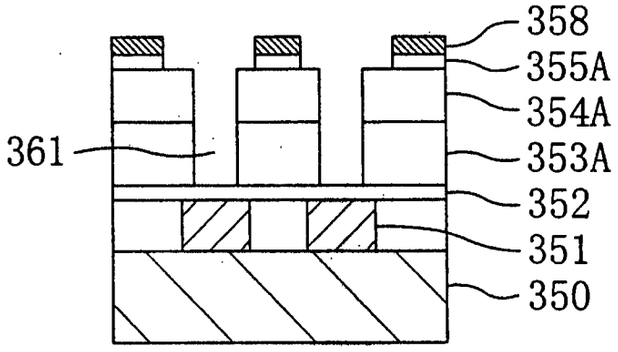
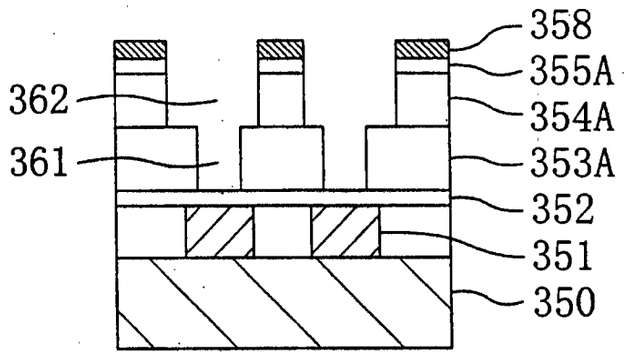


Fig. 16(d)



PRINT OF DRAWINGS
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Fig. 17(a)

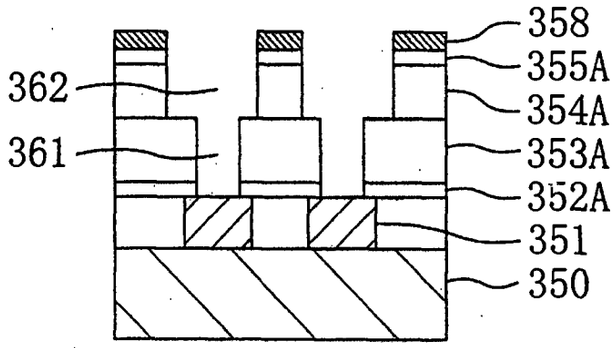

Fig. 17(b)

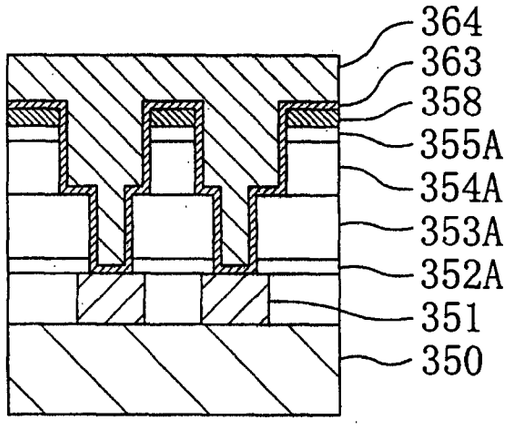

Fig. 17(c)

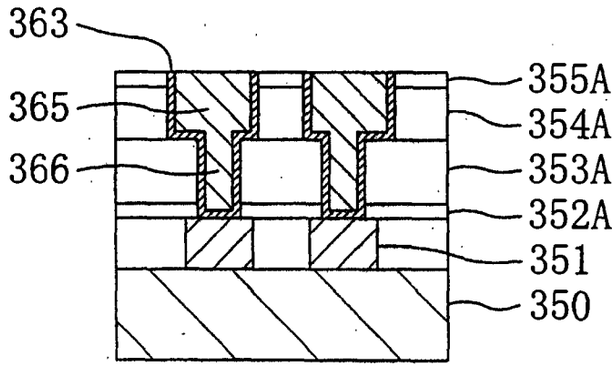

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Fig. 18(a)

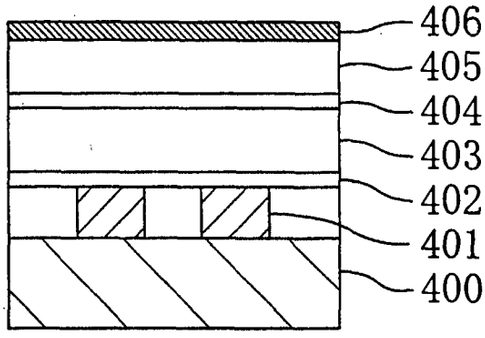

Fig. 18(b)

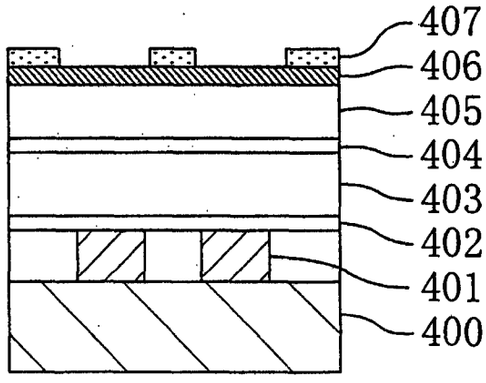

Fig. 18(c)

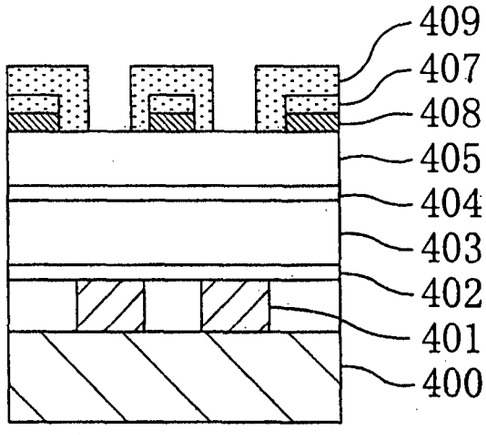

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Fig. 19(a)

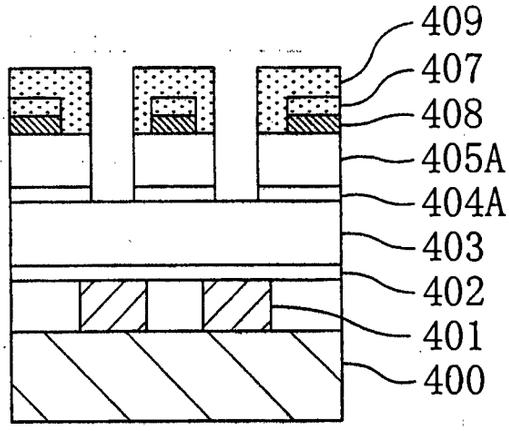

Fig. 19(b)

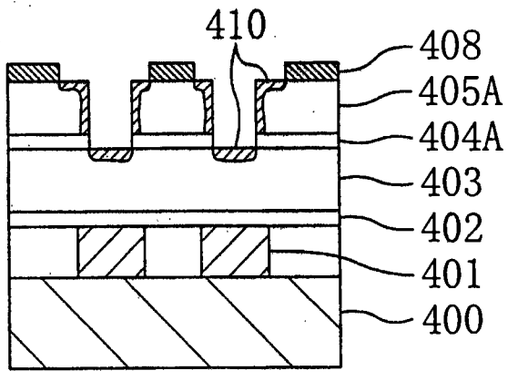

Fig. 19(c)

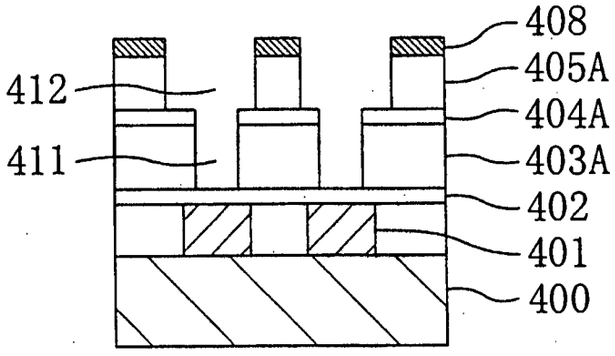

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Fig. 20(a)

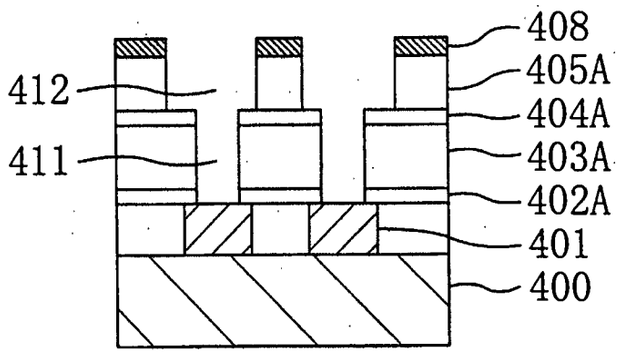

Fig. 20(b)

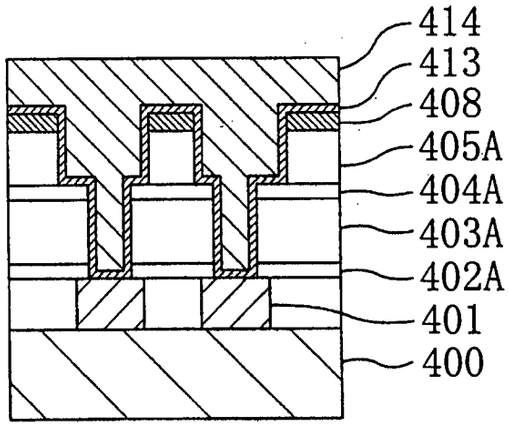

Fig. 20(c)

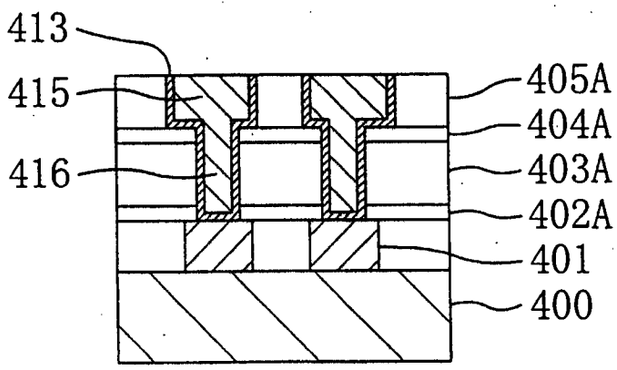

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Fig. 21(a)

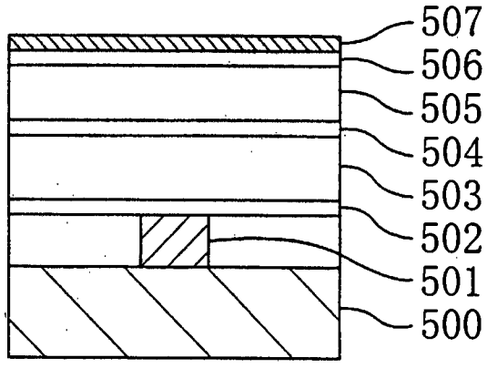

Fig. 21(b)

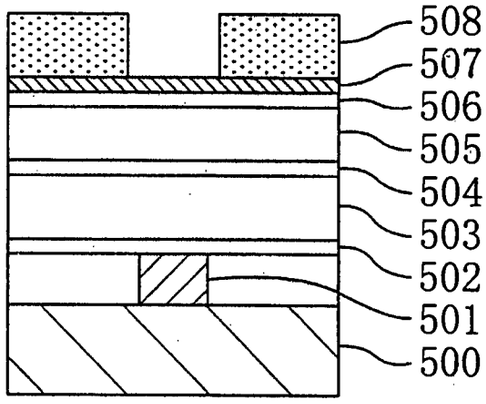

Fig. 21(c)

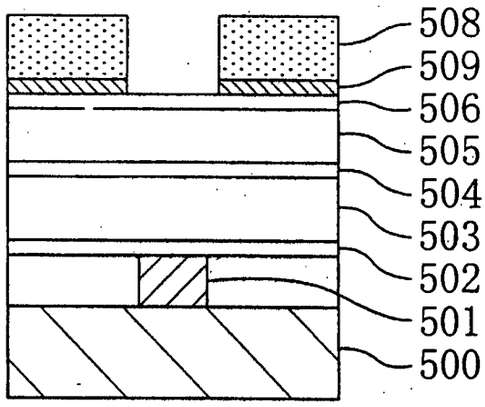

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Fig. 22(a)

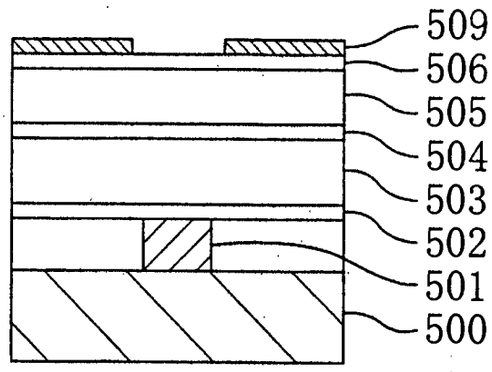

Fig. 22(b)

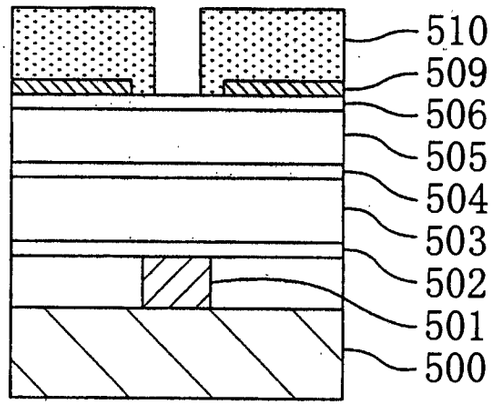

Fig. 22(c)

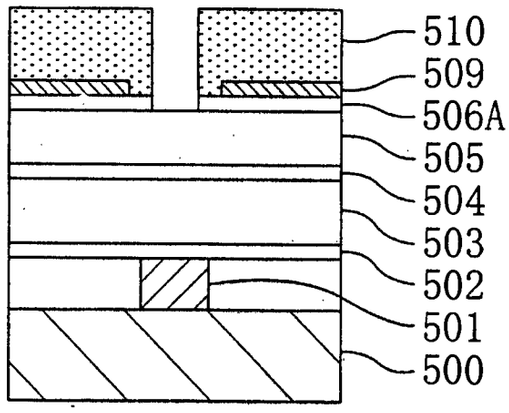

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Fig. 23(a)

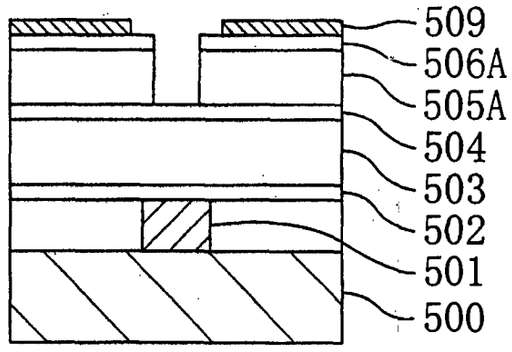

Fig. 23(b)

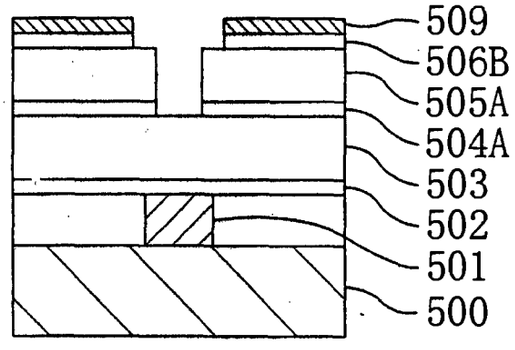

Fig. 23(c)

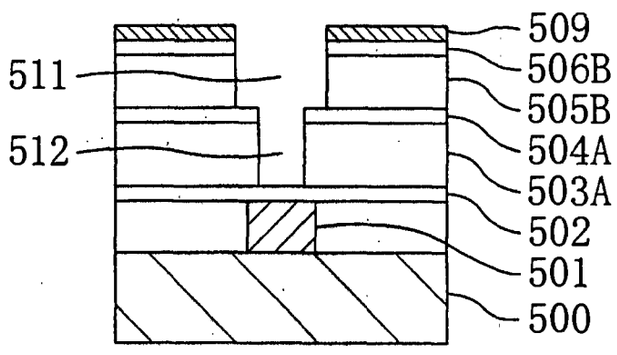

Fig. 23(d)

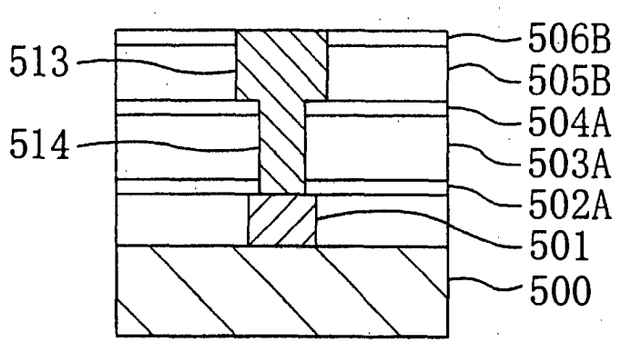

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Fig. 24(a)

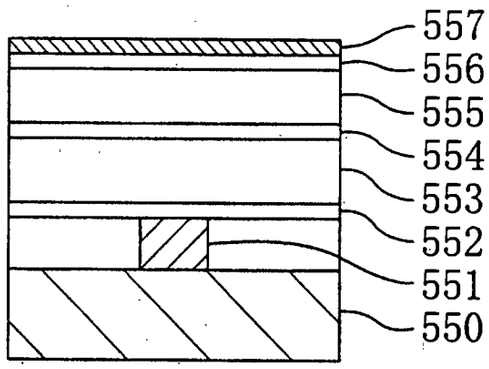

Fig. 24(b)

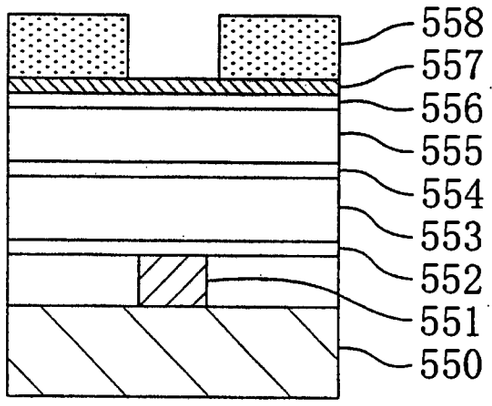

Fig. 24(c)

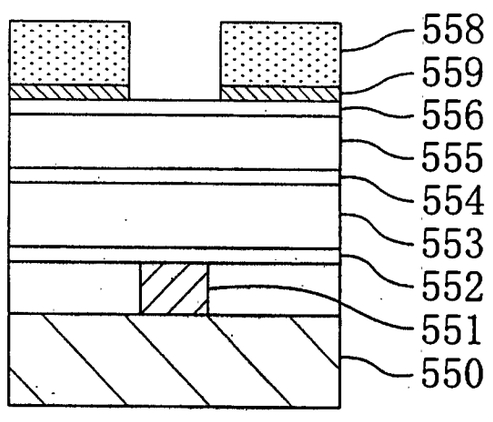

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Fig. 25(a)

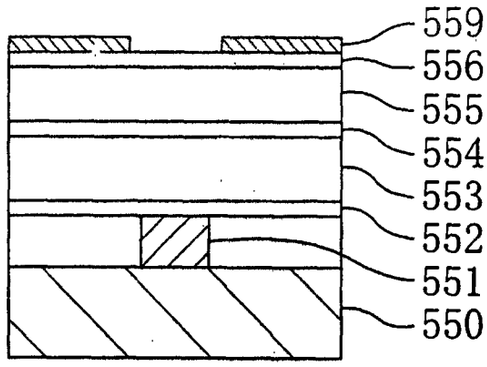

Fig. 25(b)

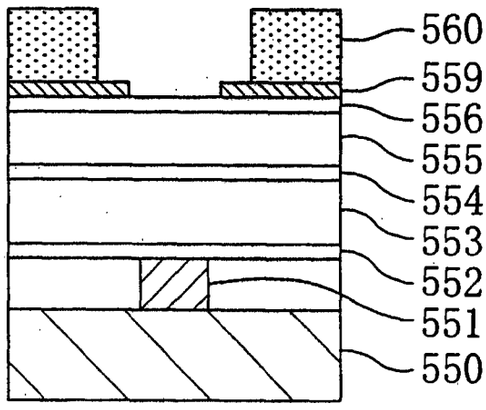

Fig. 25(c)

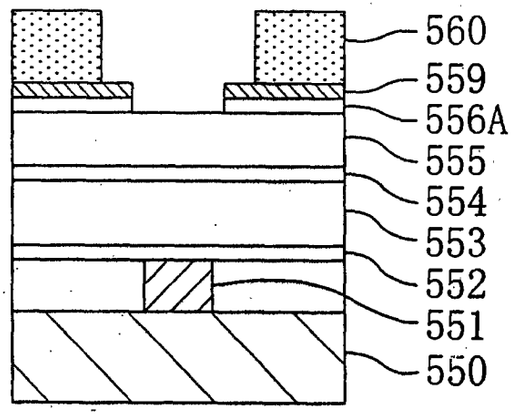

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Fig. 26(a)

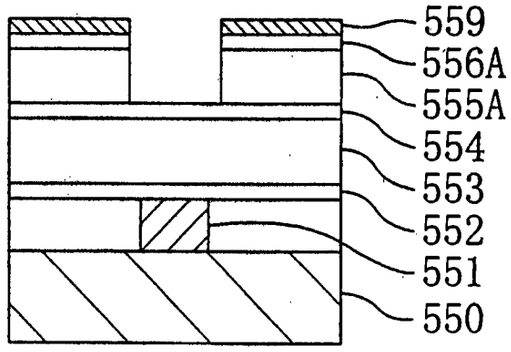

Fig. 26(b)

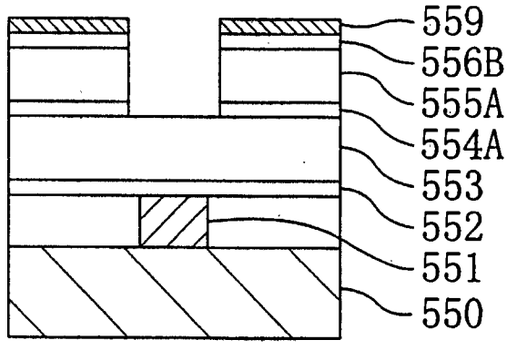

Fig. 26(c)

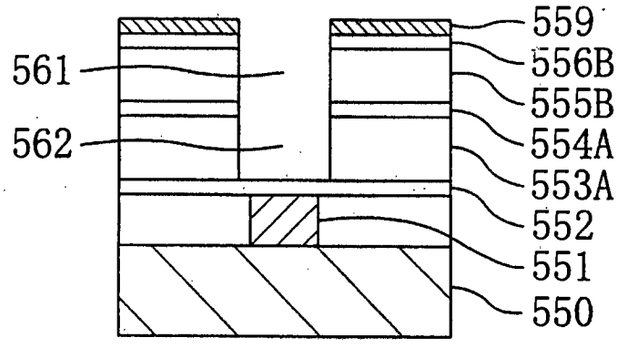

Fig. 26(d)

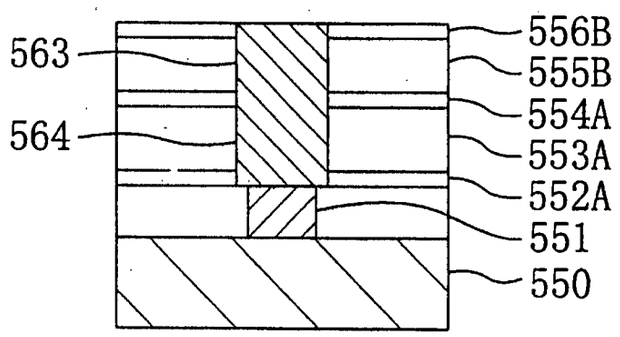

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Fig. 27(a)

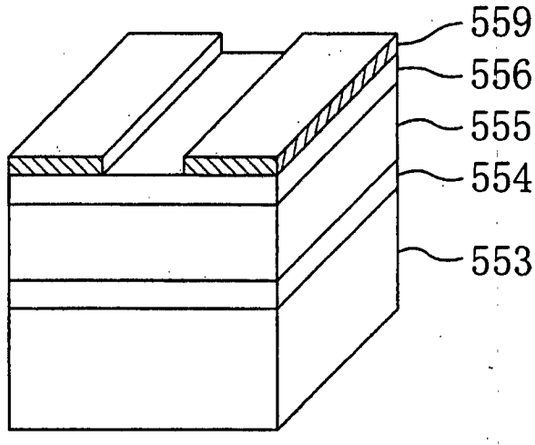

Fig. 27(b)

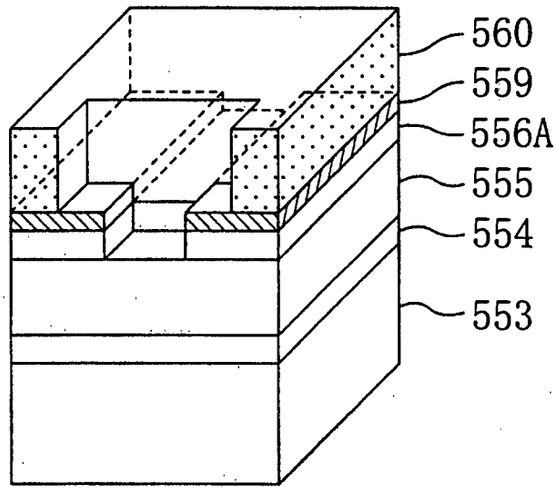

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Fig. 28(a)

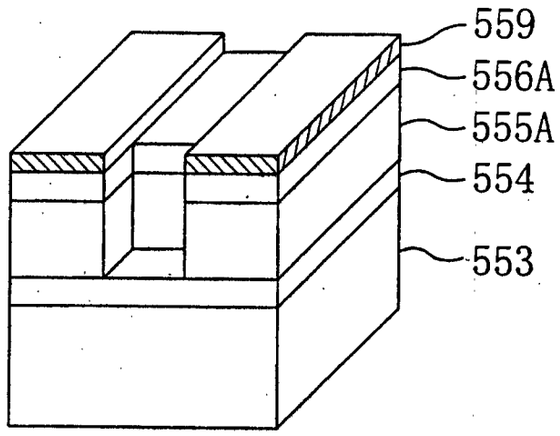

Fig. 28(b)

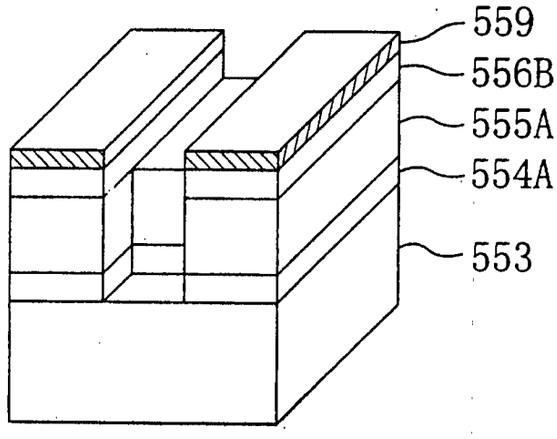

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Fig. 29(a)

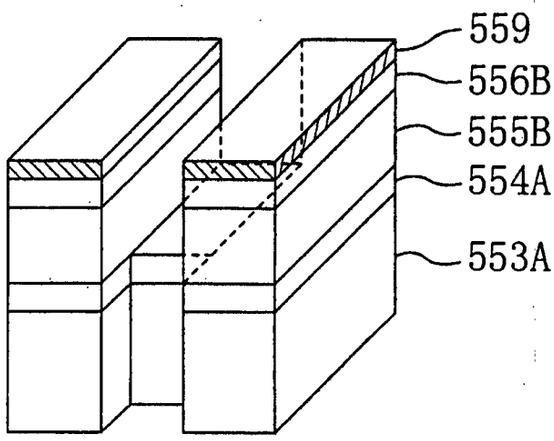
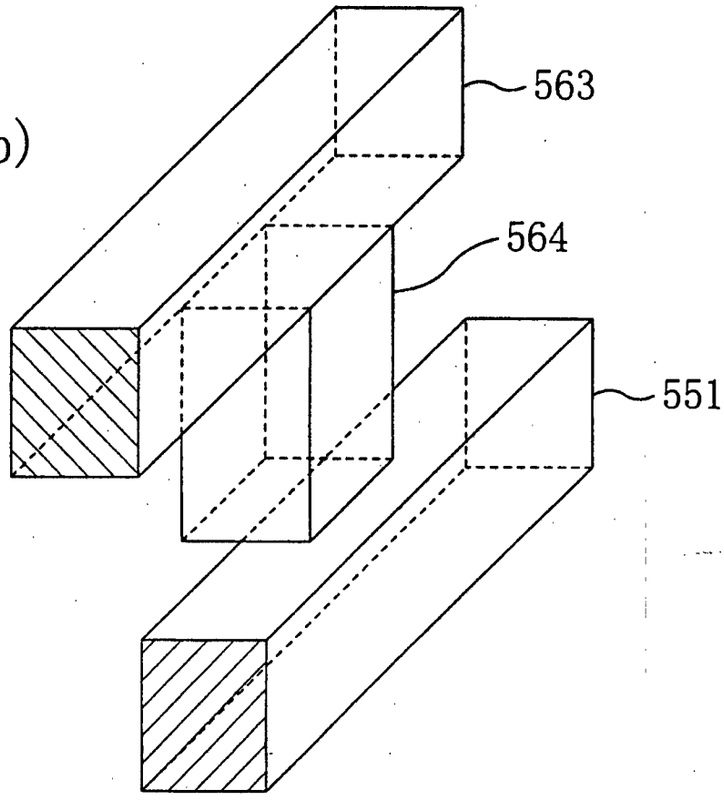


Fig. 29(b)



PRINT OF DRAWINGS
AS ORIGINALLY FILE

Fig. 30(a)

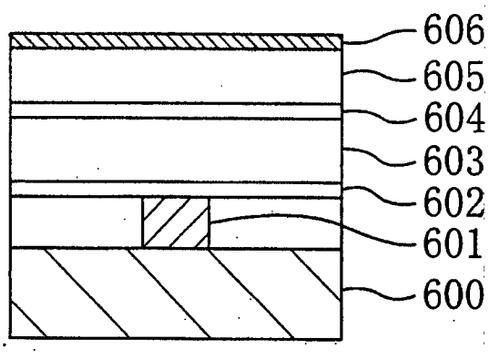


Fig. 30(b)

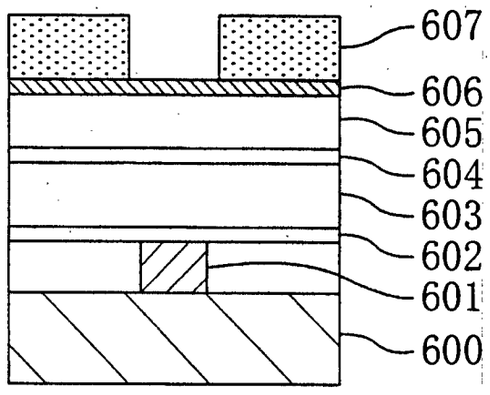
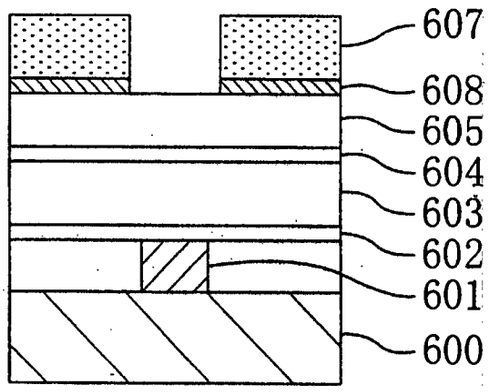


Fig. 30(c)



PRINT OF DRAWINGS
AS ORIGINALLY FILE

Fig. 31(a)

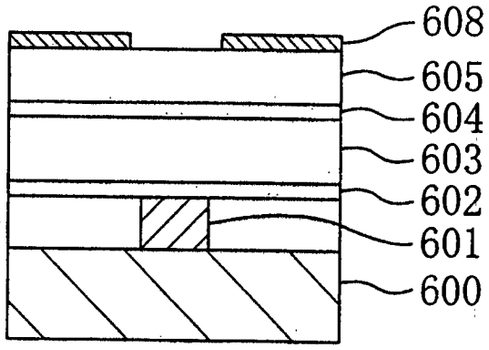


Fig. 31(b)

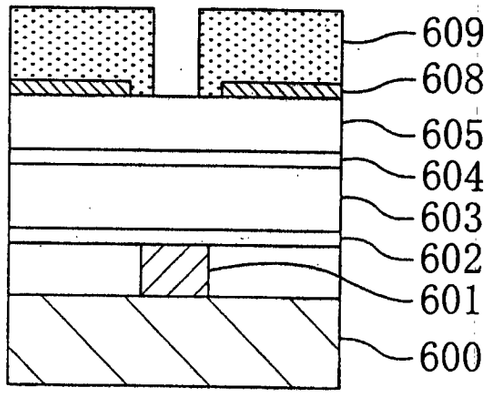
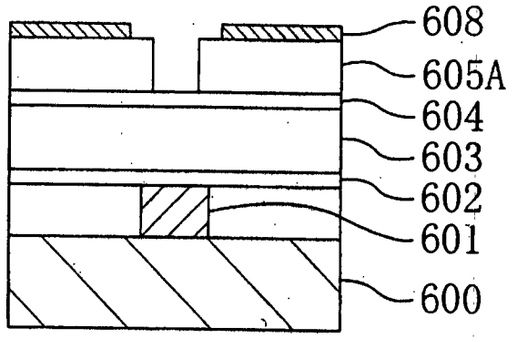


Fig. 31(c)



PRINT OF DRAWINGS
AS ORIGINALLY FILE

Fig. 32(a)

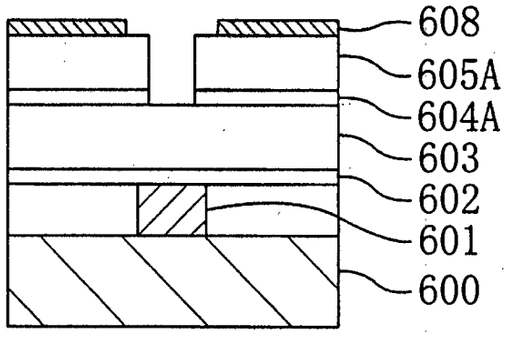


Fig. 32(b)

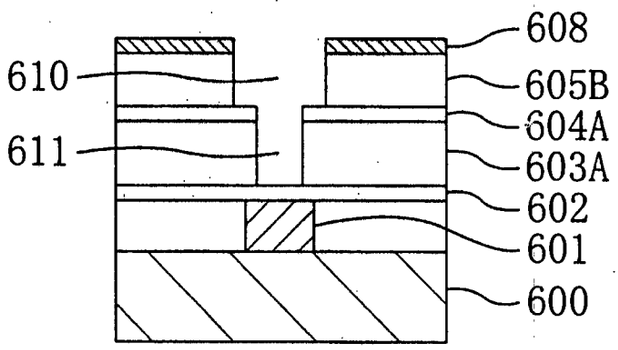
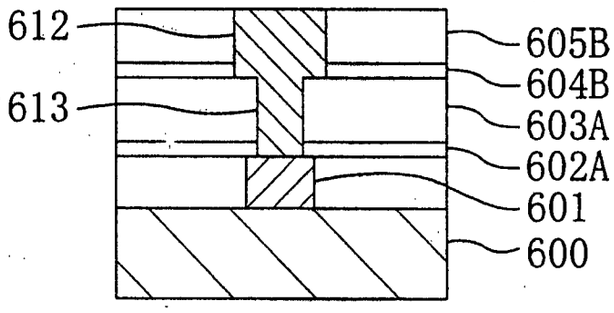


Fig. 32(c)



PRINT OF DRAWINGS
AS ORIGINALLY FILE

Fig. 33(a)

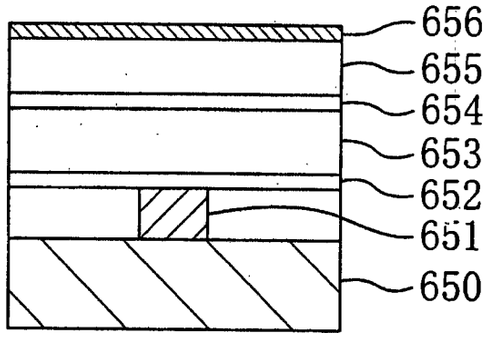


Fig. 33(b)

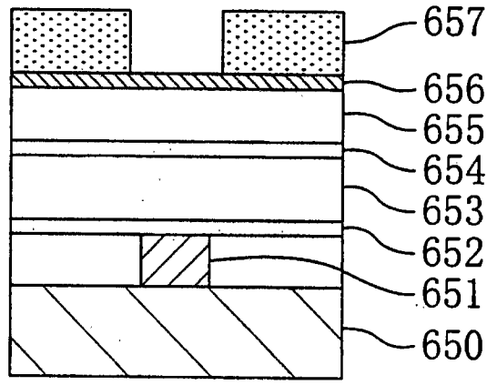
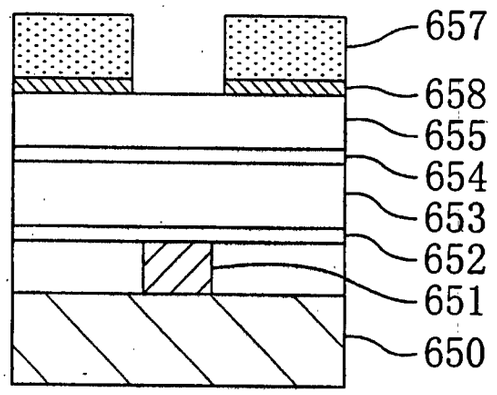


Fig. 33(c)



PRINT OF DRAWINGS
AS ORIGINALLY FILE

Fig. 34(a)

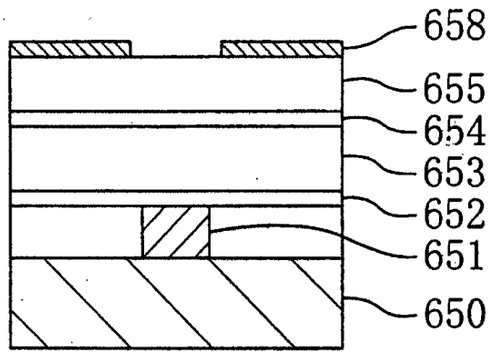


Fig. 34(b)

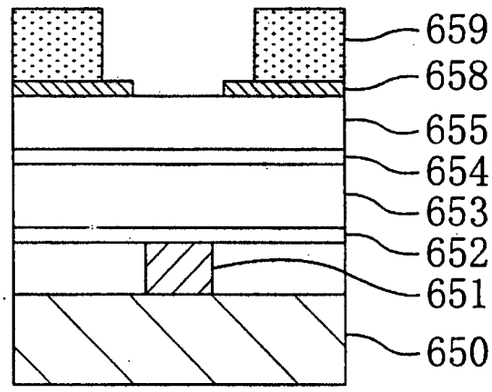
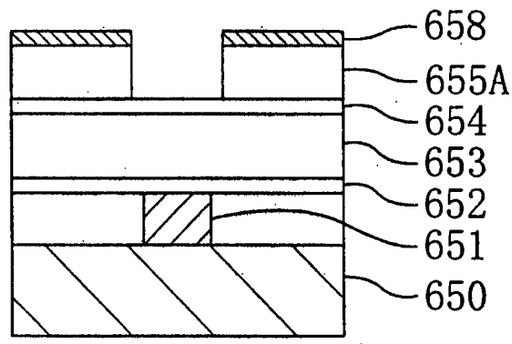


Fig. 34(c)



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AS ORIGINALLY FILI

Fig. 35(a)

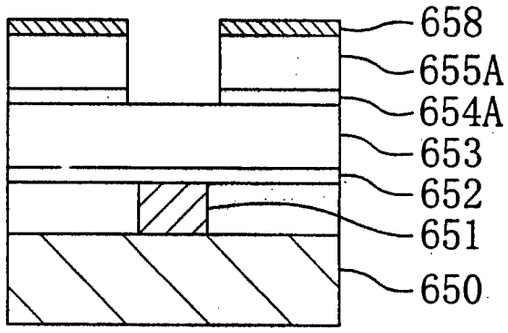


Fig. 35(b)

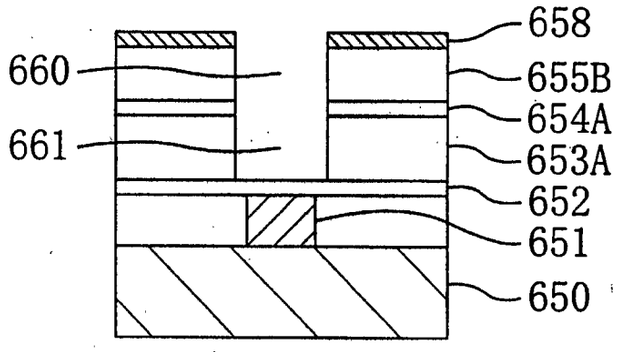
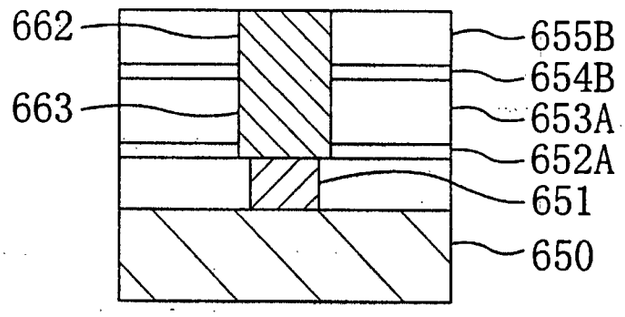
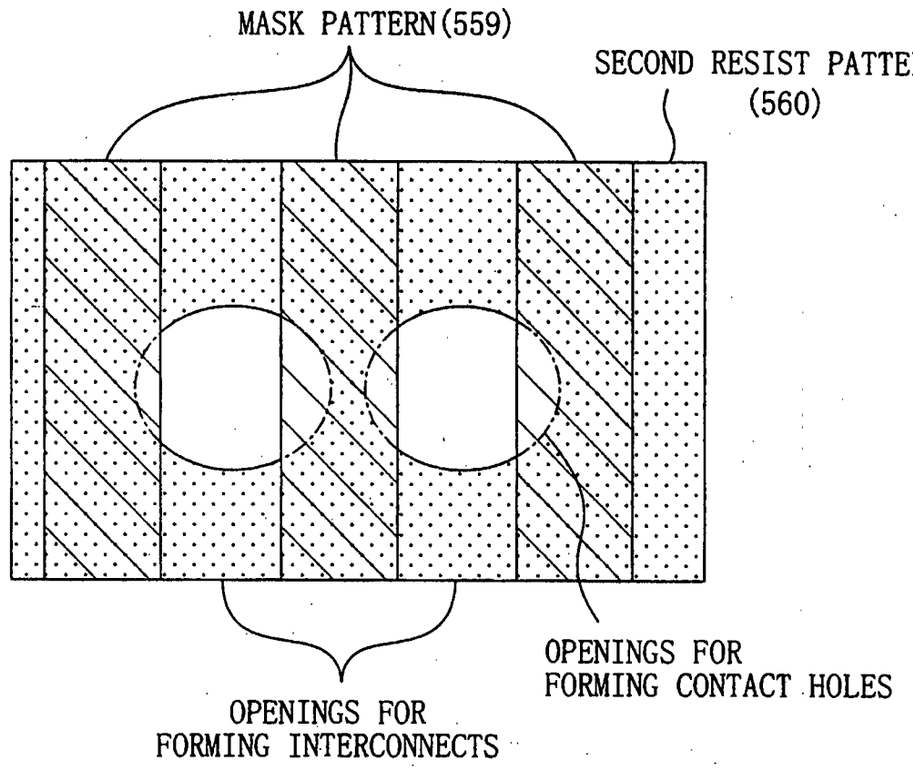


Fig. 35(c)



PRINT OF DRAWINGS
AS ORIGINALLY FILE

Fig. 36



PRINT OF DRAWINGS
AS ORIGINALLY FILE

Fig. 37(a)

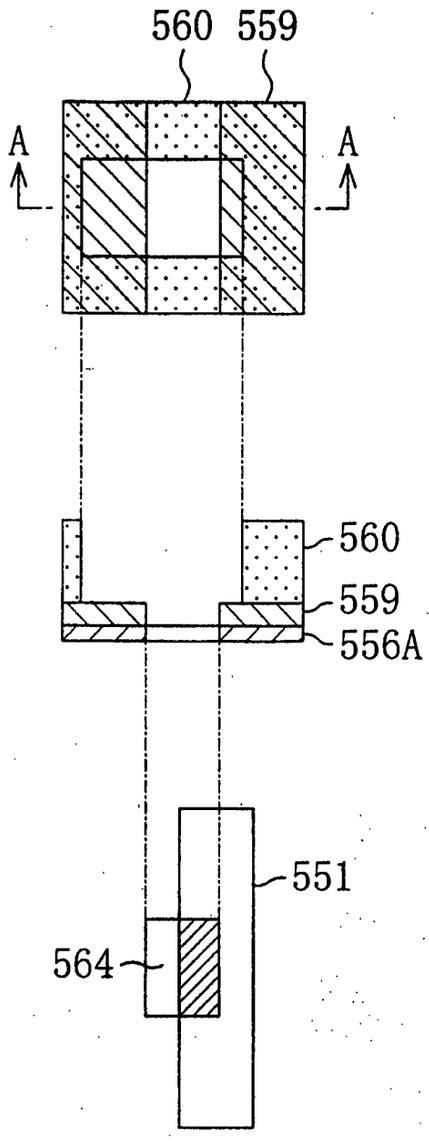
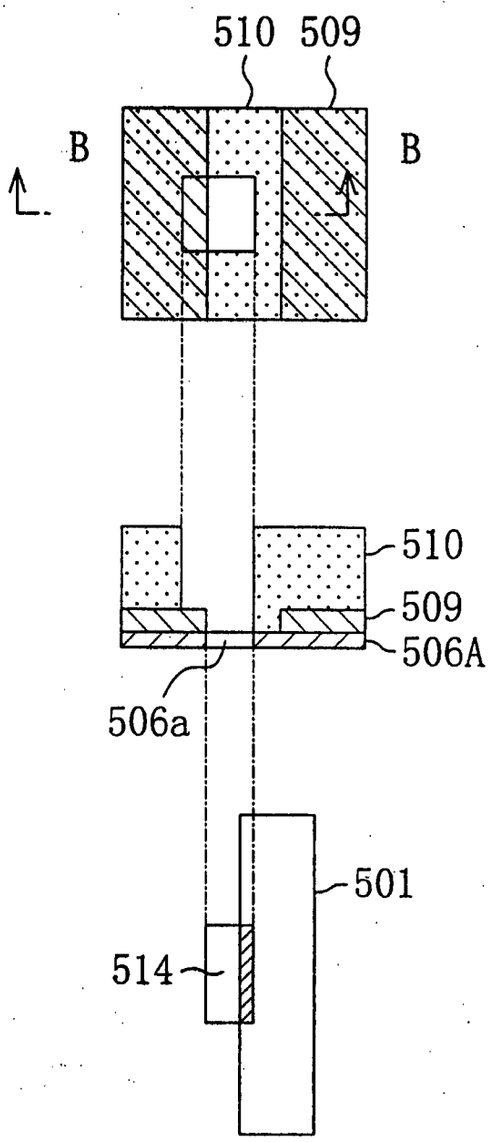


Fig. 37(b)



APPROVED BY DRAFTSMAN	O.G. FIG. 3b	
	CLASS 438	SUBCLASS 700

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Fig. 1(a)

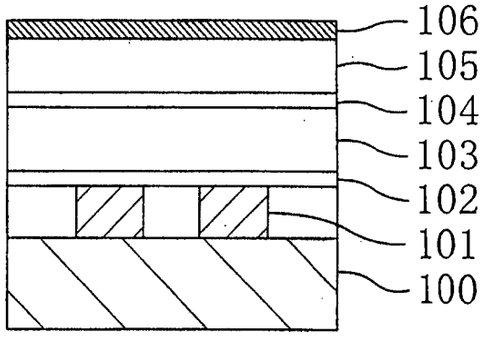


Fig. 1(b)

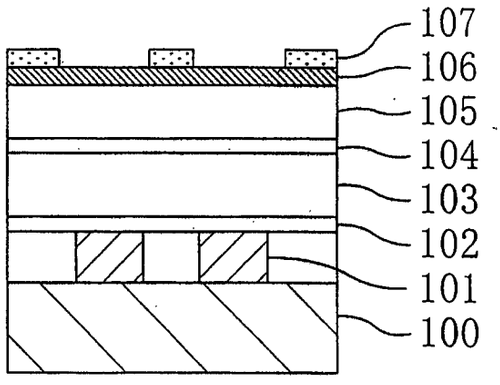
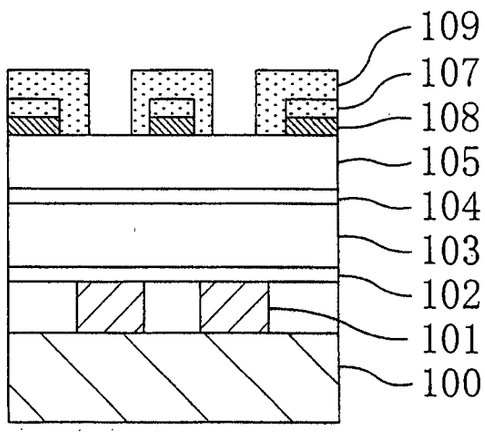


Fig. 1(c)



APPROVED BY DRAFTSMAN | O.G. FIG. 36 | CLASS 438 | SUBCLASS 700

Fig. 2(a)

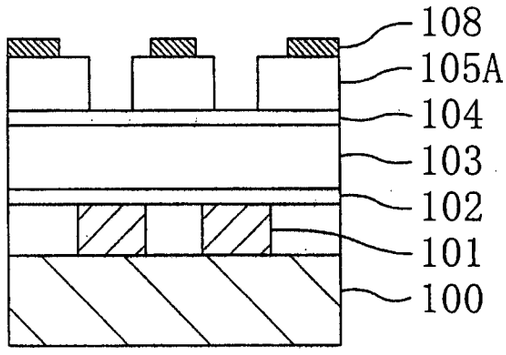


Fig. 2(b)

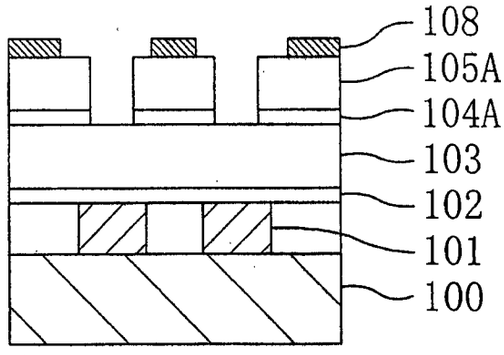
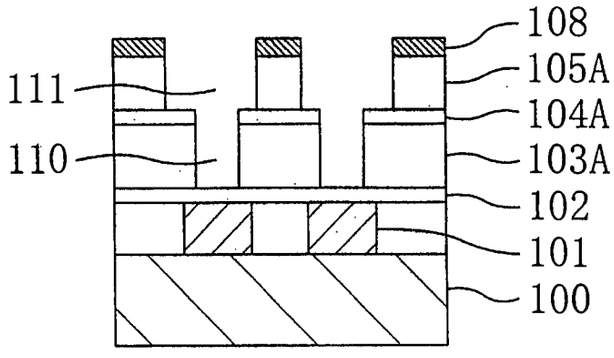


Fig. 2(c)



APPROVED BY DRAFTSMAN | O.G. FIG. 3b | CLASS 438 | SUBCLASS 700

Fig. 3(a)

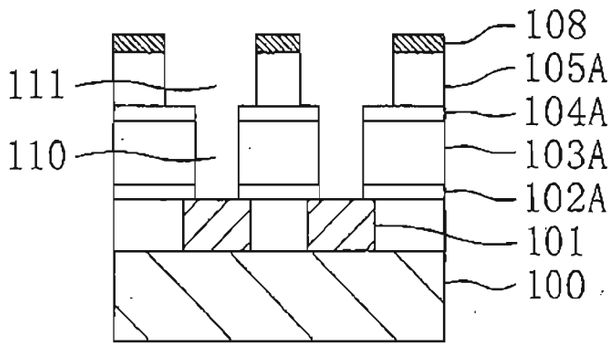


Fig. 3(b)

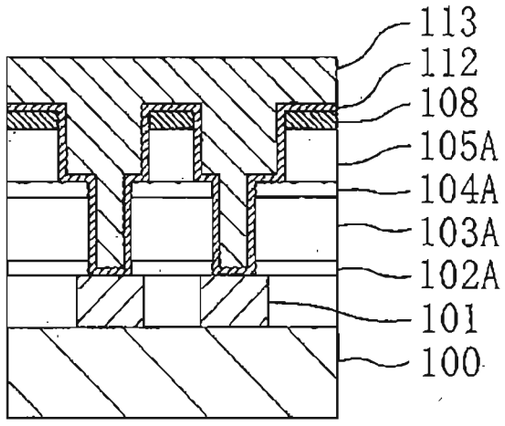
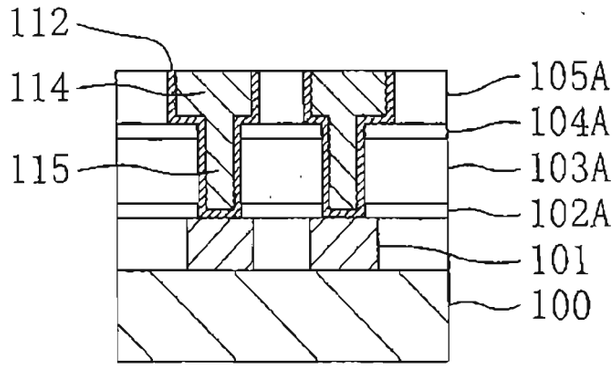


Fig. 3(c)



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APPROVED BY DRAFTSMAN	O.G. FIG. 3b	
	CLASS 438	SUBCLASS 700

Fig. 4(a)

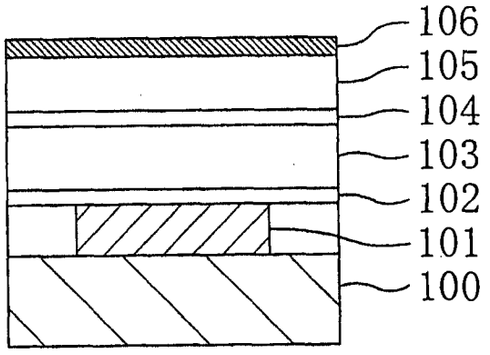


Fig. 4(b)

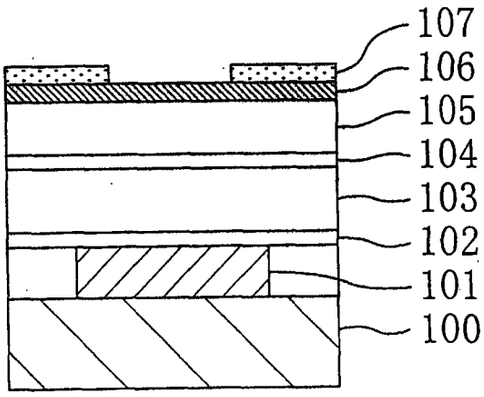
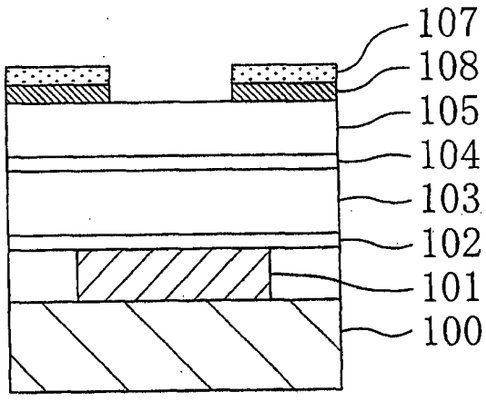


Fig. 4(c)



U.G. FIG. 3b
BY DRAFTSMAN
CLASS 436
SUBCLASS 700

Fig. 5(a)

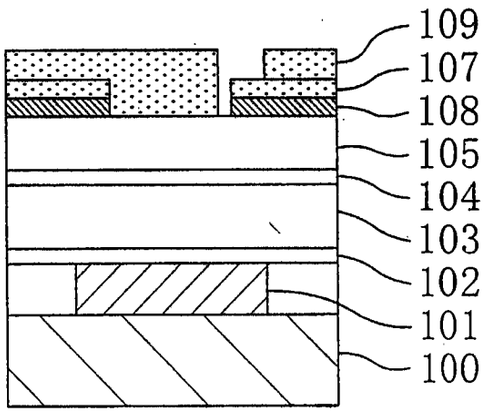


Fig. 5(b)

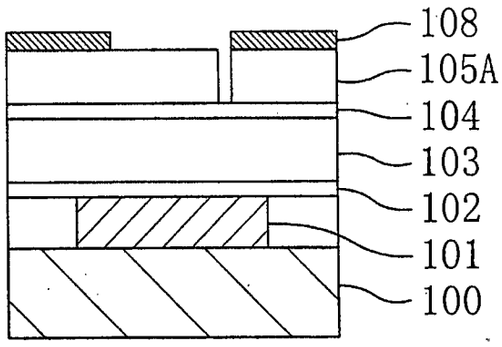
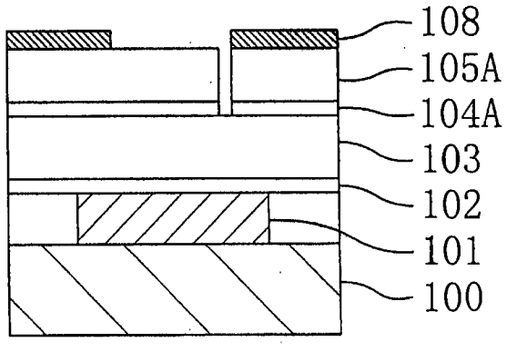


Fig. 5(c)



APPROVED BY DRAFTSMAN
O.G. FIG. 3b
CLASS 438
SUBCLASS 700

Fig. 6(a)

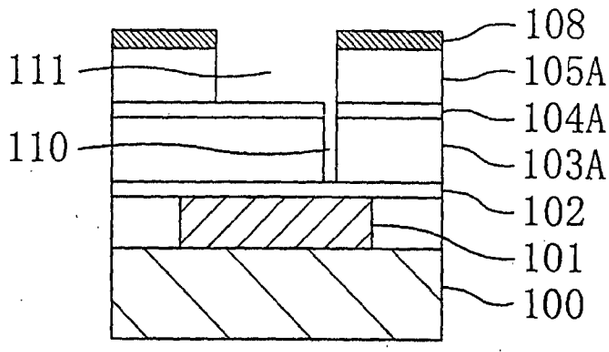


Fig. 6(b)

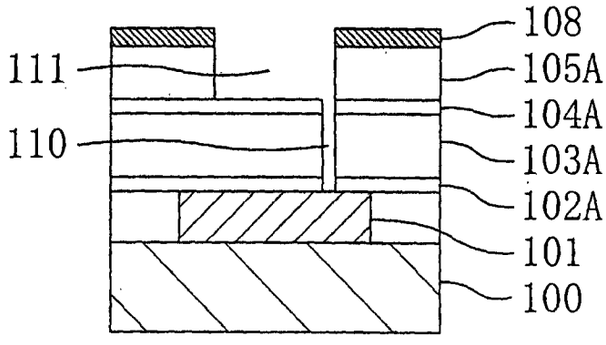
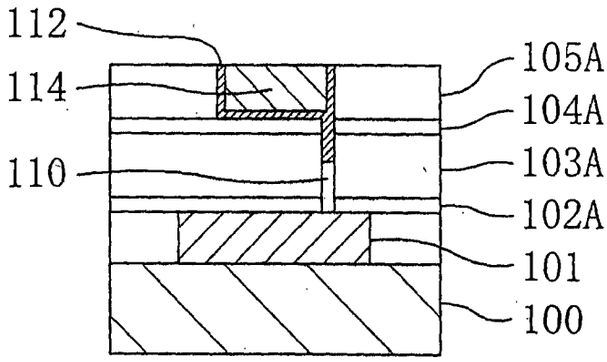


Fig. 6(c)



APPROVED BY DRAFTSMAN	O.G. FIG. 3b	
	CLASS 438	SUBCLASS 700

Fig. 7(a)

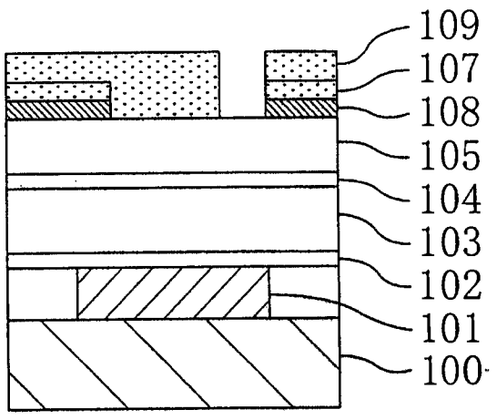


Fig. 7(b)

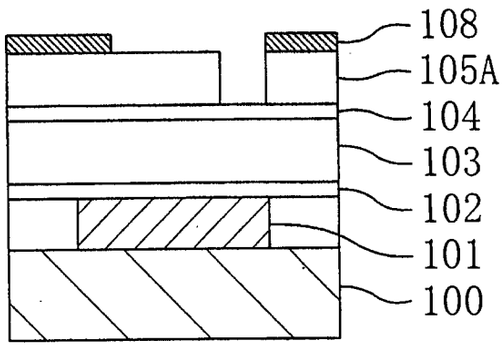
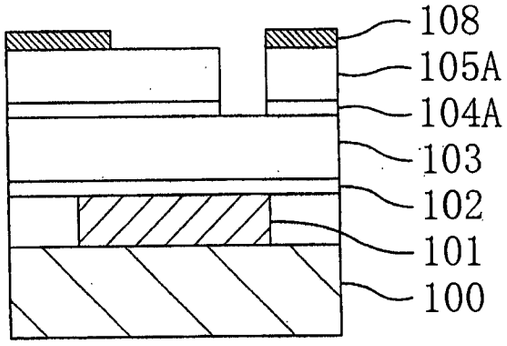


Fig. 7(c)



APPROVED BY DRAFTSMAN
O.G. FIG. 3b
CLASS 438
SUBCLASS 700

Fig. 8(a)

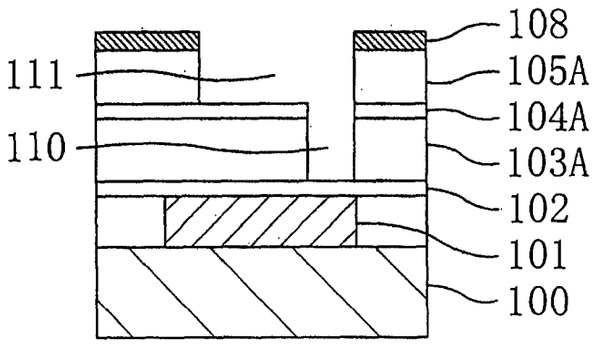


Fig. 8(b)

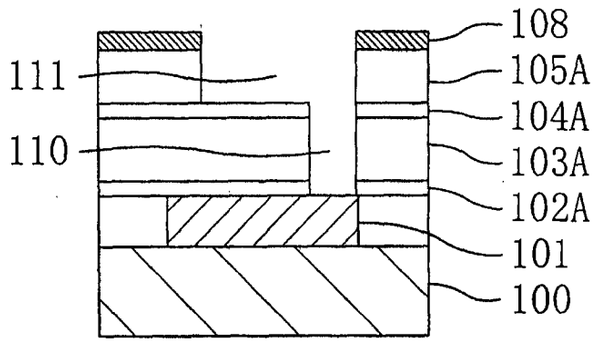
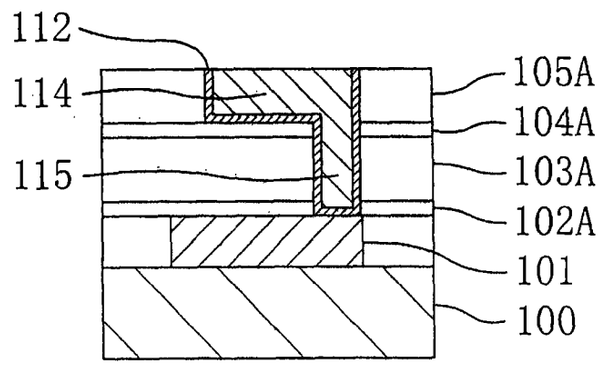


Fig. 8(c)



APPROVED BY DRAFTSMAN	O.G. FIG. 3b	
	CLASS	SUBCLASS
	438	700

Fig. 9(a)

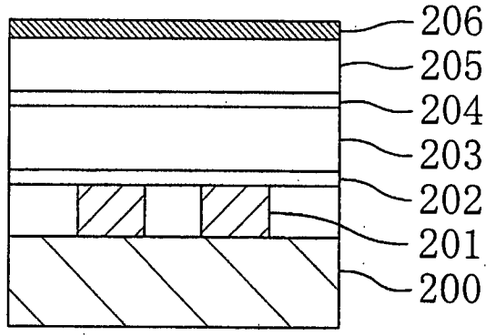


Fig. 9(b)

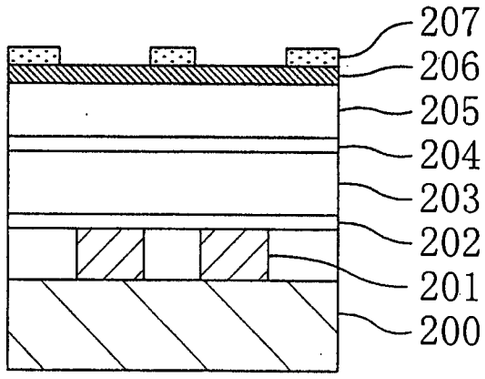
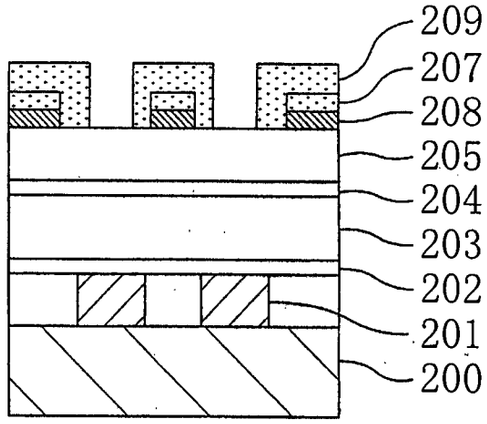


Fig. 9(c)



APPROVED BY DRAFTSMAN
O.G. FIG. 3b
CLASS 438
SUBCLASS 700

Fig. 10(a)

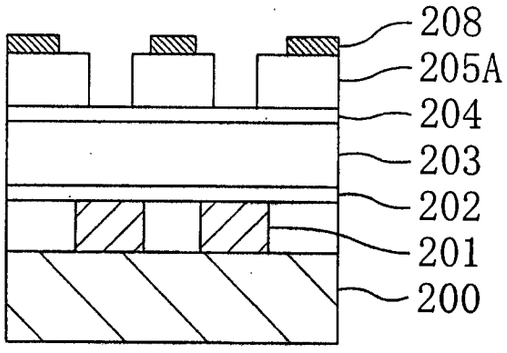


Fig. 10(b)

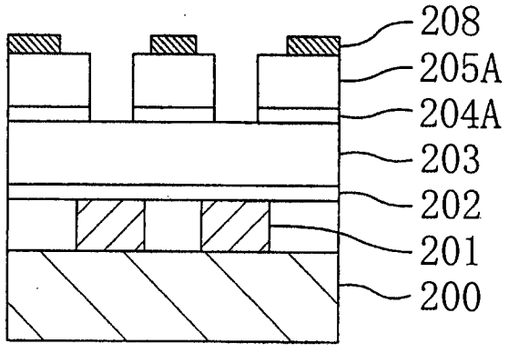
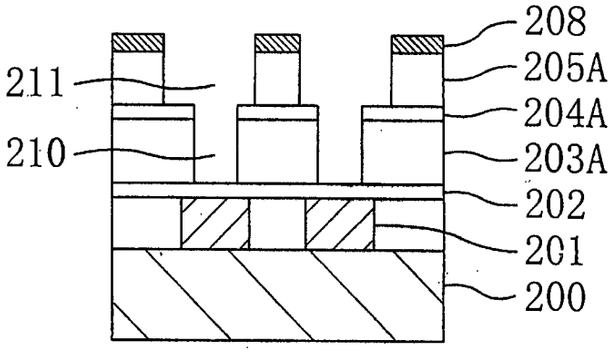


Fig. 10(c)



O.G. FIG. 3b
BY DRAFTSMAN | CLASS 438 | SUBCLASS 700

Fig. 11(a)

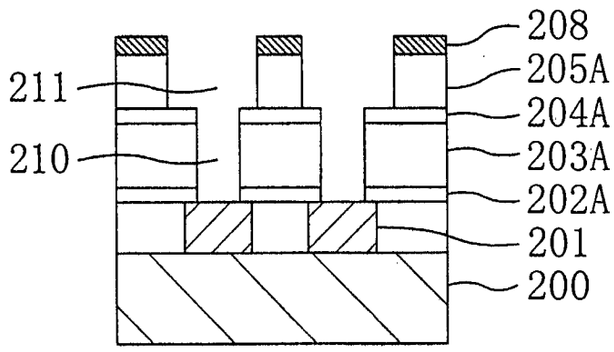


Fig. 11(b)

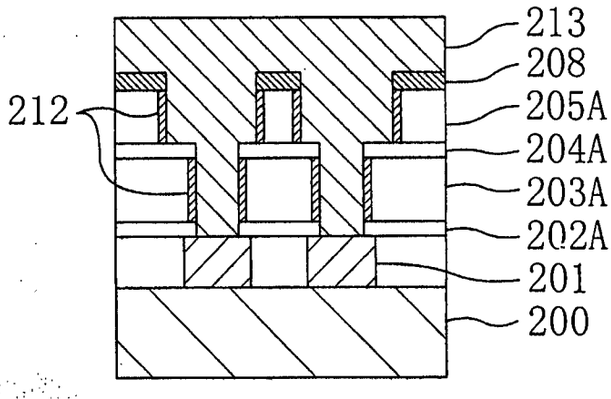
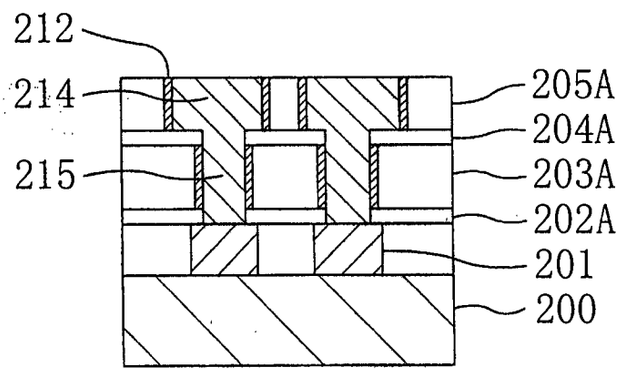


Fig. 11(c)



APPROVED BY DRAFTSMAN | O.G. FIG. 3b | CLASS 438 | SUBCLASS 700

Fig. 12(a)

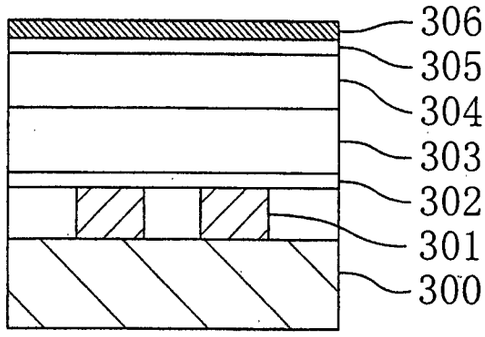


Fig. 12(b)

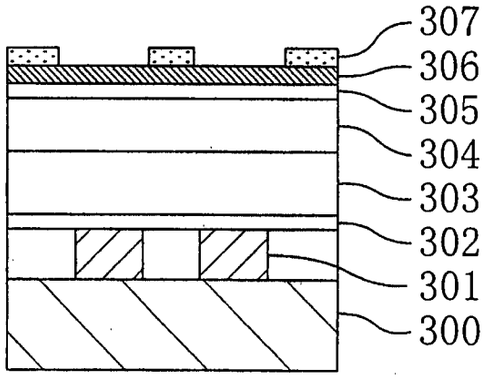
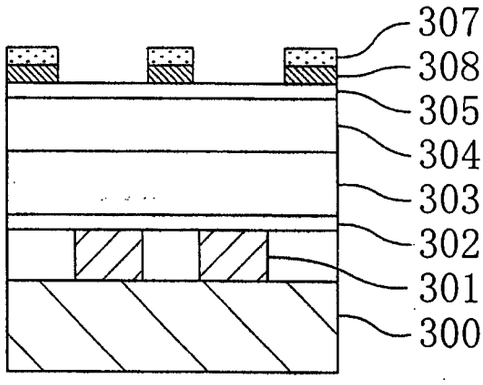


Fig. 12(c)



APPROVED BY DRAFTSMAN	O.G. FIG. 3b	
	CLASS	SUBCLASS
	438	700

Fig. 13(a)

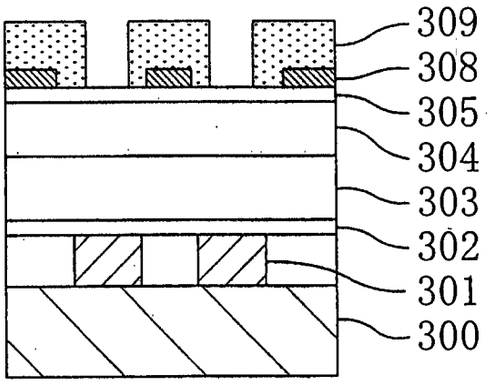


Fig. 13(b)

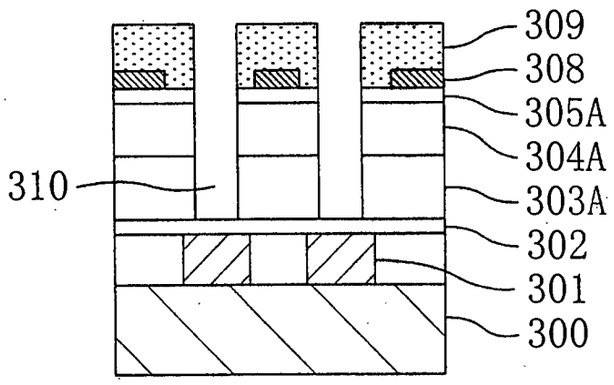
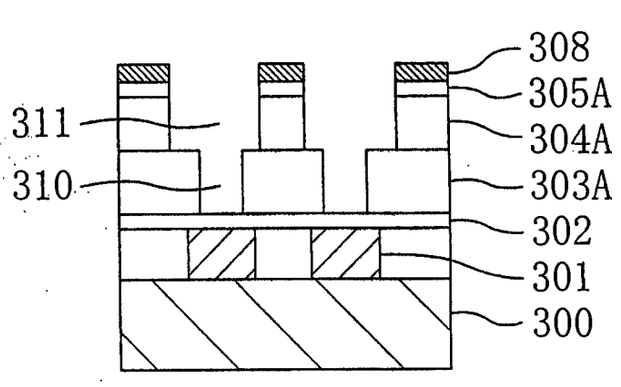


Fig. 13(c)



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O.G. FIG. 3b
CLASS 438
SUBCLASS 700

Fig. 14(a)

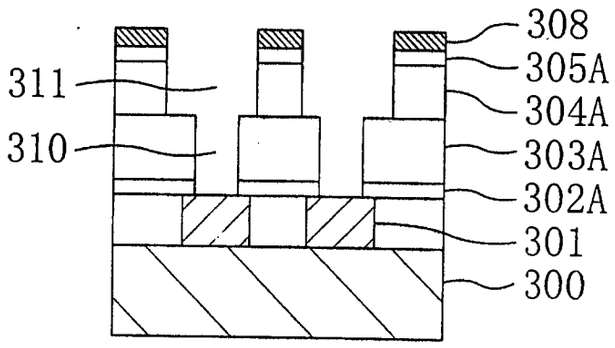


Fig. 14(b)

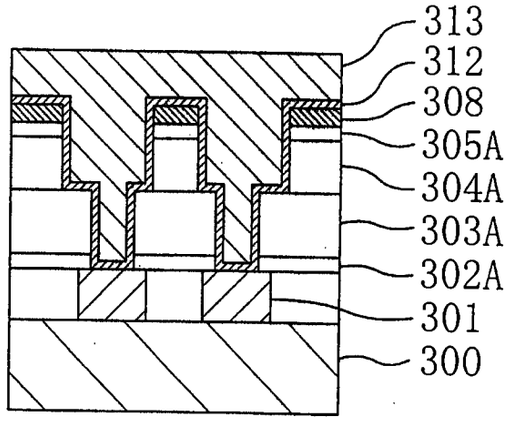
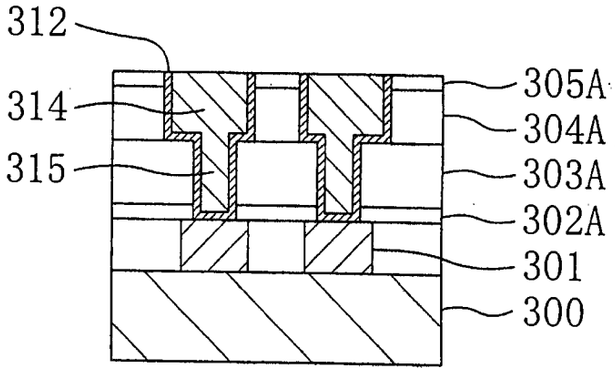


Fig. 14(c)



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O.G. FIG. 3b
CLASS 438
SUBCLASS 700

Fig. 15(a)

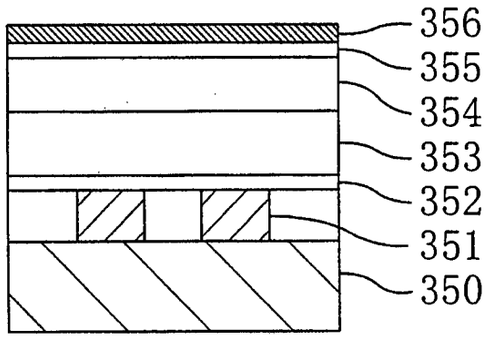


Fig. 15(b)

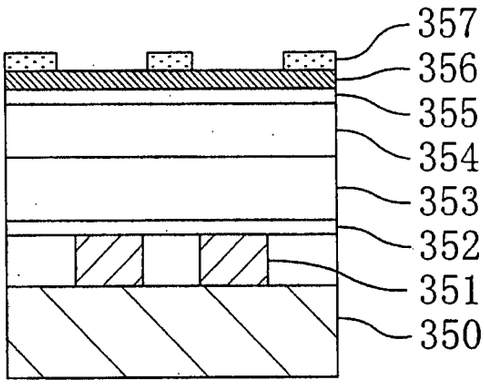
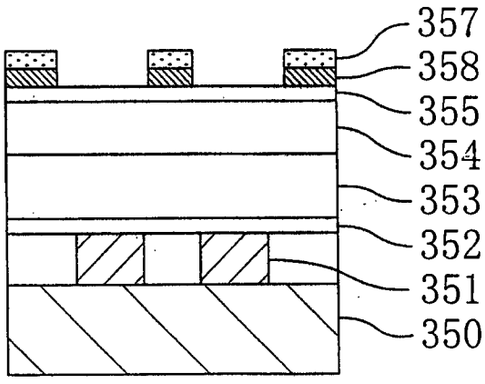


Fig. 15(c)



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D.R. FIG. 3b
CLASS 438
SUBCLASS 700

Fig. 16(a)

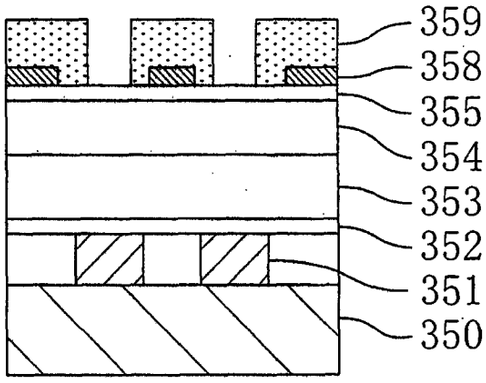


Fig. 16(b)

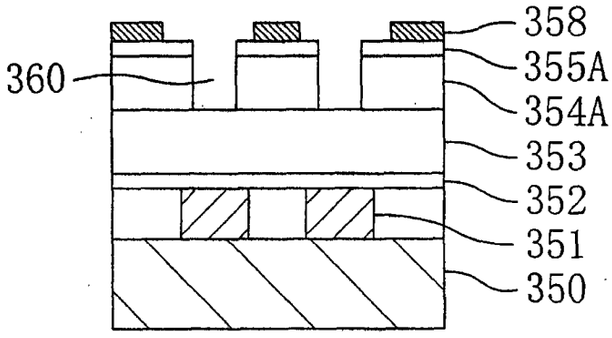


Fig. 16(c)

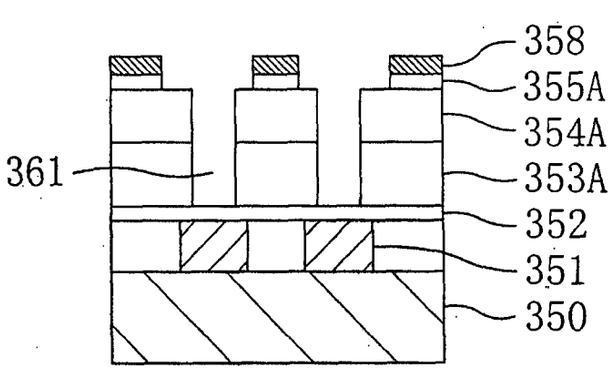
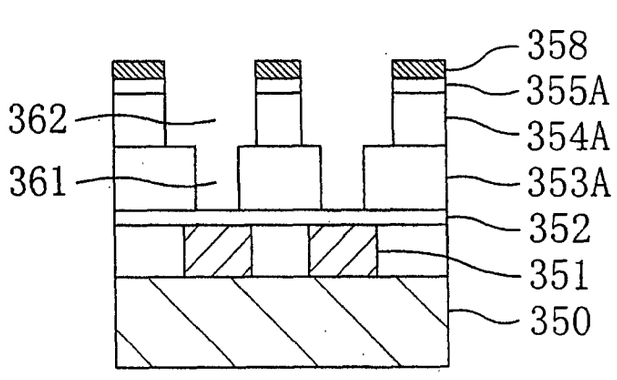


Fig. 16(d)



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O.G. FIG. 36
CLASS 438
SUBCLASS 700

Fig. 17(a)

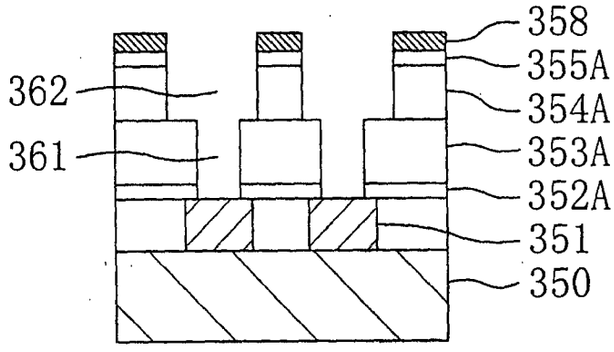


Fig. 17(b)

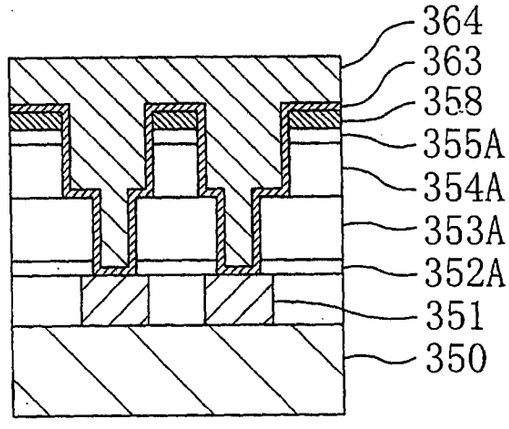
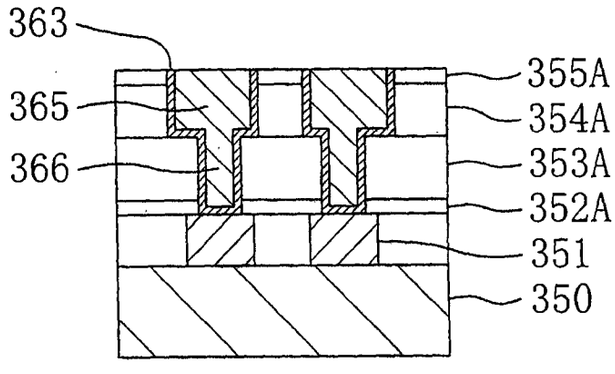


Fig. 17(c)



APPROVED BY DRAFTSMAN
O.G. FIG. 3b
CLASS 438
SUBCLASS 700

Fig. 18(a)

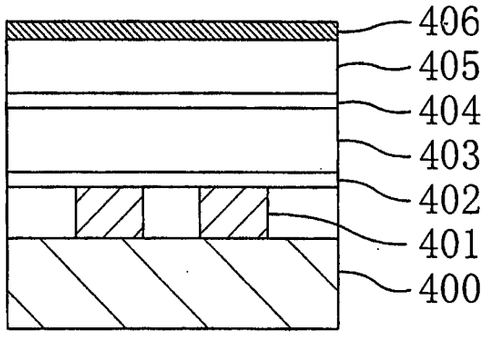


Fig. 18(b)

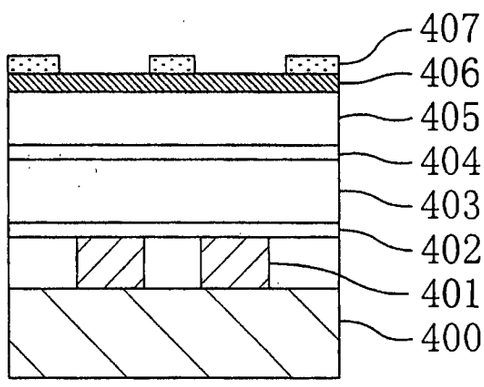
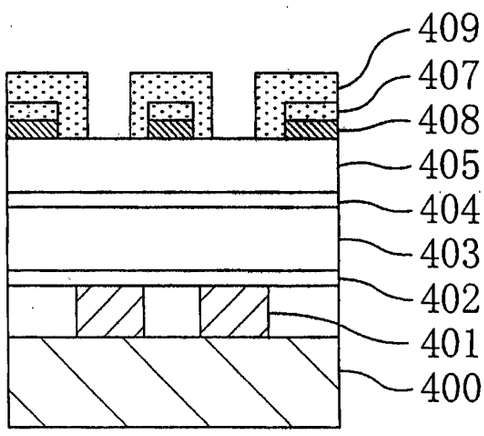


Fig. 18(c)



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O.G. FIG. 36
CLASS 438
SUBCLASS 700

Fig. 19(a)

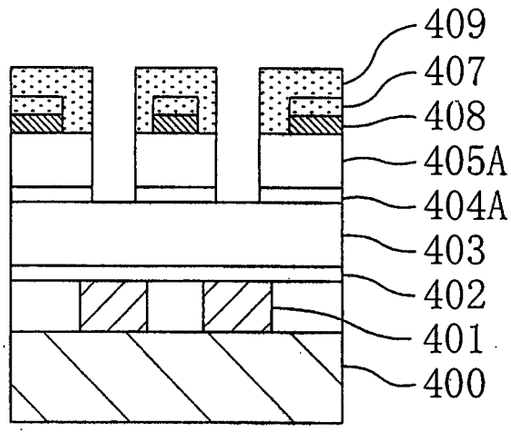


Fig. 19(b)

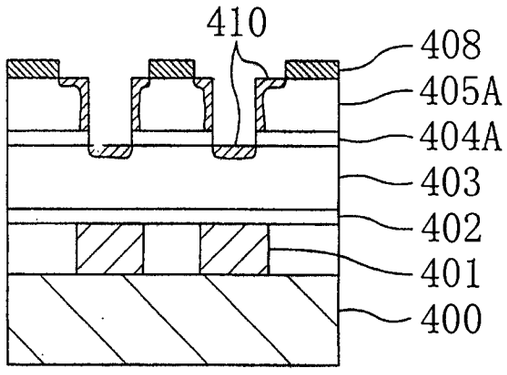
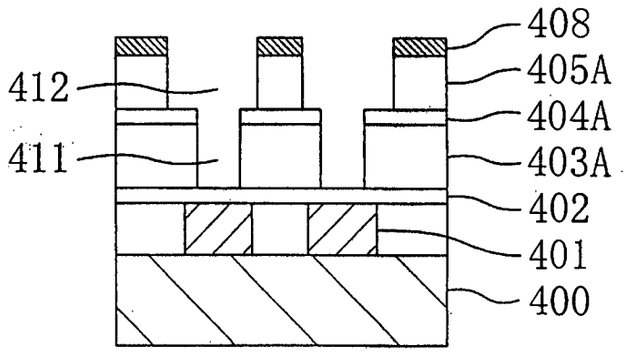


Fig. 19(c)



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O.G. FIG. 36
CLASS 438
SUBCLASS 700

Fig. 20(a)

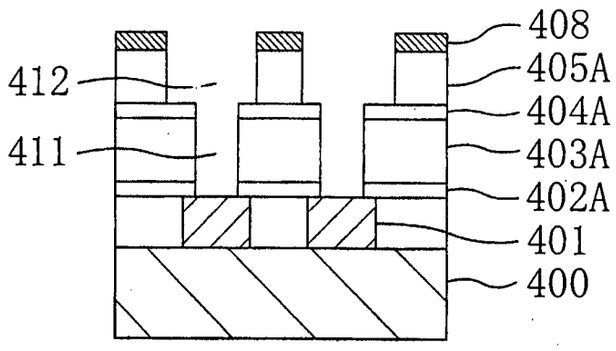


Fig. 20(b)

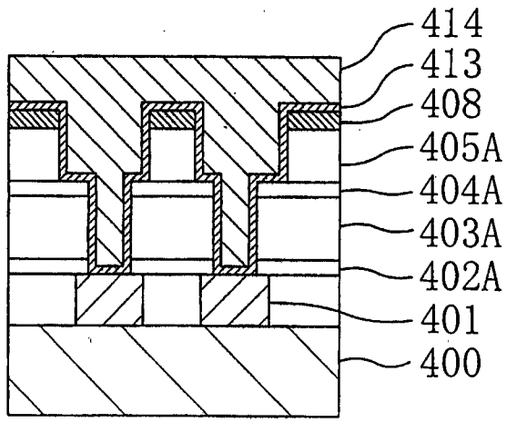
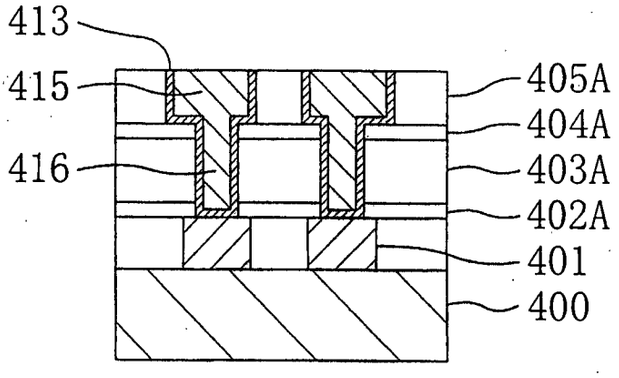


Fig. 20(c)



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O.G. FIG. 3b
CLASS 438
SUBCLASS 700

Fig. 21(a)

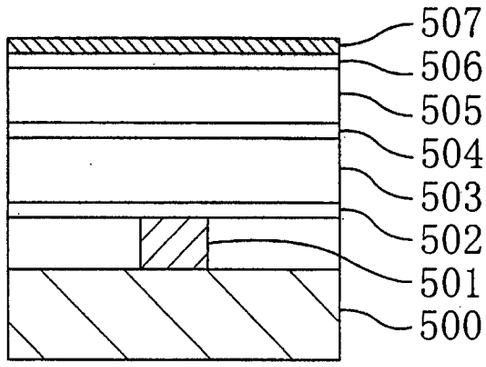


Fig. 21(b)

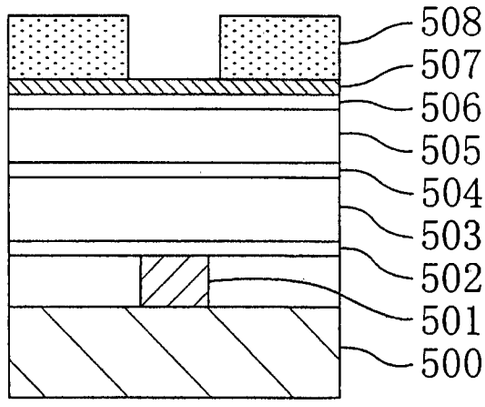
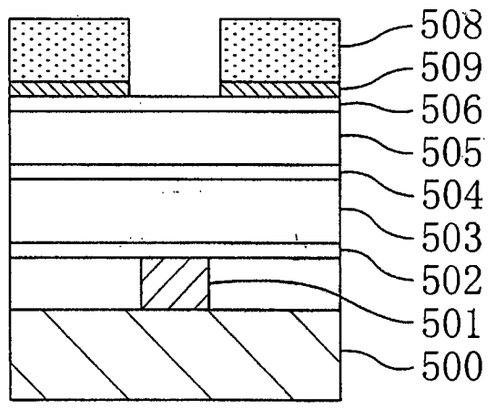


Fig. 21(c)



APPROVED BY DRAFTSMAN	O.G. FIG. 3b	
	CLASS	SUBCLASS
	438	700

Fig. 22(a)

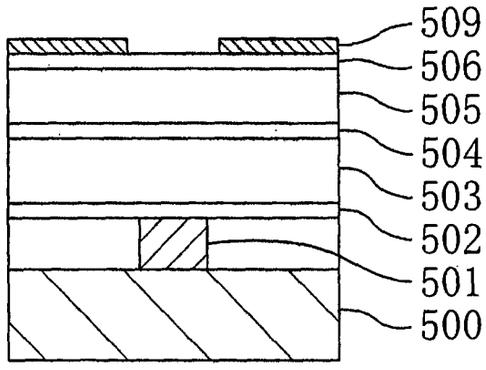


Fig. 22(b)

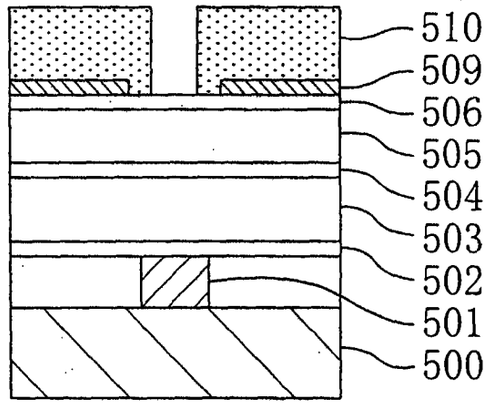
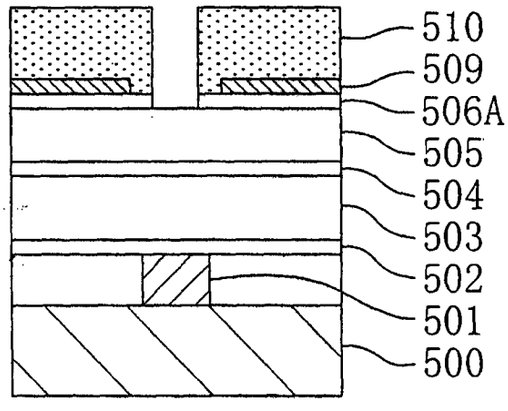


Fig. 22(c)



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CLASS 438
SUBCLASS 700

Fig. 23(a)

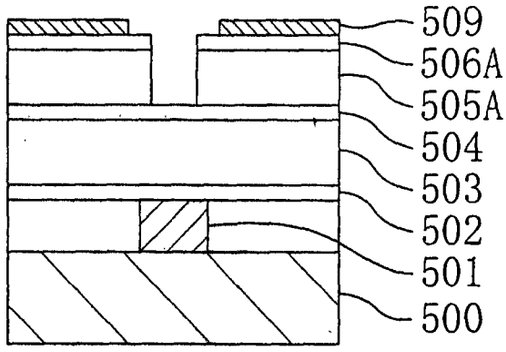


Fig. 23(b)

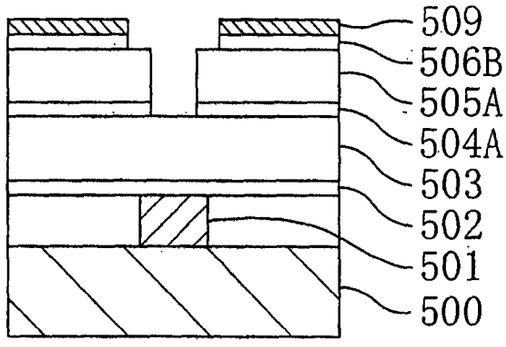


Fig. 23(c)

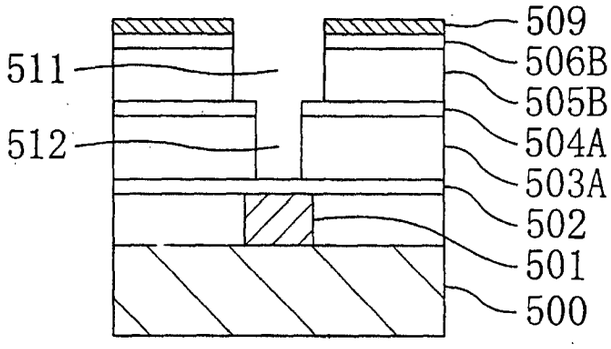
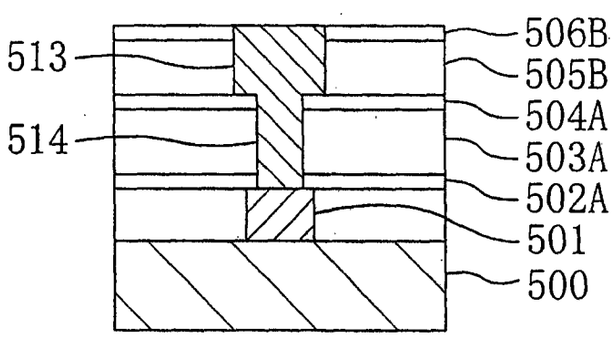


Fig. 23(d)



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O.G. FIG. 3b
CLASS 438
SUBCLASS 700

Fig. 24(a)

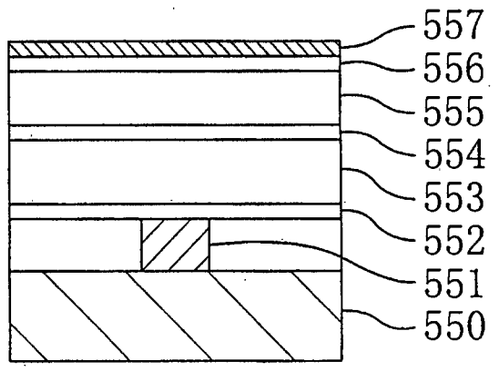


Fig. 24(b)

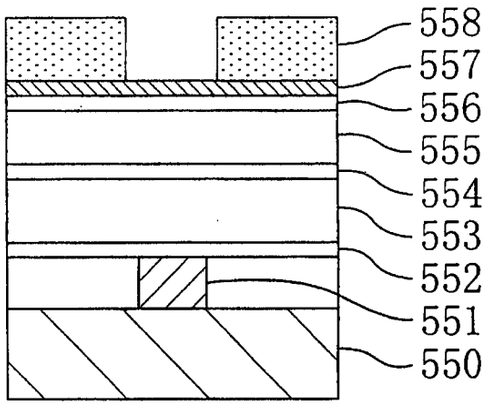
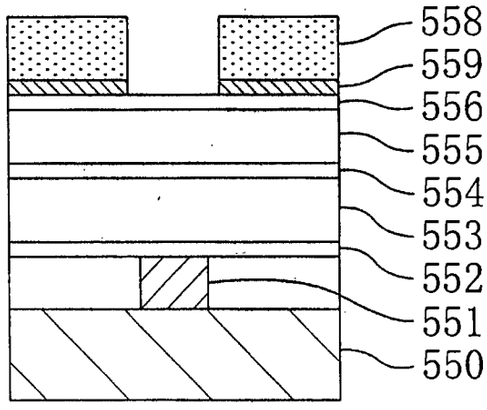


Fig. 24(c)



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O.G. FIG. 3b
CLASS 438
SUBCLASS 700

Fig. 25(a)

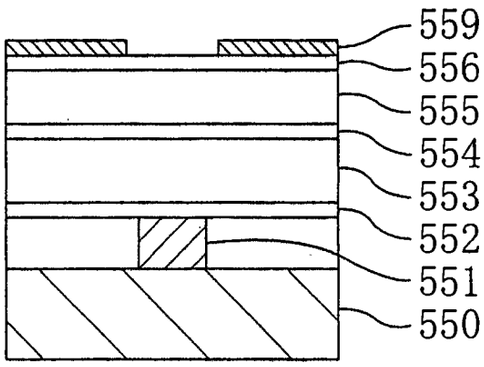


Fig. 25(b)

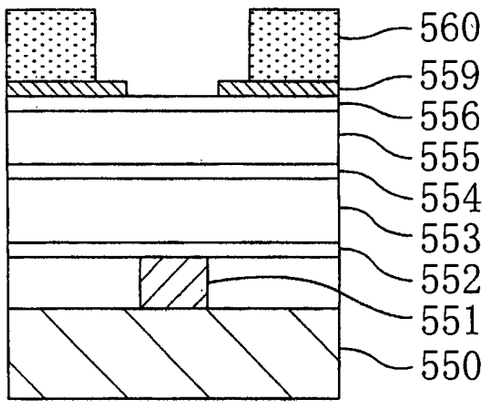
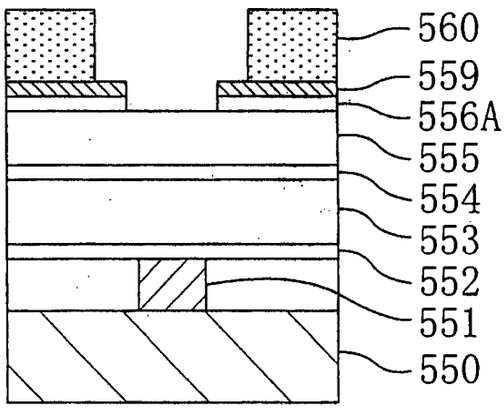


Fig. 25(c)



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O.G. FIG. 3b
CLASS 438
SUBCLASS 700

Fig. 26(a)

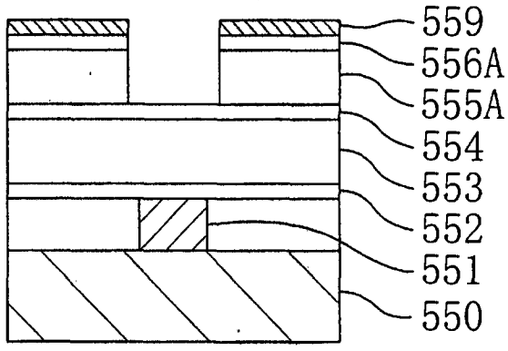


Fig. 26(b)

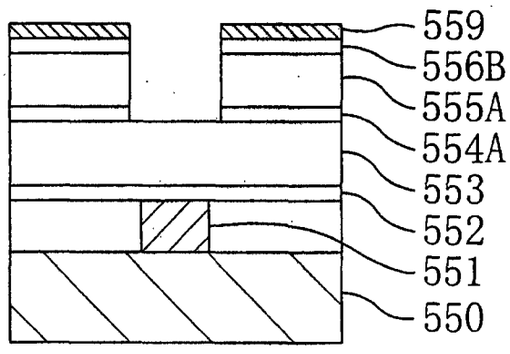


Fig. 26(c)

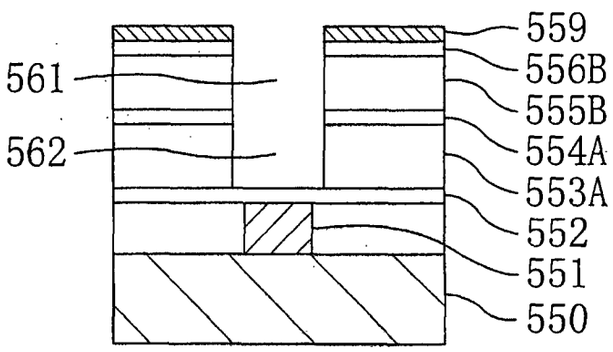
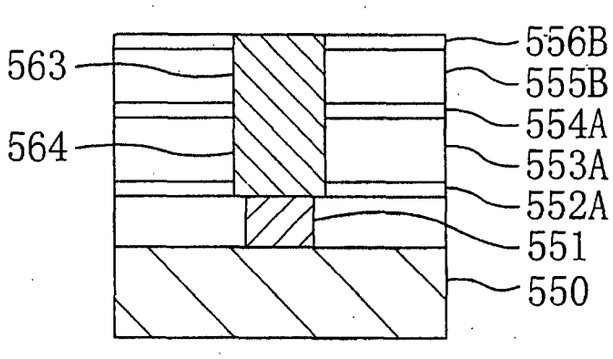


Fig. 26(d)



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O.G. FIG. 3b
CLASS 438
SUBCLASS 700

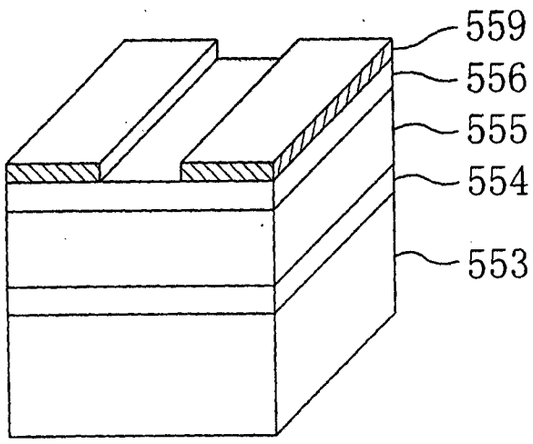

Fig. 27(a)

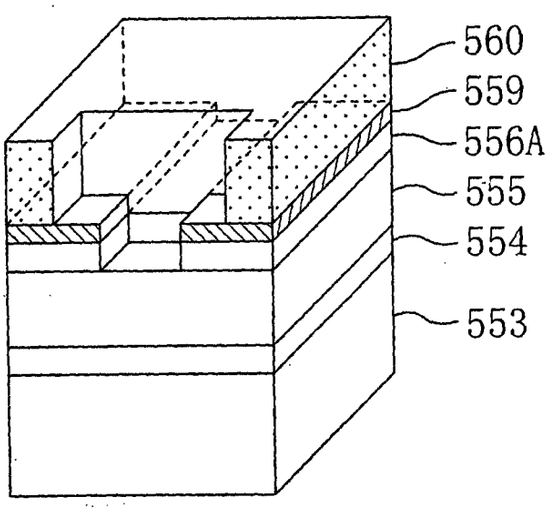

Fig. 27(b)

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O.G. FIG. 3b
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SUBCLASS 700

Fig. 28(a)

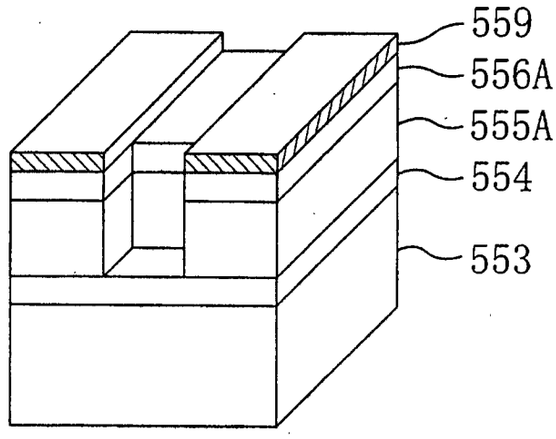
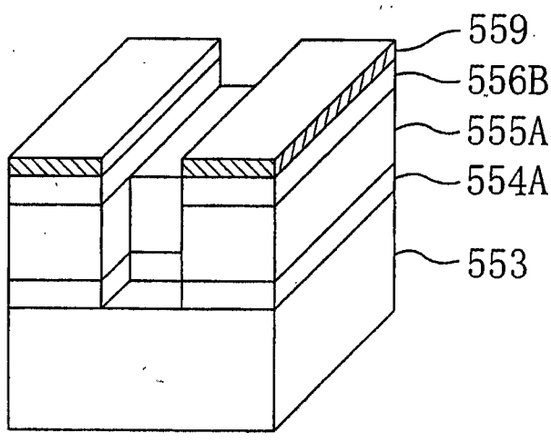


Fig. 28(b)



APPROVED BY DRAFTSMAN
O.G. FIG. 3b
CLASS 438
SUBCLASS 700

Fig. 29(a)

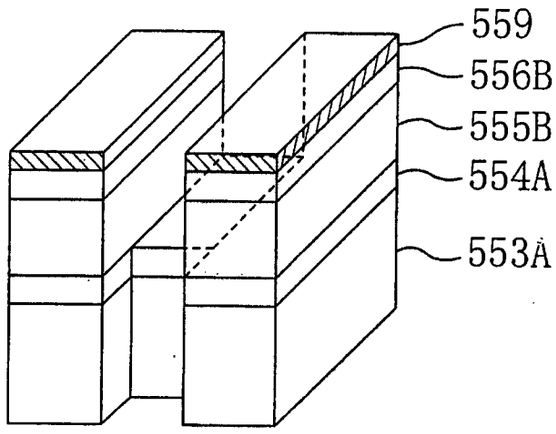
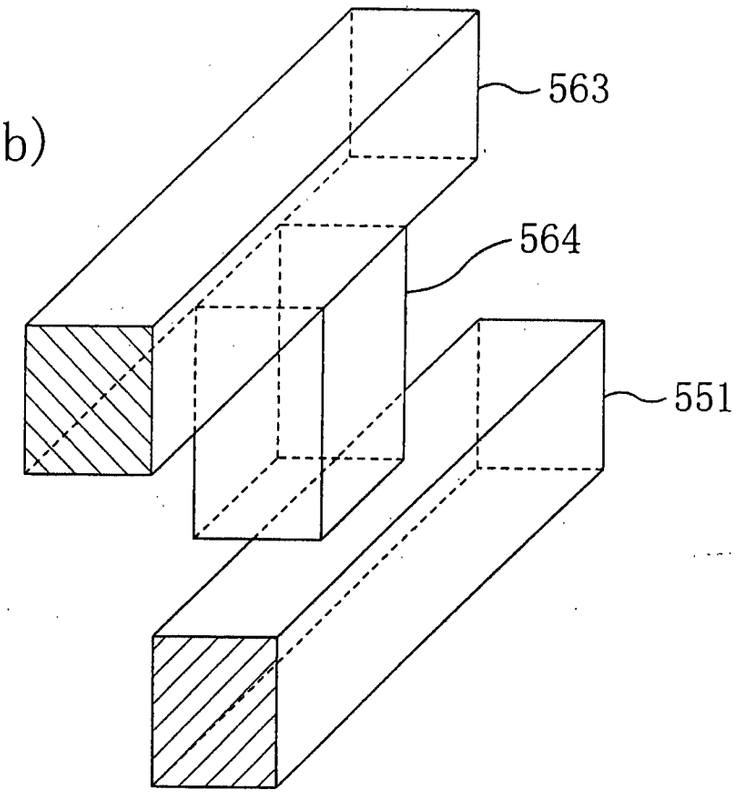


Fig. 29(b)



APPROVED BY DRAFTSMAN
O.G. FIG. 3b
CLASS 438 SUBCLASS 700

Fig. 30(a)

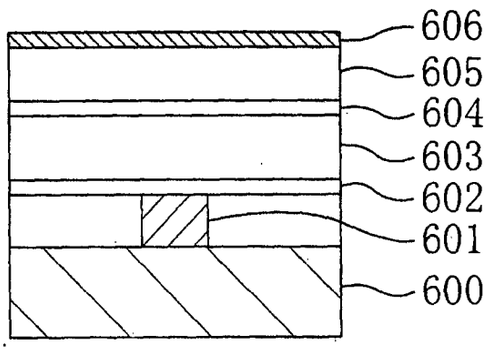


Fig. 30(b)

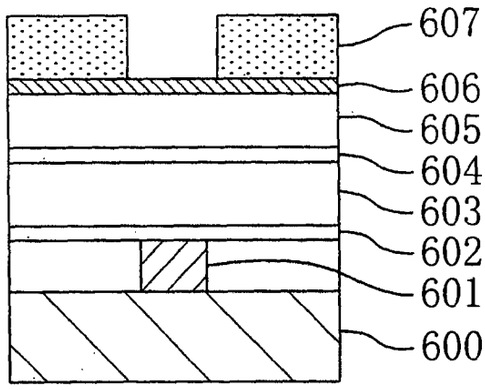
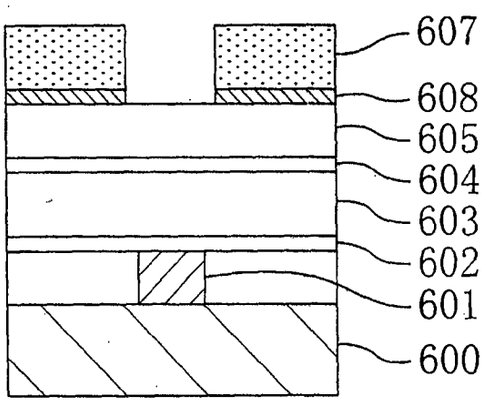


Fig. 30(c)



Doc Code: AP.PRE.REQ

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O.G. FIG. 3b
CLASS 438
SUBCLASS 700

Fig. 31(a)

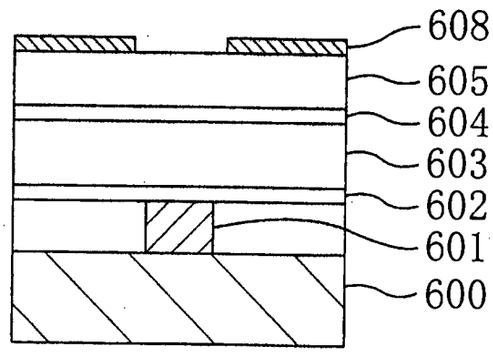

Fig. 31(b)

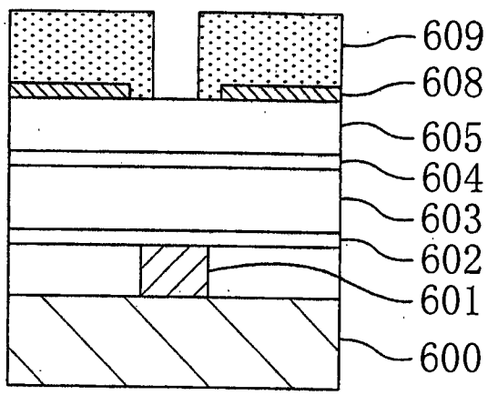

Fig. 31(c)

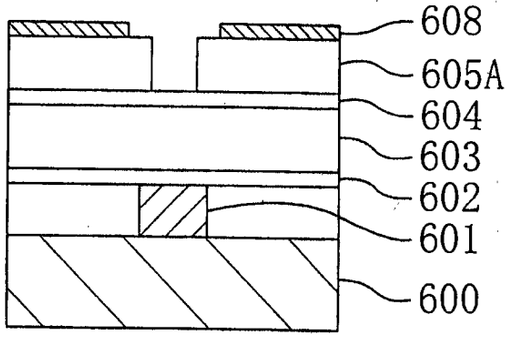

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FIG. 3b
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SUBCLASS 700

Fig. 32(a)

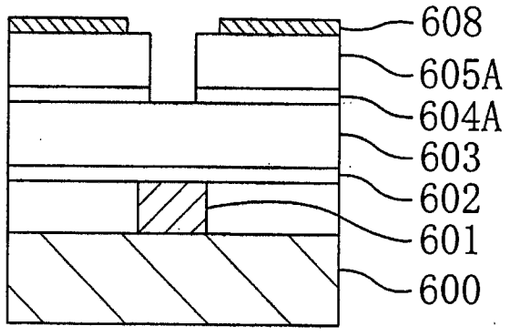


Fig. 32(b)

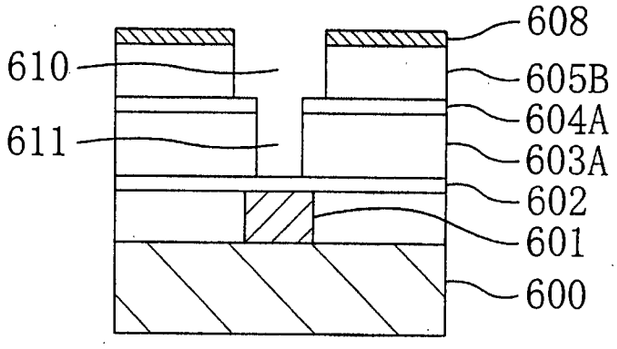
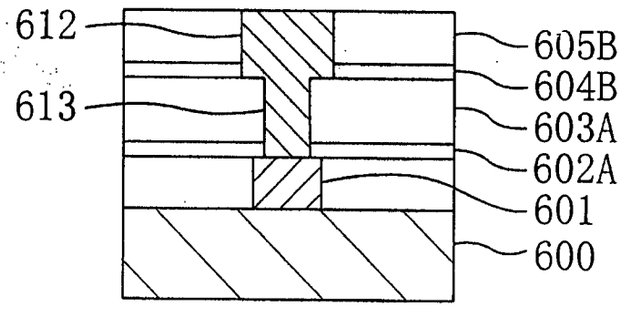


Fig. 32(c)



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D.G. FIG. 3b
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SUBCLASS 700

Fig. 33(a)

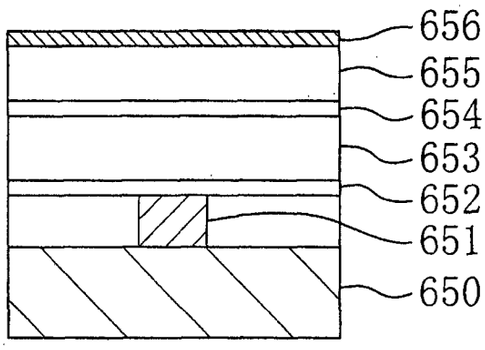

Fig. 33(b)

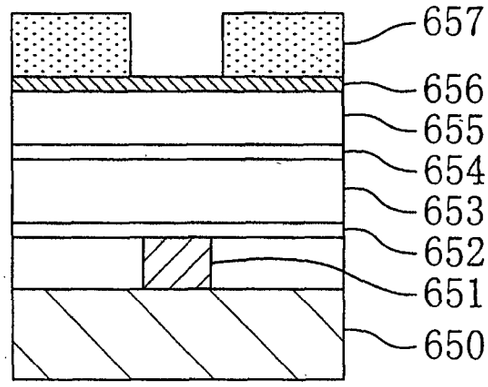

Fig. 33(c)

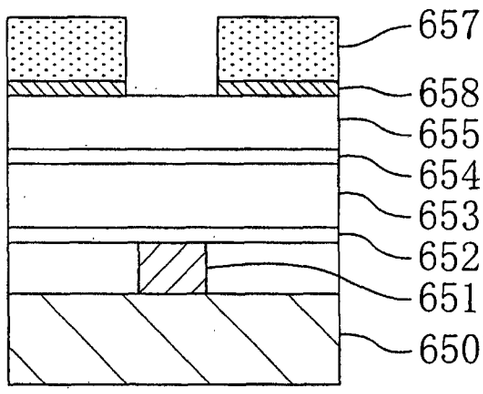

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Fig. 34(a)

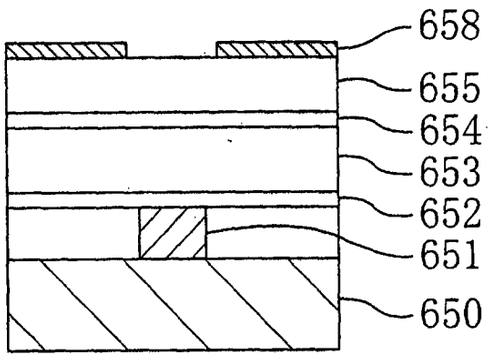

Fig. 34(b)

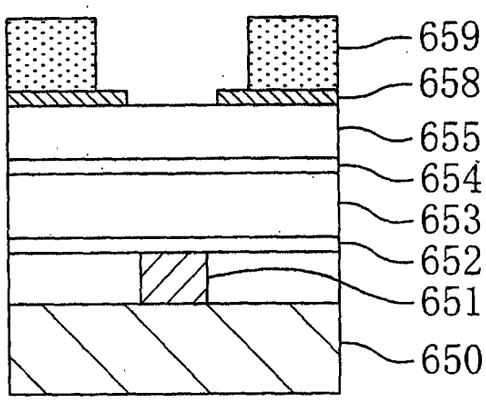

Fig. 34(c)

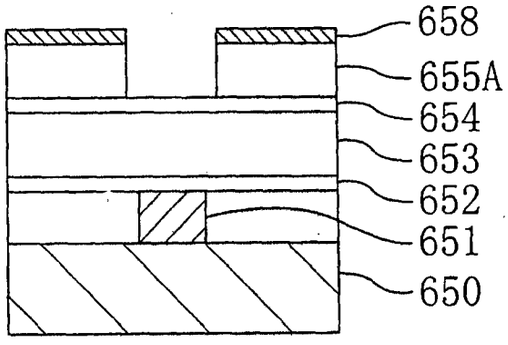

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FIG. 3b
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Fig. 35(a)

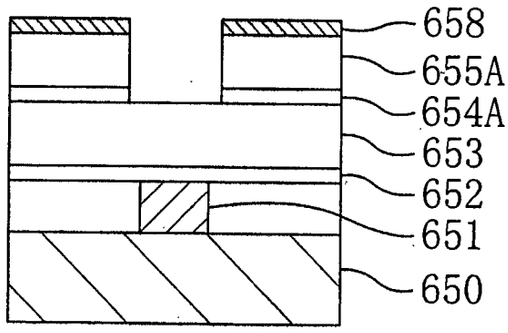


Fig. 35(b)

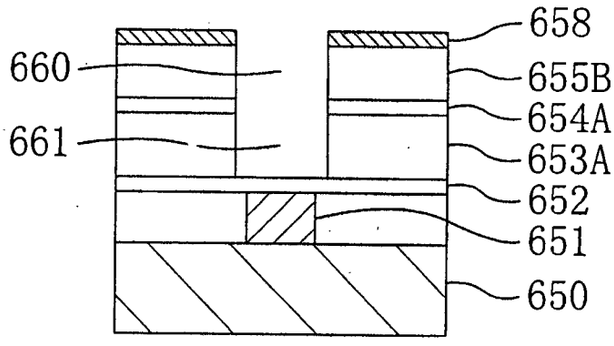
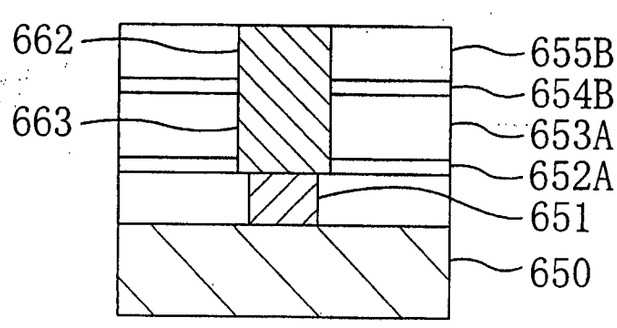
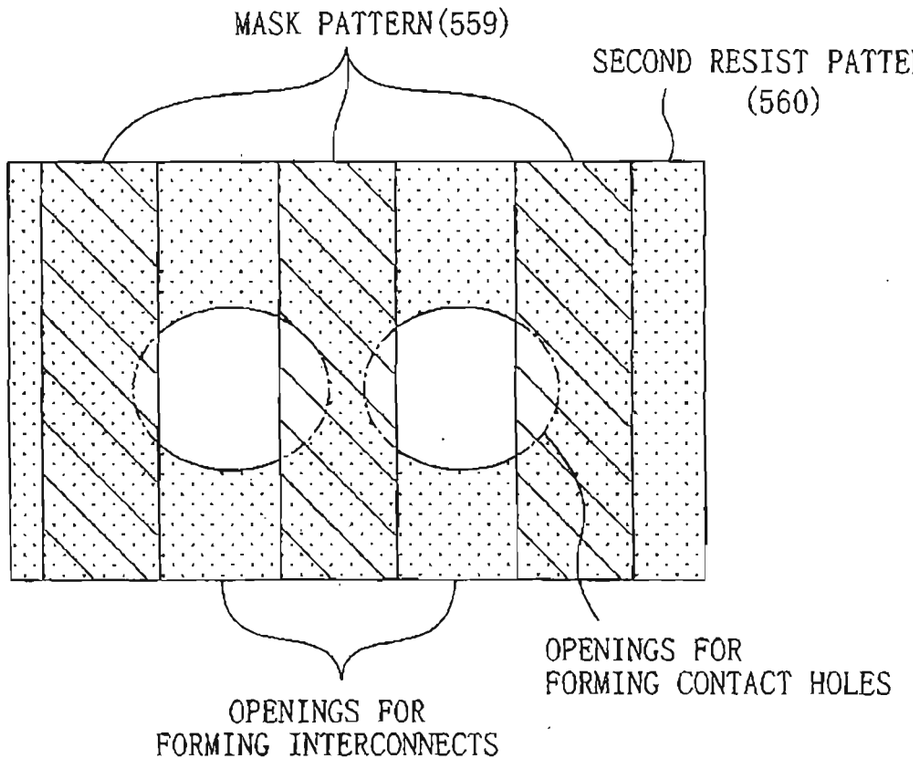


Fig. 35(c)



APPROVED BY DRAFTSMAN | U.S. FIG. 3b | CLASS 438 | SUBCLASS 700

Fig. 36



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O.G. FIG. 36
CLASS 438
SUBCLASS 700

Fig. 37(a)

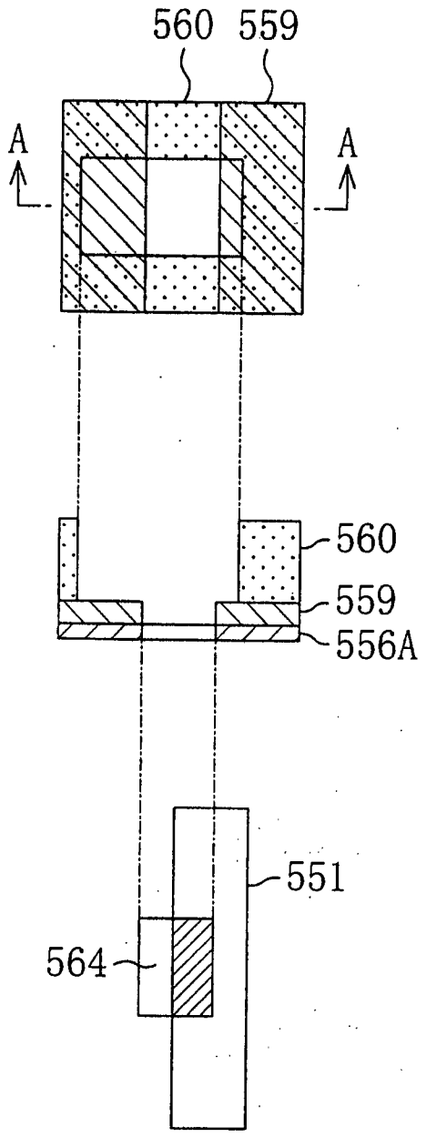
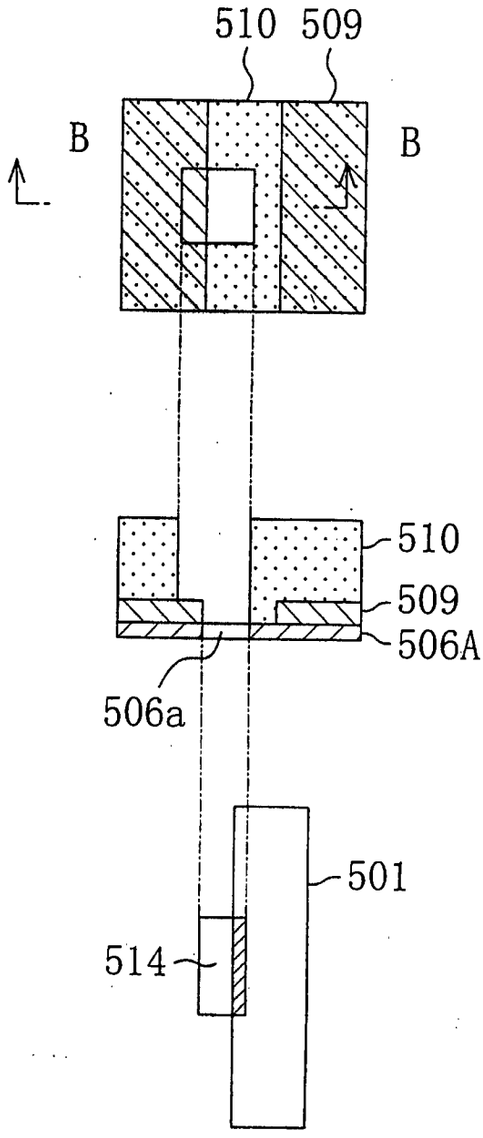


Fig. 37(b)



M99-K-033US1

DECLARATION AND POWER OF ATTORNEY FOR **PATENT** APPLICATION

ATTORNEY DOCKET NO.

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention entitled: METHOD FOR FORMING INTERCONNECTION STRUCTURE, the specification of which is attached hereto unless the following box is checked:

[ ] The specification was filed on _____
and was assigned Serial No. _____ (if known)
and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows:

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and checked at right:

Prior Foreign Application(s) (Number)	(Country)	(Month/Day/Year Filed)	Priority Claimed Yes	No
10-079371	Japan	03/26/1998	X	

All foreign applications, if any, for any Patent or Inventor's Certificate filed more than 12 months prior to the filing date of this application:

Country	Application No.	Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, §119(e) or §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status: patented, pending, abandoned

I hereby appoint the following attorneys to prosecute this application and/or any international application and to transact all business in the Patent and Trademark Office connected therewith:

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Charles M. Leedom, Jr. (Reg. No. 26,477)
David S. Safran (Reg. No. 27,997)
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Tim L. Brackett (Reg. No. 36,092)
Frank P. Presta (Reg. No. 19,828)
Robert M. Schulman (Reg. No. 31,196)
Lawrence D. Eisen (Reg. No. 41,009)
Marc S. Kaufman (Reg. No. 35,212)
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Joseph S. Presta (Reg. No. 35,329)
Thomas M. Blasey (Reg. No. 33,475)
Daniel S. Song (Reg. No. 43,143)

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SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
Telephone: (703) 790-9110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

The undersigned hereby authorize any U.S. attorney or agent named herein to accept and follow instructions from MAEDA PATENT OFFICE as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys or agents named herein will be so notified by the undersigned.

FULL NAME OF SOLE OR FIRST INVENTOR	INVENTOR'S SIGNATURE	DATE
Nobuo AOI	Nobuo Aoi	March 19, '99
RESIDENCE (City, State & Country)		CITIZENSHIP
Hyogo, Japan		Japan
POST OFFICE ADDRESS (Complete Address including City, State & Country)		
1-41-403, Taisha-cho, Nishinomiya-shi, Hyogo 662-0867, Japan		

Application Assignment Record

According to the application transmittal letter, an assignment recording ownership was filed with this application; however, a copy of this record was not located in the original file history record obtained from the United States Patent and Trademark Office. Upon your request, we will attempt to obtain the assignment documents from the Assignment Recordation Branch of of the United States Patent and Trademark Office or from a related application case (if applicable). Please note that additional charges will apply for this service.

This page is not part of the official USPTO record. It has been determined that content identified on this document is missing from the original file history record.

GP1763

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on June 23, 1999

Cecilia Campbell

Cecilia Campbell

Docket No.: 0819-226

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

OIPE JC67 JUN 25 1999 PATENT & TRADEMARK OFFICE

#2

In re PATENT application of)
Nobuo AOI)
Serial No. 09/274,114) Art Unit 1763
Filed: March 23, 1999)
For: METHOD FOR FORMING)
INTERCONNECTION STRUCTURE) June 23, 1999

RECEIVED JUL 1 1999 GROUP 1700

TRANSMITTAL OF CERTIFIED PRIORITY DOCUMENT

Honorable Assistant Commissioner for Patents
Washington, D. C. 20231

Sir:

At the time of filing the above-referenced application, a right of priority under 35 USC 119 was claimed in view of Application No. 10-079371, filed March 26, 1998 in Japan.

Submitted herewith is the certified copy of the priority document to perfect the claim for priority.

Acknowledgment is respectfully requested.

RECEIVED JUL 1 1999 GROUP 1700

Respectfully submitted,

Eric J. Robinson
Registration No. 38,285
SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

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OIPE JC67 JUN 25 1999 PATENT & TRADEMARK OFFICE

日本国特許庁
PATENT OFFICE
JAPANESE GOVERNMENT

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。
This is to certify that the annexed is a true copy of the following application as filed with this Office.

出願年月日
Date of Application: １９９８年　３月２６日

出願番号
Application Number: 平成１０年特許願第０７９３７１号

出願人
Applicant (s): 松下電器産業株式会社

１９９９年　４月　９日

特許庁長官
Commissioner,
Patent Office 伊佐山建志

出証番号　出証特平１１－３０２１６８１

【書類名】　特許願
【整理番号】　7411290311
【提出日】　平成10年 3月26日
【あて先】　特許庁長官　殿
【国際特許分類】　H01L 21/316
【発明の名称】　配線構造体の形成方法
【請求項の数】　9
【発明者】
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【弁理士】
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【識別番号】　100107445
【弁理士】
【氏名又は名称】　小根田　一郎
【手数料の表示】
【予納台帳番号】　014409
【納付金額】　21,000円

【提出物件の目録】

【物件名】　明細書　1

【物件名】　図面　1

【物件名】　要約書　1

【包括委任状番号】　9601026

【プルーフの要否】　要

【書類名】　　明細書

【発明の名称】　配線構造体の形成方法

【特許請求の範囲】

【請求項１】　下層の金属配線の上に第１の絶縁膜を形成する第１の工程と、

前記第１の絶縁膜の上に該第１の絶縁膜と組成が異なる第２の絶縁膜を形成する第２の工程と、

前記第２の絶縁膜の上に該第２の絶縁膜と組成が異なる第３の絶縁膜を形成する第３の工程と、

前記第３の絶縁膜の上に導電性膜を形成する第４の工程と、

前記導電性膜の上に、配線形成用開口部を有する第１のレジストパターンを形成する第５の工程と、

前記導電性膜に対して前記第１のレジストパターンをマスクとしてエッチングを行なって、前記導電性膜からなり配線形成用開口部を有するマスクパターンを形成する第６の工程と、

前記第３の絶縁膜の上に、コンタクトホール形成用開口部を有する第２のレジストパターンを形成する第７の工程と、

前記第３の絶縁膜、第１のレジストパターン及び第２のレジストパターンに対するエッチングレートが高い一方、前記第２の絶縁膜に対するエッチングレートが低いエッチング条件で、前記第３の絶縁膜に対してドライエッチングを行なうことにより、前記第３の絶縁膜を該第３の絶縁膜にコンタクトホール形成用開口部が形成されるようにパターン化すると共に、前記第１のレジストパターン及び第２のレジストパターンを全面的に又は下部を残して除去する第８の工程と、

前記第２の絶縁膜に対するエッチングレートが高い一方、前記第１の絶縁膜及び第３の絶縁膜に対するエッチングレートが低いエッチング条件で、前記第２の絶縁膜に対してパターン化された前記第３の絶縁膜をマスクとしてドライエッチングを行なうことにより、前記第２の絶縁膜を該第２の絶縁膜にコンタクトホール形成用開口部が形成されるようにパターン化する第９の工程と、

前記第１の絶縁膜及び第３の絶縁膜に対するエッチングレートが高い一方、前記マスクパターン及び第２の絶縁膜に対するエッチングレートが低いエッチング

条件で、前記第３の絶縁膜に対して前記マスクパターンをマスクとしてドライエッチングを行なうと共に前記第１の絶縁膜に対してパターン化された前記第２の絶縁膜をマスクとしてドライエッチングを行なうことにより、前記第３の絶縁膜に配線溝を形成すると共に前記第１の絶縁膜にコンタクトホールを形成する第１０の工程と、

前記配線溝及びコンタクトホールに金属膜を充填することにより、上層の金属配線及び前記下層の金属配線と前記上層の金属配線とを接続するコンタクトを形成する第１１の工程とを備えていることを特徴とする配線構造体の形成方法。

【請求項２】　前記第１０の工程と前記第１１の工程との間に、前記第３の絶縁膜における前記配線溝に露出している部分及び前記第１の絶縁膜における前記コンタクトホールに露出している部分に金属膜からなる密着層を形成する工程をさらに備えていることを特徴とする請求項１に記載の配線構造体の形成方法。

【請求項３】　前記第３の絶縁膜は有機成分を主成分とすることを特徴とする請求項１に記載の配線構造体の形成方法。

【請求項４】　前記第３の工程は、パーフルオロデカリンを含む反応性ガスを用いるＣＶＤ法により前記第３の絶縁膜を形成する工程を含むことを特徴とする請求項３に記載の配線構造体の形成方法。

【請求項５】　前記第１の絶縁膜は有機成分を主成分とすることを特徴とする請求項３に記載の配線構造体の形成方法。

【請求項６】　前記第１０の工程と前記第１１の工程との間に、前記第３の絶縁膜における前記配線溝に露出している部分及び前記第１の絶縁膜における前記コンタクトホールに露出している部分に、窒素を含有する反応性ガスを用いるプラズマ処理によって密着層を形成する工程をさらに備えていることを特徴とする請求項５に記載の配線構造体の形成方法。

【請求項７】　前記第１の工程は、パーフルオロデカリンを含む反応性ガスを用いるＣＶＤ法により前記第３の絶縁膜を形成する工程を含むことを特徴とする請求項３に記載の配線構造体の形成方法。

【請求項８】　下層の金属配線の上に第１の絶縁膜を形成する第１の工程と、前記第１の絶縁膜の上に該第１の絶縁膜と組成が異なる第２の絶縁膜を形成す

る第２の工程と、

前記第２の絶縁膜の上に該第２の絶縁膜と組成が異なる第３の絶縁膜を形成する第３の工程と、

前記第３の絶縁膜の上に導電性膜を形成する第４の工程と、

前記導電性膜の上に、配線形成用開口部を有する第１のレジストパターンを形成する第５の工程と、

前記導電性膜に対して前記第１のレジストパターンをマスクとしてエッチングを行なって、前記導電性膜からなり配線形成用開口部を有するマスクパターンを形成する第６の工程と、

前記第３の絶縁膜の上に、コンタクトホール形成用開口部を有する第２のレジストパターンを形成する第７の工程と、

前記第３の絶縁膜に対するエッチングレートが高い一方、前記第２の絶縁膜、第１のレジストパターン及び第２のレジストパターンに対するエッチングレートが低いエッチング条件で、前記第３の絶縁膜に対して前記第１のレジストパターン及び第２のレジストパターンをマスクとしてドライエッチングを行なうことにより、前記第３の絶縁膜を該第３の絶縁膜にコンタクトホール形成用開口部が形成されるようにパターン化する第８の工程と、

前記第２の絶縁膜に対するエッチングレートが高い一方、前記第１の絶縁膜、第３の絶縁膜、第１のレジストパターン及び第２のレジストパターンに対するエッチングレートが低いエッチング条件で、前記第２の絶縁膜に対して前記第１のレジストパターン及び第２のレジストパターンをマスクとしてドライエッチングを行なうことにより、前記第２の絶縁膜を該第２の絶縁膜にコンタクトホール形成用開口部が形成されるようにパターン化する第９の工程と、

前記第１のレジストパターン及び第２のレジストパターンを除去する第１０の工程と、

前記第１の絶縁膜及び第３の絶縁膜に対するエッチングレートが高い一方、前記マスクパターン及び第２の絶縁膜に対するエッチングレートが低いエッチング条件で、前記第３の絶縁膜に対して前記マスクパターンをマスクとしてドライエッチングを行なうと共に前記第１の絶縁膜に対してパターン化された前記第２の

絶縁膜をマスクとしてドライエッチングを行なうことにより、前記第３の絶縁膜に配線溝を形成すると共に前記第１の絶縁膜にコンタクトホールを形成する第１１の工程と、

前記配線溝及びコンタクトホールに金属膜を充填することにより、上層の金属配線及び前記下層の金属配線と前記上層の金属配線とを接続するコンタクトを形成する第１２の工程とを備えていることを特徴とする配線構造体の形成方法。

【請求項９】　前記第３の絶縁膜は、シロキサン骨格を有する低誘電率ＳＯＧ膜であることを特徴とする請求項８に記載の配線構造体の形成方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】

本発明は半導体集積回路装置における配線構造体の形成方法に関する。

【０００２】

【従来の技術】

半導体集積回路の高集積化の進展に伴い、金属配線同士の間の寄生容量である配線間容量の増加に起因する配線遅延時間の増大が半導体集積回路の高性能化の妨げとなっている。配線遅延時間は金属配線の抵抗と配線間容量との積に比例するいわゆるＲＣ遅延と言われるものである。

【０００３】

従って、配線遅延時間を低減するためには、金属配線の抵抗を小さくするか又は配線間容量を小さくすることが必要である。

【０００４】

そこで、配線抵抗を小さくために、配線材料としてアルミ系合金に代えて銅を用いる半導体集積回路装置がＩＢＭ社やモトローラ社から報告されている。銅材料はアルミ系合金材料の３分の２程度の比抵抗を有しているため、配線材料として銅材料を用いると、アルミ系合金材料を用いる場合に比べて、単純に計算すると配線遅延時間が３分の２に減少するので、１．５倍の高速化を実現することができる。

【０００５】

しかしながら、半導体集積回路の高集積化がさらに進展すると、銅からなる金属配線を用いる場合でも、配線遅延時間の増大によって、高速化が限界に達すると懸念されている。また、配線材料としての銅は、金又は銀についで比抵抗が小さいので、銅からなる金属配線に代えて金又は銀からなる金属配線を用いても、配線抵抗の低減は僅かなものである。

【０００６】

このため、半導体集積回路の高集積化のためには、配線抵抗の低減と共に配線間容量の低減が重要になっており、配線間容量の低減のためには、層間絶縁膜の比誘電率を小さくすることが必要である。従来、層間絶縁膜としては、シリコン酸化膜が用いられているが、シリコン酸化膜の比誘電率は４～４．５程度であって、より高集積化された半導体集積回路における層間絶縁膜には採用し難いという問題がある。

【０００７】

そこで、比誘電率がシリコン酸化膜よりも小さい層間絶縁膜として、フッ素添加シリコン酸化膜、低誘電率ＳＯＧ膜及び有機高分子膜が提案されている。

【０００８】

【発明が解決しようとする課題】

ところで、フッ素添加シリコン酸化膜の比誘電率は３．３～３．７であって、従来のシリコン酸化膜に比べて２割程度小さいが、フッ素添加シリコン酸化膜は、吸湿性が高いので大気中の水分を吸収しやすい。このため、フッ素添加シリコン酸化膜が水分を吸収して、比誘電率の高いＳｉＯＨが膜中に取り込まれるので、フッ素添加シリコン酸化膜の比誘電率が増加したり、熱処理工程においてＳｉＯＨが反応してH_2Oガスを放出したりするという問題、及びフッ素添加シリコン酸化膜中に遊離しているフッ素が熱処理工程において表面に偏析し、偏析したフッ素が密着層としてのＴｉＮ膜のＴｉ等と反応して剥がれやすいＴｉＦ膜を形成するという問題等があり、フッ素添加シリコン酸化膜は実用上の課題が多い。

【０００９】

低誘電率ＳＯＧ膜としては、ＨＳＱ（Hydrogen silsesquioxane：Ｓｉ原子と

、Ｏ原子と、Ｏ原子の数の３分の２の数のＨ原子とからなる構造体）膜が検討されているが、ＨＳＱ膜は、従来のシリコン酸化膜に比べて、水分放出量が多いので加工性が悪いという問題がある。ＨＳＱ膜は加工性が悪いためＨＳＱ膜に埋め込み配線を形成することは困難であるから、ＨＳＱ膜に金属配線を形成する場合には金属膜がパターン化されてなる金属配線を用いる必要がある。

【００１０】

また、ＨＳＱ膜は金属配線との密着性が低いので、金属配線との密着性を確保するために金属配線との間に密着層としてのＣＶＤ酸化膜を形成する必要がある。ところが、金属配線の上にＣＶＤ酸化膜を形成すると、金属配線間に比誘電率の大きいＣＶＤ酸化膜が存在するため、実質的な配線間容量はＨＳＱ膜とＣＶＤ酸化膜とから構成される直列容量になるので、ＨＳＱ膜を単体で用いた場合に比べて配線間容量が大きくなってしまうという問題がある。

【００１１】

有機高分子膜は、低誘電率ＳＯＧ膜と同様、金属配線との密着性が低いので、金属配線との間に密着層としてのＣＶＤ酸化膜を形成する必要がある。

【００１２】

また、有機高分子膜に対するエッチングレートが酸素プラズマによりレジストパターンをアッシングする際のアッシングレートとほぼ等しいため、レジストパターンをアッシングにより除去する際に有機高分子膜がダメージを受けるので、通常のレジストプロセスが使えないという問題がある。そこで、有機高分子膜の上にＣＶＤ酸化膜を形成した後、該ＣＶＤ酸化膜の上にレジスト膜を形成し、ＣＶＤ酸化膜をエッチングストッパー（保護膜）としてレジスト膜をエッチング加工する方法が提案されている。

【００１３】

ところが、有機高分子膜の上にＣＶＤ酸化膜を形成する際、有機高分子膜の表面が酸素を含む反応性ガスに曝されるため、有機高分子膜が酸素と反応して有機高分子膜中にカルボニル基やケトン基等の極性基が導入されるので、有機高分子膜の比誘電率が増加してしまうという問題がある。

【００１４】

また、有機高分子膜に銅の埋め込み配線を形成する場合、有機高分子膜は金属配線との密着性が低いため、有機高分子膜に形成された配線用凹部の周面に例えばＴｉＮ等からなる密着層を形成する必要があるが、ＴｉＮ膜は抵抗が高いため金属配線の有効断面積が減少してしまうので、銅からなる金属配線を用いて低抵抗化を図ったメリットが損なわれてしまうという問題がある。

【００１５】

前記に鑑み、本発明は、通常のレジストプロセスを採用して、比誘電率が低い層間絶縁膜を形成できるようにすることを目的とする。

【００１６】

【課題を解決するための手段】

本発明に係る第１の配線構造体の形成方法は、下層の金属配線の上に第１の絶縁膜を形成する第１の工程と、第１の絶縁膜の上に該第１の絶縁膜と組成が異なる第２の絶縁膜を形成する第２の工程と、第２の絶縁膜の上に該第２の絶縁膜と組成が異なる第３の絶縁膜を形成する第３の工程と、第３の絶縁膜の上に導電性膜を形成する第４の工程と、導電性膜の上に、配線形成用開口部を有する第１のレジストパターンを形成する第５の工程と、導電性膜に対して第１のレジストパターンをマスクとしてエッチングを行なって、導電性膜からなり配線形成用開口部を有するマスクパターンを形成する第６の工程と、第３の絶縁膜の上に、コンタクトホール形成用開口部を有する第２のレジストパターンを形成する第７の工程と、第３の絶縁膜、第１のレジストパターン及び第２のレジストパターンに対するエッチングレートが高い一方、第２の絶縁膜に対するエッチングレートが低いエッチング条件で、第３の絶縁膜に対してドライエッチングを行なうことにより、第３の絶縁膜を該第３の絶縁膜にコンタクトホール形成用開口部が形成されるようにパターン化すると共に、第１のレジストパターン及び第２のレジストパターンを全面的に又は下部を残して除去する第８の工程と、第２の絶縁膜に対するエッチングレートが高い一方、第１の絶縁膜及び第３の絶縁膜に対するエッチングレートが低いエッチング条件で、第２の絶縁膜に対してパターン化された第３の絶縁膜をマスクとしてドライエッチングを行なうことにより、第２の絶縁膜

を該第２の絶縁膜にコンタクトホール形成用開口部が形成されるようにパターン化する第９の工程と、第１の絶縁膜及び第３の絶縁膜に対するエッチングレートが高い一方、マスクパターン及び第２の絶縁膜に対するエッチングレートが低いエッチング条件で、第３の絶縁膜に対してマスクパターンをマスクとしてドライエッチングを行なうと共に第１の絶縁膜に対してパターン化された第２の絶縁膜をマスクとしてドライエッチングを行なうことにより、第３の絶縁膜に配線溝を形成すると共に第１の絶縁膜にコンタクトホールを形成する第１０の工程と、配線溝及びコンタクトホールに金属膜を充填することにより、上層の金属配線及び下層の金属配線と上層の金属配線とを接続するコンタクトを形成する第１１の工程とを備えている。

【００１７】

第１の配線構造体の形成方法によると、第８の工程において、第３の絶縁膜、第１のレジストパターン及び第２のレジストパターンに対するエッチングレートが高い一方、第２の絶縁膜に対するエッチングレートが低いエッチング条件で、第３の絶縁膜に対してドライエッチングを行なって、第３の絶縁膜をパターン化すると共に、第１のレジストパターン及び第２のレジストパターンを除去するため、第１のレジストパターン及び第２のレジストパターンを酸素プラズマを用いるアッシングにより除去する工程が不要になる。

【００１８】

また、第２の絶縁膜の組成と第３の絶縁膜の組成とが異なるため、第１０の工程において、第３の絶縁膜に対してマスクパターンをマスクとしてドライエッチングを行なって配線溝を形成する際に、第２の絶縁膜をエッチングストッパーとして用いることができる。

【００１９】

第１の配線構造体の形成方法は、第１０の工程と第１１の工程との間に、第３の絶縁膜における配線溝に露出している部分及び第１の絶縁膜におけるコンタクトホールに露出している部分に金属膜からなる密着層を形成する工程をさらに備えていることが好ましい。

【００２０】

第１の配線構造体の形成方法において、第３の絶縁膜は有機成分を主成分とすることが好ましい。

【００２１】

この場合、第３の工程は、パーフルオロデカリンを含む反応性ガスを用いるＣＶＤ法により第３の絶縁膜を形成する工程を含むことが好ましい。

【００２２】

また、この場合、第１の絶縁膜も有機成分を主成分とすることが好ましい。

【００２３】

第１の絶縁膜及び第２の絶縁膜が有機成分を主成分とする場合には、第１０の工程と第１１の工程との間に、第３の絶縁膜における配線溝に露出している部分及び第１の絶縁膜におけるコンタクトホールに露出している部分に、窒素を含有する反応性ガスを用いるプラズマ処理によって密着層を形成する工程をさらに備えていることが好ましい。

【００２４】

第１の絶縁膜が有機成分を主成分とする場合には、第１の工程は、パーフルオロデカリンを含む反応性ガスを用いるＣＶＤ法により第３の絶縁膜を形成する工程を含むことが好ましい。

【００２５】

本発明に係る第２の配線構造体の形成方法は、下層の金属配線の上に第１の絶縁膜を形成する第１の工程と、第１の絶縁膜の上に該第１の絶縁膜と組成が異なる第２の絶縁膜を形成する第２の工程と、第２の絶縁膜の上に該第２の絶縁膜と組成が異なる第３の絶縁膜を形成する第３の工程と、第３の絶縁膜の上に導電性膜を形成する第４の工程と、導電性膜の上に、配線形成用開口部を有する第１のレジストパターンを形成する第５の工程と、導電性膜に対して第１のレジストパターンをマスクとしてエッチングを行なって、導電性膜からなり配線形成用開口部を有するマスクパターンを形成する第６の工程と、第３の絶縁膜の上に、コンタクトホール形成用開口部を有する第２のレジストパターンを形成する第７の工程と、第３の絶縁膜に対するエッチングレートが高い一方、第２の絶縁膜、第１

のレジストパターン及び第２のレジストパターンに対するエッチングレートが低いエッチング条件で、第３の絶縁膜に対して第１のレジストパターン及び第２のレジストパターンをマスクとしてドライエッチングを行なうことにより、第３の絶縁膜を該第３の絶縁膜にコンタクトホール形成用開口部が形成されるようにパターン化する第８の工程と、第２の絶縁膜に対するエッチングレートが高い一方、第１の絶縁膜、第３の絶縁膜、第１のレジストパターン及び第２のレジストパターンに対するエッチングレートが低いエッチング条件で、第２の絶縁膜に対して第１のレジストパターン及び第２のレジストパターンをマスクとしてドライエッチングを行なうことにより、第２の絶縁膜を該第２の絶縁膜にコンタクトホール形成用開口部が形成されるようにパターン化する第９の工程と、第１のレジストパターン及び第２のレジストパターンを除去する第１０の工程と、第１の絶縁膜及び第３の絶縁膜に対するエッチングレートが高い一方、マスクパターン及び第２の絶縁膜に対するエッチングレートが低いエッチング条件で、第３の絶縁膜に対してマスクパターンをマスクとしてドライエッチングを行なうと共に第１の絶縁膜に対してパターン化された第２の絶縁膜をマスクとしてドライエッチングを行なうことにより、第３の絶縁膜に配線溝を形成すると共に第１の絶縁膜にコンタクトホールを形成する第１１の工程と、配線溝及びコンタクトホールに金属膜を充填することにより、上層の金属配線及び下層の金属配線と上層の金属配線とを接続するコンタクトを形成する第１２の工程とを備えている。

【００２６】

第２の配線構造体の形成方法によると、第１０の工程において、第１のレジストパターン及び第２のレジストパターンを除去する際に、第１の絶縁膜及び第３の絶縁膜における第２の絶縁膜のコンタクトホール形成用開口部に露出している部分にダメージ層が形成されても、第１１の工程において、第１の絶縁膜及び第３の絶縁膜に対するエッチングレートが高い一方、マスクパターン及び第２の絶縁膜に対するエッチングレートが低いエッチング条件で、第３の絶縁膜に対してマスクパターンをマスクとしてドライエッチングを行なうと共に第１の絶縁膜に対してパターン化された第２の絶縁膜をマスクとしてドライエッチングを行なって、第３の絶縁膜に配線溝を形成すると共に第１の絶縁膜にコンタクトホールを

形成するため、第１の絶縁膜及び第３の絶縁膜に形成されているダメージ層は確実に除去される。

【００２７】

第２の配線構造体の形成方法において、第３の絶縁膜は、シロキサン骨格を有する低誘電率ＳＯＧ膜であることが好ましい。

【００２８】

【発明の実施の形態】

（第１の実施形態）

以下、本発明の第１の実施形態に係る配線構造体の形成方法について、図１（ａ）～（ｃ）、図２（ａ）～（ｃ）及び図３（ａ）～（ｃ）を参照しながら説明する。

【００２９】

まず、図１（ａ）に示すように、半導体基板１００上に形成された第１の金属配線１０１の上に、後に行なわれるエッチング工程において第１の金属配線１０１を保護する例えば５０ｎｍの膜厚を有するシリコン窒化膜１０２を形成した後、該シリコン窒化膜１０２の上に、例えば１μｍの膜厚を有すると共に有機成分を主成分とする第１の有機膜１０３を堆積する。次に、第１の有機膜１０３の上に、例えば５０ｎｍの膜厚を有すると共にシリコン酸化物中に有機成分を含有する有機含有シリコン酸化膜１０４を堆積した後、該有機含有シリコン酸化膜１０４の上に、例えば４００ｎｍの膜厚を有すると共に有機成分を主成分とする第２の有機膜１０５を堆積し、その後、該第２の有機膜１０５の上に例えば５０ｎｍの膜厚を有する窒化チタン膜１０６を堆積する。

【００３０】

第１及び第２の有機膜１０３、１０５の堆積方法については、特に限定されないが、例えばパーフルオロデカシンを主原料とする反応性ガスを用いるプラズマＣＶＤ法が挙げられる。また、第１及び第２の有機膜１０３、１０５としては、プラズマＣＶＤ法、塗布法又は熱ＣＶＤ法により形成された、炭化水素膜又はフッ素を含有する炭化水素膜を用いることができる。

【００３１】

また、第１の有機膜１０３の堆積方法としては、例えばパーフルオロデカシンと、ヘキサメチルジシロキサン、アリルアルコキシシラン又はアルキルアルコキシシラン等の有機シランとを主原料とする反応性ガスを用いるプラズマＣＶＤ法でもよい。このようにすると、有機無機ハイブリッド膜が得られる。

【００３２】

また、有機含有シリコン酸化膜１０４の堆積方法については、特に限定されないが、例えばフェニルトリメトキシランを主原料とする反応性ガスを用いるＣＶＤ法が挙げられる。このようにすると、シリコン酸化物中にシリコン原子と結合したフェニル基が取り込まれた構造を有する有機含有シリコン酸化膜１０４が得られる。

【００３３】

次に、図１（ｂ）に示すように、窒化チタン膜１０６の上に、リソグラフィ工程により配線溝形成用開口部を有する第１のレジストパターン１０７を形成した後、該第１のレジストパターン１０７をマスクとして窒化チタン膜１０６に対してドライエッチングを行なって、図１（ｃ）に示すように、窒化チタン膜１０６からなるマスクパターン１０８を形成する。

【００３４】

次に、第１のレジストパターン１０７を除去することなく、第２の有機膜１０５の上に、リソグラフィ工程によりコンタクトホール形成用開口部を有する第２のレジストパターン１０９を形成した後、第２の有機膜１０５に対してドライエッチングを行なって、図２（ａ）に示すように、コンタクトホール形成用開口部を有するパターン化された第２の有機膜１０５Ａを形成する。この場合、第２の有機膜１０５と、第１のレジストパターン１０７及び第２のレジストパターン１０９とは共に有機成分を主成分としているため、第２の有機膜１０５に対するエッチングレートと、第１及び第２のレジストパターン１０７、１０９に対するエッチングレートとはほぼ等しいので、第２の有機膜１０５に対するドライエッチング工程により、第１のレジストパターン１０７及び第２のレジストパターン１０９は除去される。

【００３５】

尚、第２の有機膜１０５に対するドライエッチング工程において、第２のレジストパターン１０９が残存しても差し支えない。その理由は、残存する第２のレジストパターン１０９は、後に行なわれるパターン化された第２の有機膜１０５Ａに配線溝１１１を形成する工程（図２（ｃ）を参照）において除去されるからである。

【００３６】

次に、パターン化された第２の有機膜１０５Ａをマスクとして有機含有シリコン酸化膜１０４に対してドライエッチングを行なって、図２（ｂ）に示すように、コンタクトホール形成用開口部を有するパターン化された有機含有シリコン酸化膜１０４Ａを形成する。このドライエッチング工程は、有機含有シリコン酸化膜１０４に対するエッチングレートがパターン化された第２の有機膜１０５Ａに対するエッチングレートよりも大きくなるようなエッチング条件を選択することにより、パターン化された第２の有機膜１０５Ａがエッチングされる事態を防止する。

【００３７】

次に、マスクパターン１０８をマスクとしてパターン化された第２の有機膜１０５Ａに対し、またパターン化された有機含有シリコン酸化膜１０４Ａをマスクとして第１の有機膜１０３に対してそれぞれドライエッチングを行なって、図２（ｃ）に示すように、パターン化された第２の有機膜１０５Ａに配線溝１１１を形成すると共に、コンタクトホール１１０を有するパターン化された第１の有機膜１０３Ａを形成する。

【００３８】

次に、パターン化された有機含有シリコン酸化膜１０４Ａをマスクとしてシリコン窒化膜１０２に対してドライエッチングを行なって、図３（ａ）に示すように、パターン化されたシリコン窒化膜１０２Ａを形成すると共に、第１の金属配線１０１をコンタクトホール１１０に露出させる。

【００３９】

次に、図３（ｂ）に示すように、コンタクトホール１１０及び配線溝１１１の

壁面に例えば５０ｎｍの膜厚を有する窒化チタンからなる密着層１１２を堆積した後、コンタクトホール１１０及び配線溝１１１が埋まるように全面に亘って金属膜１１３を堆積する。金属膜１１３の組成は特に限定されず、銅、アルミニウム、金、銀、ニッケル、コバルト、タングステン又はこれらの合金等を用いることができると共に、金属膜１１３の堆積方法も特に限定されず、メッキ法、ＣＶＤ法又はスパッタ法等を用いることができる。

【００４０】

次に、図３（ｃ）に示すように、パターン化された第２の有機膜１０５Ａの上に堆積されている、密着層１１２、金属膜１１３及びマスクパターン１０８を例えばＣＭＰ法により除去して、金属膜１１３からなる第２の金属配線１１４、及び第１の金属配線１０１と第２の金属配線１１４とを接続する金属膜１１３からなるコンタクト１１５を形成する。

【００４１】

尚、第２の金属配線１１４の上に、前述した工程と同様の工程を行なうことにより、多層配線構造を形成することができる。

【００４２】

第１の実施形態によると、有機含有シリコン酸化膜１０４は、フェニルトリメトキシシランを主原料とする反応性ガスを用いるＣＶＤ法により形成された膜であるため、シリコン酸化物中にシリコン原子と結合したフェニル基（有機基）が取り込まれた構造を有している。従って、従来のＣＶＤ酸化膜と同程度に良好な加工性及びＨＳＱ膜と同程度に低い比誘電率を有していると共に、有機膜、酸化膜及び金属膜に対する高い密着性を有している。

【００４３】

また、窒化チタン膜１０６からなるマスクパターン１０８を形成した後、第１のレジストパターン１０７を除去することなく第２のレジストパターン１０９を形成すると共に、第２の有機膜１０５に対するドライエッチング工程により、第１のレジストパターン１０７及び第２のレジストパターン１０９を除去するため、第１のレジストパターン１０７及び第２のレジストパターン１０９を酸素プラズマを用いるアッシングにより除去する工程が不要になるので、レジストパター

ンをアッシングにより除去する際に第２の有機膜１０５がダメージを受ける事態を回避することができる。従って、層間絶縁膜として比誘電率が低い第２の有機膜１０５を用いるにも拘わらず、通常のレジストプロセスを採用することが可能になる。

【００４４】

また、マスクパターン１０８をマスクとしパターン化された有機含有シリコン酸化膜１０４Ａをエッチングストッパーとして、パターン化された第２の有機膜１０５Ａに対してドライエッチングを行なって配線溝１１１を形成するため、配線溝１１１の深さは第２の有機膜１０５の膜厚と一致するので、配線溝１１１の深さを自己整合的に規定することができる。

【００４５】

以下、第２のレジストパターン１０９が第１のレジストパターン１０７に対して位置ずれを起こした場合の問題点及びその場合の解決策について説明する。

【００４６】

まず、第２のレジストパターン１０９が位置ずれを起こした場合の問題点について、図４（ａ）～（ｃ）、図５（ａ）～（ｃ）及び図６（ａ）～（ｃ）を参照しながら説明する。

【００４７】

第１の実施形態と同様、図４（ａ）に示すように、半導体基板１００上に形成された第１の金属配線１０１の上に例えば５０ｎｍの膜厚を有するシリコン窒化膜１０２を形成した後、該シリコン窒化膜１０２の上に、例えば１μｍの膜厚を有すると共に有機成分を主成分とする第１の有機膜１０３を堆積する。

【００４８】

次に、第１の有機膜１０３の上に、例えば５０ｎｍの膜厚を有すると共にシリコン酸化物中に有機成分を含有する有機含有シリコン酸化膜１０４を堆積した後、該有機含有シリコン酸化膜１０４の上に、例えば４００ｎｍの膜厚を有すると共に有機成分を主成分とする第２の有機膜１０５を堆積し、その後、第２の有機膜１０５の上に例えば５０ｎｍの膜厚を有する窒化チタン膜１０６を堆積する。

【００４９】

次に、図４（ｂ）に示すように、窒化チタン膜１０６の上に、配線溝形成用開口部を有する第１のレジストパターン１０７を形成した後、該第１のレジストパターン１０７をマスクとして窒化チタン膜１０６に対してドライエッチングを行なって、図４（ｃ）に示すように、窒化チタン膜１０６からなるマスクパターン１０８を形成する。

【００５０】

次に、図５（ａ）に示すように、第１のレジストパターン１０７を除去することなく、第２の有機膜１０５の上に、コンタクトホール形成用開口部を有する第２のレジストパターン１０９を形成する。この場合、図５（ａ）と図１（ｃ）との対比から分かるように、第２のレジストパターン１０９は第１のレジストパターン１０７に対して位置ずれを起こしている。

【００５１】

次に、第２の有機膜１０５に対してドライエッチングを行なって、図５（ｂ）に示すように、コンタクトホール形成用開口部を有するパターン化された第２の有機膜１０５Ａを形成する。第１の実施形態と同様、第２の有機膜１０５と、第１のレジストパターン１０７及び第２のレジストパターン１０９とは共に有機成分を主成分としているため、第２の有機膜１０５に対するドライエッチング工程により、第１のレジストパターン１０７及び第２のレジストパターン１０９は除去される。この場合、第２のレジストパターン１０９が第１のレジストパターン１０７に対して位置ずれを起こしているため、第２の有機膜１０５Ａに形成されるコンタクトホール形成用開口部の径は小さい。

【００５２】

次に、パターン化された第２の有機膜１０５Ａをマスクとして有機含有シリコン酸化膜１０４に対してドライエッチングを行なって、図５（ｃ）に示すように、コンタクトホール形成用開口部を有するパターン化された有機含有シリコン酸化膜１０４Ａを形成する。

【００５３】

次に、マスクパターン１０８をマスクとしてパターン化された第２の有機膜１

０５Ａに対し、またパターン化された有機含有シリコン酸化膜１０４Ａをマスクとして第１有機膜１０３に対してそれぞれドライエッチングを行なって、図６（ａ）に示すように、パターン化された第２の有機膜１０５Ａに配線溝１１１を形成すると共に、コンタクトホール１１０を有するパターン化された第１の有機膜１０３Ａを形成する。その後、パターン化された有機含有シリコン酸化膜１０４Ａをマスクとしてシリコン窒化膜１０２に対してドライエッチングを行なって、図６（ｂ）に示すように、パターン化されたシリコン窒化膜１０２Ａを形成すると共に、第１の金属配線１０１をコンタクトホール１１０に露出させる。

【００５４】

次に、コンタクトホール１１０及び配線溝１１１の壁面に例えば５０ｎｍの膜厚を有する窒化チタン層からなる密着層１１２を堆積した後、全面に亘って金属膜を堆積し、その後、パターン化された第２の有機膜１０５Ａの上に堆積されている、密着層１１２、金属膜及びマスクパターン１０８を例えばＣＭＰ法により除去する。このようにすると、図６（ｃ）に示すように、金属膜からなる第２の金属配線１１４は形成されるが、コンタクトホール１１０の径が小さいため該コンタクトホール１１０には金属膜が完全には充填されないので、第１の金属配線１０１と第２の金属配線１１２とは接続されず、不良が発生する。

【００５５】

以下、第２のレジストパターン１０９が位置ずれを起こした場合の解決策について、図７（ａ）～（ｃ）及び図８（ａ）～（ｃ）を参照しながら説明する。

【００５６】

まず、図４（ａ）～（ｃ）及び図５（ａ）に基づいて説明した前述の工程と同様の工程によって、コンタクトホール形成用開口部を有する第２のレジストパターン１０９を形成するが、この場合にも、第２のレジストパターン１０９は第１のレジストパターン１０７に対して位置ずれを起こしている（図５（ａ）を参照）。

【００５７】

そこで、図７（ａ）に示すように、第２のレジストパターン１０９をマスクとして第１のレジストパターン１０７及びマスクパターン１０８に対してドライエ

ッチングを行なって、第１のレジストパターン１０７における第２のレジストパターン１０９と重なっていない領域を除去すると共に、マスクパターン１０８の開口部を配線溝形成用開口部及びコンタクトホール形成用開口部を含む大きさに拡大する。これによって、第２のレジストパターン１０９のコンタクトホール形成用開口部は、第１のレジストパターン１０７及びマスクパターン１０８に転写される。

【００５８】

次に、第２の有機膜１０５に対してドライエッチングを行なって、図７（ｂ）に示すように、コンタクトホール形成用開口部を有するパターン化された第２の有機膜１０５Ａを形成する。この場合にも、第２の有機膜１０５と、第１のレジストパターン１０７及び第２のレジストパターン１０９とは共に有機成分を主成分としているため、第２の有機膜１０５に対するドライエッチング工程により、第１のレジストパターン１０７及び第２のレジストパターン１０９は除去される。

【００５９】

次に、パターン化された有機膜１０５Ａをマスクとして有機含有シリコン酸化膜１０４に対してドライエッチングを行なって、図７（ｃ）に示すように、コンタクトホール形成用開口部を有するパターン化された有機含有シリコン酸化膜１０４Ａを形成する。

【００６０】

前述のように、第２のレジストパターン１０９が第１のレジストパターン１０７に対して位置ずれを起こしているが、第２のレジストパターン１０９のコンタクトホール形成用開口部を第１のレジストパターン１０７及びマスクパターン１０８に転写しているので、パターン化された第２の有機膜１０５Ａ及びパターン化された有機含有シリコン酸化膜１０４Ａに形成されるコンタクトホール形成用開口部の径は所定の大きさを有している。

【００６１】

次に、マスクパターン１０８及びパターン化された有機含有シリコン酸化膜１０４Ａをマスクとしてパターン化された第２の有機膜１０５Ａ及び第１の有機膜

１０３に対してドライエッチングを行なって、図８（ａ）に示すように、パターン化された第２の有機膜１０５Ａに配線溝１１１を形成すると共に、コンタクトホール１１０を有するパターン化された第１の有機膜１０３Ａを形成する。その後、パターン化された有機含有シリコン酸化膜１０４Ａをマスクとしてシリコン窒化膜１０２に対してドライエッチングを行なって、図８（ｂ）に示すように、パターン化されたシリコン窒化膜１０２Ａを形成すると共に、第１の金属配線１０１をコンタクトホール１１０に露出させる。

【００６２】

次に、コンタクトホール１１０及び配線溝１１１の壁面に例えば５０ｎｍの膜厚を有する窒化チタン層からなる密着層１１２を堆積した後、全面に亘って金属膜を堆積し、その後、パターン化された第２の有機膜１０５Ａの上に堆積されている、密着層１１２、金属膜及びマスクパターン１０８を例えばＣＭＰ法により除去する。このようにすると、図８（ｃ）に示すように、窒化チタン膜１１２及び金属膜からなる、第２の金属配線１１４及びコンタクト１１５が形成される。

【００６３】

（第２の実施形態）

以下、本発明の第２の実施形態に係る配線構造体の形成方法について、図９（ａ）～（ｃ）、図１０（ａ）～（ｃ）及び図１１（ａ）～（ｃ）を参照しながら説明する。

【００６４】

まず、図９（ａ）に示すように、半導体基板２００上に形成された第１の金属配線２０１の上に例えば５０ｎｍの膜厚を有するシリコン窒化膜２０２を形成した後、該シリコン窒化膜２０２の上に、例えば１μｍの膜厚を有すると共に有機成分を主成分とする第１の有機膜２０３を堆積する。次に、第１の有機膜２０３の上に、例えば５０ｎｍの膜厚を有すると共にシリコン酸化物中に有機成分を含有する有機含有シリコン酸化膜２０４を堆積した後、該有機含有シリコン酸化膜２０４の上に、例えば４００ｎｍの膜厚を有すると共に有機成分を主成分とする第２の有機膜２０５を堆積し、その後、該第２の有機膜の上に例えば５０ｎｍの膜厚を有する窒化チタン膜２０６を堆積する。

【００６５】

第１及び第２の有機膜２０３、２０５の堆積方法については、特に限定されないが、例えばパーフルオロデカシンを主原料とする反応性ガスを用いるプラズマＣＶＤ法が挙げられる。また、第１及び第２の有機膜２０３、２０５としては、プラズマＣＶＤ法、塗布法又は熱ＣＶＤ法により形成された、炭化水素膜又はフッ素を含有する炭化水素膜を用いることができる。

【００６６】

また、有機含有シリコン酸化膜２０４の堆積方法については、特に限定されないが、例えばフェニルトリメトキシランを主原料とする反応性ガスを用いるＣＶＤ法が挙げられる。

【００６７】

次に、図９（ｂ）に示すように、窒化チタン膜２０６の上に、リソグラフィ工程により配線溝形成用開口部を有する第１のレジストパターン２０７を形成した後、該第１のレジストパターン２０７をマスクとして窒化チタン膜２０６に対してドライエッチングを行なって、図９（ｃ）に示すように、窒化チタン膜２０６からなるマスクパターン２０８を形成する。

【００６８】

次に、第１のレジストパターン２０７を除去することなく、第２の有機膜２０５の上に、リソグラフィ工程によりコンタクトホール形成用開口部を有する第２のレジストパターン２０９を形成した後、第２の有機膜２０５に対してドライエッチングを行なって、図１０（ａ）に示すように、コンタクトホール形成用開口部を有するパターン化された第２の有機膜２０５Ａを形成する。この場合、第２の有機膜２０５と、第１のレジストパターン２０７及び第２のレジストパターン２０９とは共に有機成分を主成分としているため、第２の有機膜２０５に対するエッチングレートと、第１及び第２のレジストパターン２０７、２０９に対するエッチングレートとはほぼ等しいので、第２の有機膜２０５に対するドライエッチング工程により、第１のレジストパターン２０７及び第２のレジストパターン２０９は除去される。

【００６９】

尚、第２のレジストパターン２０９が第１のレジストパターン２０７に対して位置ずれしている恐れがある場合には、第１の実施形態において説明したように、第２のレジストパターン２０９をマスクとして第１のレジストパターン２０７及びマスクパターン２０８に対してドライエッチングを行なって、第１のレジストパターン２０７における第２のレジストパターン２０９と重なっていない領域を除去すると共に、マスクパターン２０８の開口部を配線溝形成用開口部及びコンタクトホール形成用開口部を含む大きさに拡大する。

【００７０】

次に、パターン化された第２の有機膜２０５Ａをマスクとして有機含有シリコン酸化膜２０４に対してドライエッチングを行なって、図１０（ｂ）に示すように、コンタクトホール形成用開口部を有するパターン化された有機含有シリコン酸化膜２０４Ａを形成する。その後、マスクパターン２０８をマスクとしてパターン化された第２の有機膜２０５Ａに対し、またパターン化された有機含有シリコン酸化膜２０４Ａをマスクとして第１の有機膜２０３に対してそれぞれドライエッチングを行なって、図１０（ｃ）に示すように、パターン化された第２の有機膜２０５Ａに配線溝２１１を形成すると共に、コンタクトホール２１０を有するパターン化された第１の有機膜２０３Ａを形成する。

【００７１】

次に、パターン化された有機含有シリコン酸化膜２０３Ａをマスクとしてシリコン窒化膜２０２に対してドライエッチングを行なって、図１１（ａ）に示すように、パターン化されたシリコン窒化膜２０２Ａを形成すると共に、第１の金属配線２０１をコンタクトホール２１０に露出させる。

【００７２】

次に、パターン化された第１の有機膜２０３Ａ及びパターン化された第２の有機膜２０５Ａに対してアンモニアガスを用いるプラズマ処理を行なう。このようにすると、図１１（ｂ）に示すように、パターン化された第１の有機膜２０３Ａにおけるコンタクトホール２１０に露出する壁部及びパターン化された第２の有機膜２０５Ａにおける配線溝２１１に露出する壁部に、アミノ基及びアミド基を

有する密着層２１２がそれぞれ形成される。その後、コンタクトホール２１０及び配線溝２１１が埋まるように全面に亘って金属膜２１３を堆積する。金属膜２１３の組成は特に限定されず、銅、アルミニウム、金、銀、ニッケル、コバルト、タングステン又はこれらの合金等を用いることができると共に、金属膜２１３の堆積方法も特に限定されず、メッキ法、ＣＶＤ法又はスパッタ法等を用いることができる。

【００７３】

次に、図１１（ｃ）に示すように、パターン化された第２の有機膜２０５Ａの上に堆積されている、金属膜２１３及びマスクパターン２０８を例えばＣＭＰ法により除去して、金属膜２１３からなる、第２の金属配線２１４及びコンタクト２１５を形成する。

【００７４】

尚、第２の金属配線２１４の上に、前述した工程と同様の工程を行なうことにより、多層配線構造を形成することができる。

【００７５】

（第３の実施形態）

以下、本発明の第３の実施形態に係る配線構造体の形成方法について、図１２（ａ）～（ｃ）、図１３（ａ）～（ｃ）及び図１４（ａ）～（ｃ）を参照しながら説明する。

【００７６】

まず、図１２（ａ）に示すように、半導体基板３００上に形成された第１の金属配線３０１の上に、後に行なわれるエッチング工程において第１の金属配線３０１を保護する例えば５０ｎｍの膜厚を有するシリコン窒化膜３０２を形成した後、該シリコン窒化膜３０２の上に、例えば１μｍの膜厚を有すると共にシリコン酸化物中に有機成分を含有する第１の有機含有シリコン酸化膜３０３を堆積する。次に、第１の有機含有シリコン酸化膜３０３の上に、例えば４００ｎｍの膜厚を有すると共にシロキサン骨格を有する低誘電率ＳＯＧ膜３０４を堆積した後、該低誘電率ＳＯＧ膜３０４の上に、例えば５０ｎｍの膜厚を有すると共にシリコン酸化物中に有機成分を含有する第２の有機含有シリコン酸化膜３０５を堆積

し、その後、第２の有機含有シリコン酸化膜３０５の上に例えば５０ｎｍの膜厚を有する窒化チタン膜３０６を形成する。

【００７７】

第１の有機含有シリコン酸化膜３０３及び第２の有機含有シリコン酸化膜３０５の堆積方法については、特に限定されないが、例えばフェニルトリメトキシランを主原料とする反応性ガスを用いるＣＶＤ法が挙げられる。また、シロキサン骨格を有する低誘電率ＳＯＧ膜３０４としてはＨＳＱ膜を用いることができる。

【００７８】

次に、図１２（ｂ）に示すように、窒化チタン膜３０６の上に、リソグラフィ工程により配線溝形成用開口部を有する第１のレジストパターン３０７を形成した後、該第１のレジストパターン３０７をマスクとして窒化チタン膜３０６に対してドライエッチングを行なって、図１２（ｃ）に示すように、窒化チタン膜３０６からなるマスクパターン３０８を形成する。

【００７９】

次に、図１３（ａ）に示すように、第１のレジストパターン３０７を除去した後、第２の有機含有シリコン酸化膜３０５の上に、コンタクトホール形成用開口部を有する第２のレジストパターン３０９を形成する。その後、第２のレジストパターン３０９をマスクとして、第２の有機含有シリコン酸化膜３０５、低誘電率ＳＯＧ膜３０４及び第１の有機含有シリコン酸化膜３０３に対して順次ドライエッチングを行なって、図１３（ｂ）に示すように、パターン化された第２の有機含有シリコン酸化膜３０５Ａ、パターン化された低誘電率ＳＯＧ膜３０４Ａ及びコンタクトホール３１０を有するパターン化された第１の有機含有シリコン酸化膜３０３Ａをそれぞれ形成する。

【００８０】

次に、図１３（ｃ）に示すように、第２のレジストパターン３０９を除去した後、マスクパターン３０８をマスクとしてパターン化された第２の有機含有シリコン酸化膜３０５Ａに対してドライエッチングを行なって、パターン化された第２の有機含有シリコン酸化膜３０５Ａに配線溝形成用開口部を形成し、その後、マスクパターン３０８及び配線溝形成用開口部を有するパターン化された第２の

有機含有シリコン酸化膜３０５Ａをマスクとしてパターン化された低誘電率ＳＯＧ膜３０４Ａに対してドライエッチングを行なって配線溝３１１を形成する。配線溝３１１を形成する工程においては、第１の有機含有シリコン酸化膜３０３Ａに対するエッチングレートが低誘電率ＳＯＧ膜３０４Ａに対するエッチングレートに比べて十分に遅くなるようなエッチング条件を設定することにより、パターン化された第１の有機含有シリコン酸化膜３０３Ａに対する十分な選択比を確保できるので、配線溝３１１の深さを第２の有機含有シリコン酸化膜３０５及び低誘電率ＳＯＧ膜３０４の合計膜厚により一義的に決定することができる。

【００８１】

尚、第２のレジストパターン３０９が第１のレジストパターン３０７に対して位置ずれしている恐れがある場合には、第２のレジストパターン３０９をマスクとして第２の有機含有シリコン酸化膜３０５に対してドライエッチングを行なう前に、第２のレジストパターン３０９をマスクとしてマスクパターン３０８に対するドライエッチングを行なうことが好ましい。すなわち、第２のレジストパターン３０９が第１のレジストパターン３０７に対して位置ずれしているために、マスクパターン３０８が第２のレジストパターン３０９のコンタクトホール形成用開口部に露出している場合には、第２のレジストパターン３０９をマスクとしてマスクパターン３０８に対してドライエッチングを行なうことにより、マスクパターン３０８の開口部を配線溝形成用開口部及びコンタクトホール形成用開口部を含む大きさに拡大する。

【００８２】

次に、パターン化された第１の有機含有シリコン酸化膜３０３Ａをマスクとしてシリコン窒化膜３０２に対してドライエッチングを行なって、図１４（ａ）に示すように、パターン化されたシリコン窒化膜３０２Ａを形成すると共に、第１の金属配線３０１をコンタクトホール３１０に露出させる。

【００８３】

次に、図１４（ｂ）に示すように、コンタクトホール３１０及び配線溝３１１の壁面に例えば５０ｎｍの膜厚を有する窒化チタン層からなる密着層３１２を堆積した後、コンタクトホール３１０及び配線溝３１１が埋まるように全面に亘っ

て金属膜３１３を堆積する。金属膜３１３の組成は特に限定されず、銅、アルミニウム、金、銀、ニッケル、コバルト、タングステン又はこれらの合金等を用いることができると共に、金属膜３１３の堆積方法も特に限定されず、メッキ、ＣＶＤ法又はスパッタ法等を用いることができる。

【００８４】

次に、図１４（ｃ）に示すように、パターン化された第２の有機含有シリコン酸化膜３０５Ａの上に堆積されている、密着層３１２、金属膜３１３及びマスクパターン３０８を例えばＣＭＰ法により除去して、金属膜３１３からなる第２の金属配線３１４、及び第１の金属配線３０１と第２の金属配線３１４とを接続する金属膜３１３からなるコンタクト３１５を形成する。

【００８５】

尚、第２の金属配線３１４の上に、前述した工程と同様の工程を行なうことにより、多層配線構造を形成することができる。

【００８６】

第３の実施形態によると、第１のレジストパターン３０７を酸素プラズマを用いるアッシングにより除去する際には、低誘電率ＳＯＧ膜３０４の上に第２の有機含有シリコン酸化膜３０５が存在しているため、低誘電率ＳＯＧ膜３０４が酸素プラズマに曝されることはない。

【００８７】

また、第２のレジストパターン３０９をマスクとして、第２の有機含有シリコン酸化膜３０５、低誘電率ＳＯＧ膜３０４及び第１の有機含有シリコン酸化膜３０３に対して順次ドライエッチングを行なった後、第２のレジストパターン３０９を酸素プラズマを用いるアッシングにより除去するため、パターン化された低誘電率ＳＯＧ膜３０４Ａにおけるコンタクトホール形成用開口部に露出する領域は酸素プラズマに曝されるのでダメージを受ける。しかしながら、パターン化された低誘電率ＳＯＧ膜３０４Ａにおけるダメージ層は、パターン化された低誘電率ＳＯＧ膜３０４Ａに配線溝３１１を形成する際に除去されるので、後工程において悪影響を及ぼさない。

【００８８】

従って、低誘電率ＳＯＧ膜３０４としては、酸素プラズマによって劣化する材料を使用することが可能である。例えば、ＨＳＱ膜は、酸素プラズマに曝されると、Ｓｉ－Ｈ結合が酸化されてしまうため、含有水分量の増加及び比誘電率の増加が起こって、素子の信頼性及び性能の劣化が引き起こされるが、第３の実施形態によると、配線溝３１１が形成された後のパターン化された低誘電率ＳＯＧ膜３０４Ａは酸素プラズマの影響を受けていないので、層間絶縁膜としてＨＳＱ膜を用いても、素子の信頼性及び性能の劣化を回避することができる。

【００８９】

（第３の実施形態の変形例）

以下、本発明の第３の実施形態の変形例に係る配線構造体の形成方法について、図１５（ａ）～（ｃ）、図１６（ａ）～（ｄ）及び図１７（ａ）～（ｃ）を参照しながら説明する。

【００９０】

まず、図１５（ａ）に示すように、半導体基板３５０上に形成された第１の金属配線３５１の上に、後に行なわれるエッチング工程において第１の金属配線３５１を保護する例えば５０ｎｍの膜厚を有するシリコン窒化膜３５２を形成した後、該シリコン窒化膜３５２の上に、例えば１μｍの膜厚を有する第１のシリコン酸化膜３５３を堆積する。次に、第１のシリコン酸化膜３５３の上に、例えば４００ｎｍの膜厚を有する有機膜３５４を堆積した後、該有機膜３５４の上に、例えば５０ｎｍの膜厚を有する第２のシリコン酸化膜３５５を堆積し、その後、第２のシリコン酸化膜３５５の上に例えば５０ｎｍの膜厚を有する窒化チタン膜３５６を形成する。

【００９１】

第１のシリコン酸化膜３５３及び第２のシリコン酸化膜３５５の堆積方法については、特に限定されないが、例えばフェニルトリメトキシランを主原料とする反応性ガスを用いるＣＶＤ法が挙げられる。

【００９２】

次に、図１５（ｂ）に示すように、窒化チタン膜３５６の上に、リソグラフィ

工程により配線溝形成用開口部を有する第１のレジストパターン３５７を形成した後、該第１のレジストパターン３５７をマスクとして窒化チタン膜３５６に対してドライエッチングを行なって、図１５（ｃ）に示すように、窒化チタン膜３５６からなるマスクパターン３５８を形成する。

【００９３】

次に、図１６（ａ）に示すように、第１のレジストパターン３５７を除去した後、第２のシリコン酸化膜３５５の上に、コンタクトホール形成用開口部を有する第２のレジストパターン３５９を形成する。その後、第２のレジストパターン３５９をマスクとして、第２のシリコン酸化膜３５５及び有機膜３５４に対して順次ドライエッチングを行なって、図１６（ｂ）に示すように、コンタクトホール形成用開口部３６０を有する、パターン化された第２のシリコン酸化膜３５５Ａ及びパターン化された有機膜３５４Ａをそれぞれ形成する。この場合、有機膜３５４に対するエッチング工程において第２のレジストパターン３５９が除去される。

【００９４】

次に、図１６（ｃ）に示すように、パターン化された第２のシリコン酸化膜３５５Ａ及びパターン化された有機膜３５４Ａをマスクとして第１のシリコン酸化膜３５３に対してドライエッチングを行なって、コンタクトホール３６１を有するパターン化された第１のシリコン酸化膜３５３Ａを形成する。このエッチング工程において、パターン化された第２のシリコン酸化膜３５５Ａにマスクパターン３５８が転写されるので、パターン化された第２のシリコン酸化膜３５５Ａに配線溝形成用開口部が形成される。

【００９５】

次に、図１６（ｄ）に示すように、マスクパターン３５８及び配線溝形成用開口部を有するパターン化された第２のシリコン酸化膜３５５Ａをマスクとしてパターン化された有機膜３５４Ａに対してドライエッチングを行なって配線溝３６２を形成する。配線溝３６２を形成する工程においては、第１のシリコン酸化膜３５３Ａに対するエッチングレートが有機膜３５４Ａに対するエッチングレートに比べて十分に遅くなるようなエッチング条件を設定することにより、パターン

化された第１のシリコン酸化膜３５３Ａに対する十分な選択比を確保できるので、配線溝３６２の深さを第２のシリコン酸化膜３５５及び有機膜３５４の合計膜厚により一義的に決定することができる。

【００９６】

尚、第２のレジストパターン３５９が第１のレジストパターン３５７に対して位置ずれしている恐れがある場合には、第２のレジストパターン３５９をマスクとして第２のシリコン酸化膜３５５に対してドライエッチングを行なう前に、第２のレジストパターン３５９をマスクとしてマスクパターン３５８に対するドライエッチングを行なうことが好ましい。すなわち、第２のレジストパターン３５９が第１のレジストパターン３５７に対して位置ずれしているために、マスクパターン３５８が第２のレジストパターン３５９のコンタクトホール形成用開口部に露出している場合には、第２のレジストパターン３５９をマスクとしてマスクパターン３５８に対してドライエッチングを行なうことにより、マスクパターン３５８の開口部を配線溝形成用開口部及びコンタクトホール形成用開口部を含む大きさに拡大する。

【００９７】

次に、パターン化された第１のシリコン酸化膜３５３Ａをマスクとしてシリコン窒化膜３５２に対してドライエッチングを行なって、図１７（ａ）に示すように、パターン化されたシリコン窒化膜３５２Ａを形成すると共に、第１の金属配線３５１をコンタクトホール３６１に露出させる。

【００９８】

次に、図１７（ｂ）に示すように、コンタクトホール３６１及び配線溝３６２の壁面に例えば５０ｎｍの膜厚を有する窒化チタン層からなる密着層３６３を堆積した後、コンタクトホール３６１及び配線溝３６２が埋まるように全面に亘って金属膜３６４を堆積する。金属膜３６４の組成は特に限定されず、銅、アルミニウム、金、銀、ニッケル、コバルト、タングステン又はこれらの合金等を用いることができると共に、金属膜３６４の堆積方法も特に限定されず、メッキ法、ＣＶＤ法又はスパッタ法等を用いることができる。

【００９９】

次に、図１７（ｃ）に示すように、パターン化された第２のシリコン酸化膜３５５Ａの上に堆積されている、密着層３６３、金属膜３６４及びマスクパターン３５８を例えばＣＭＰ法により除去して、金属膜３６４からなる第２の金属配線３６５、及び第１の金属配線３５１と第２の金属配線３６５とを接続する金属膜３６４からなるコンタクト３６６を形成する。

【０１００】

尚、第２の金属配線３６５の上に、前述した工程と同様の工程を行なうことにより、多層配線構造を形成することができる。

【０１０１】

第３の実施形態の変形例によると、第１のレジストパターン３５７を酸素プラズマを用いるアッシングにより除去する際には、有機膜３５４の上に第２のシリコン酸化膜３５５が存在しているため、有機膜３５４が酸素プラズマに曝されることはない。

【０１０２】

また、第２のレジストパターン３５９をマスクとして、第２のシリコン酸化膜３５５及び有機膜３５４に対してドライエッチングを行なう際に、第２のレジストパターン３５９が除去されるため、第２のレジストパターン３５９を酸素プラズマを用いるアッシングによって除去する必要がないので、有機膜３５４は酸素プラズマに曝されることがない。

【０１０３】

（第４の実施形態）

以下、本発明の第４の実施形態に係る配線構造体の形成方法について、図１８（ａ）～（ｃ）、図１９（ａ）～（ｃ）及び図２０（ａ）～（ｃ）を参照しながら説明する。

【０１０４】

まず、図１８（ａ）に示すように、半導体基板４００上に形成された第１の金属配線４０１の上に、後に行なわれるエッチング工程において第１の金属配線４０１を保護する例えば５０ｎｍの膜厚を有するシリコン窒化膜４０２を形成した

後、該シリコン窒化膜４０２の上に、例えば１μｍの膜厚を有すると共にシロキサン骨格を有する第１の低誘電率ＳＯＧ膜４０３を堆積する。次に、第１の低誘電率ＳＯＧ膜４０３の上に、例えば５０ｎｍの膜厚を有すると共にシリコン酸化物中に有機成分を含有する有機含有シリコン酸化膜４０４を堆積した後、該有機含有シリコン酸化膜４０４の上に、例えば４００ｎｍの膜厚を有すると共にシロキサン骨格を有する第２の低誘電率ＳＯＧ膜４０５を堆積し、その後、該第２の低誘電率ＳＯＧ膜４０５の上に例えば５０ｎｍの膜厚を有する窒化チタン膜４０６を堆積する。

【０１０５】

第１及び第２の低誘電率ＳＯＧ膜４０３、４０５としては例えばＨＳＱ膜を用いることができる。また、有機含有シリコン酸化膜４０４の堆積方法については、特に限定されないが、例えばフェニルトリメトキシランを主原料とする反応性ガスを用いるＣＶＤ法が挙げられる。このようにすると、シリコン酸化物中にシリコン原子と結合したフェニル基が取り込まれた構造を有する有機含有シリコン酸化膜４０４が得られる。

【０１０６】

次に、図１８（ｂ）に示すように、窒化チタン膜４０６の上に、リソグラフィ工程により配線溝形成用開口部を有する第１のレジストパターン４０７を形成した後、該第１のレジストパターン４０７をマスクとして窒化チタン膜４０６に対してドライエッチングを行なって、図１８（ｃ）に示すように、窒化チタン膜４０６からなるマスクパターン４０８を形成する。

【０１０７】

次に、第１のレジストパターン４０７を除去することなく、第２の低誘電率ＳＯＧ膜４０５の上に、リソグラフィ工程によりコンタクトホール形成用開口部を有する第２のレジストパターン４０９を形成した後、該第２のレジストパターン４０９をマスクとして、第２の低誘電率ＳＯＧ膜４０５及び有機含有シリコン酸化膜４０４に対して順次ドライエッチングを行なって、図１９（ａ）に示すように、パターン化された第２の低誘電率ＳＯＧ膜４０５Ａ及びパターン化された有機含有シリコン酸化膜４０４Ａをそれぞれ形成する。

【０１０８】

次に、第１及び第２のレジストパターン４０７、４０９を酸素プラズマを用いるアッシングにより除去すると、図１９（ｂ）に示すように、パターン化された第２の低誘電率ＳＯＧ膜４０５Ａ及び第１の低誘電率ＳＯＧ膜４０３におけるコンタクトホール形成用開口部に露出する領域にダメージ層４１０が形成されてしまう。

【０１０９】

次に、マスクパターン４０８をマスクとしてパターン化された第２の低誘電率ＳＯＧ膜４０５Ａに対して、またパターン化された有機含有シリコン酸化膜４０４Ａをマスクとして第１の低誘電率ＳＯＧ膜４０３に対してそれぞれドライエッチングを行なって、図１９（ｃ）に示すように、パターン化された第２の低誘電率ＳＯＧ膜４０５Ａに配線溝４１２を形成すると共に、コンタクトホール４１１を有するパターン化された第１の低誘電率ＳＯＧ膜４０３Ａを形成する。このドライエッチング工程により、パターン化された第２の低誘電率ＳＯＧ膜４０５Ａ及び第１の低誘電率ＳＯＧ膜４０３のダメージ層４１０は除去される。

【０１１０】

次に、パターン化された有機含有シリコン酸化膜４０４Ａをマスクとしてシリコン窒化膜４０２に対してドライエッチングを行なって、図２０（ａ）に示すように、パターン化されたシリコン窒化膜４０２Ａを形成すると共に、第１の金属配線４０１をコンタクトホール４１１に露出させる。

【０１１１】

次に、図２０（ｂ）に示すように、コンタクトホール４１１及び配線溝４１２の壁面に例えば５０ｎｍの膜厚を有する窒化チタン層からなる密着層４１３を堆積した後、コンタクトホール４１１及び配線溝４１２が埋まるように全面に亘って金属膜４１４を堆積する。金属膜４１４の組成は特に限定されず、銅、アルミニウム、金、銀、ニッケル、コバルト、タングステン又はこれらの合金等を用いることができると共に、金属膜４１４の堆積方法も特に限定されず、メッキ法、ＣＶＤ法又はスパッタ法等を用いることができる。

【０１１２】

次に、図２０（ｃ）に示すように、パターン化された第２の低誘電率ＳＯＧ膜４０５Ａの上に堆積されている、密着層４１３、金属膜４１４及びマスクパターン４０８を例えばＣＭＰ法により除去して、金属膜４１４からなる第２の金属配線４１５、及び第１の金属配線４０１と第２の金属配線４１５とを接続する金属膜４１４からなるコンタクト４１６を形成する。

【０１１３】

尚、第２の金属配線１１４の上に、前述した工程と同様の工程を行なうことにより、多層配線構造を形成することができる。

【０１１４】

第４の実施形態によると、第１及び第２のレジストパターン４０７、４０９を酸素プラズマを用いるアッシングにより除去する際に、パターン化された第２の低誘電率ＳＯＧ膜４０５Ａ及び第１の低誘電率ＳＯＧ膜４０３にダメージ層４１０が形成されてしまうが、該ダメージ層４１０はコンタクトホール４１１及び配線溝４１２を形成する際に除去される。

【０１１５】

従って、第１及び第２の低誘電率ＳＯＧ膜４０３、４０５としては、酸素プラズマによって劣化する材料を使用することが可能である。例えば、ＨＳＱ膜は、酸素プラズマに曝されると、Ｓｉ－Ｈ結合が酸化されてしまうため、含有水分量の増加及び比誘電率の増加が起こって、素子の信頼性及び性能の劣化が引き起こされるが、第４の実施形態によると、コンタクトホール４１１が形成された後のパターン化された第１の低誘電率ＳＯＧ膜４０３Ａ、及び配線溝４１２が形成された後のパターン化された第２の低誘電率ＳＯＧ膜４０５Ａは酸素プラズマの影響を受けていないので、層間絶縁膜としてＨＳＱ膜を用いても、素子の信頼性及び性能の劣化を回避することができる。

【０１１６】

【発明の効果】

第１の配線構造体の形成方法によると、第１のレジストパターン及び第２のレジストパターンを酸素プラズマを用いるアッシングにより除去する工程が不要に

なり、レジストパターンをアッシングにより除去する際に第３の絶縁膜がダメージを受ける事態を回避できるため、第３の絶縁膜として、酸素プラズマによりダメージを受けるが比誘電率は低い絶縁膜を用いることが可能になるので、通常のレジストプロセスを採用しつつ比誘電率が低い層間絶縁膜を形成することができる。

【０１１７】

また、第１０の工程において、第３の絶縁膜に対してマスクパターンをマスクとしてドライエッチングを行なって配線溝を形成する際に第２の絶縁膜をエッチングストッパーとできるため、配線溝の深さを第３の絶縁膜の膜厚と一致させることができるので、配線溝の深さを自己整合的に規定することができる。

【０１１８】

第１の配線構造体の形成方法が、第１０の工程と第１１の工程との間に、第３の絶縁膜における配線溝に露出している部分及び第１の絶縁膜におけるコンタクトホールに露出している部分に金属膜からなる密着層を形成する工程を備えていると、上層の金属配線と第３の絶縁膜との密着性及びコンタクトと第１の絶縁膜との密着性を確保することができる。

【０１１９】

第１の配線構造体の形成方法において、第３の絶縁膜が有機成分を主成分とすると、第８の工程において、第３の絶縁膜、第１のレジストパターン及び第２のレジストパターンに対するエッチングレートが高い一方、第２の絶縁膜に対するエッチングレートが低いエッチング条件を確実に実現することができる。

【０１２０】

この場合、第３の工程が、パーフルオロデカリンを含む反応性ガスを用いるＣＶＤ法により第３の絶縁膜を形成する工程を含むと、有機成分を主成分とし且つ比誘電率が低い第３の絶縁膜を確実に形成することができる。

【０１２１】

また、この場合、第１の絶縁膜も有機成分を主成分とすると、第９の工程において、第２の絶縁膜に対するエッチングレートが高い一方、第１の絶縁膜及び第３の絶縁膜に対するエッチングレートが低いエッチング条件を確実に実現できる

と共に、第１０の工程において、第１の絶縁膜及び第３の絶縁膜に対するエッチングレートが高い一方、マスクパターン及び第２の絶縁膜に対するエッチングレートが低いエッチング条件を確実に実現することができる。

【０１２２】

第１の絶縁膜及び第２の絶縁膜が有機成分を主成分とする場合において、第１０の工程と第１１の工程との間に、第３の絶縁膜における配線溝に露出している部分及び第１の絶縁膜におけるコンタクトホールに露出している部分に、窒素を含有する反応性ガスを用いるプラズマ処理によって密着層を形成する工程を備えていると、上層の金属配線及びコンタクトと、有機成分を主成分とする第１の絶縁膜及び第３の絶縁膜との密着性を確実に確保することができる。

【０１２３】

第１の絶縁膜が有機成分を主成分とする場合において、第１の工程が、パーフルオロデカリンを含む反応性ガスを用いるＣＶＤ法により第１の絶縁膜を形成工程を含むと、有機成分を主成分とし且つ比誘電率が低い第１の絶縁膜を確実に形成することができる。

【０１２４】

第２の配線構造体の形成方法によると、第１０の工程において、第１のレジストパターン及び第２のレジストパターンを除去する際に、第１の絶縁膜及び第３の絶縁膜における第２の絶縁膜のコンタクトホール形成用開口部に露出している部分にダメージ層が形成されても、該ダメージ層は第１１の工程において確実に除去されるため、第１及び第３の絶縁膜として、酸素プラズマによりダメージを受けるが比誘電率は低い絶縁膜を用いることが可能になるので、通常のレジストプロセスを採用しつつ比誘電率が低い層間絶縁膜を形成することができる。

【０１２５】

第２の配線構造体の形成方法において、第３の絶縁膜がシロキサン骨格を有する低誘電率ＳＯＧ膜であると、通常のレジストプロセスを採用しつつ比誘電率が低い層間絶縁膜を確実に形成することができる。

【図面の簡単な説明】

【図１】

（ａ）～（ｃ）は本発明の第１の実施形態に係る配線構造体の形成方法を示す断面図である。

【図２】

（ａ）～（ｃ）は本発明の第１の実施形態に係る配線構造体の形成方法を示す断面図である。

【図３】

（ａ）～（ｃ）は本発明の第１の実施形態に係る配線構造体の形成方法を示す断面図である。

【図４】

（ａ）～（ｃ）は本発明の第１の実施形態に係る配線構造体の形成方法において、第２のレジストパターンが位置ずれを起こした場合の問題点を説明する断面図である。

【図５】

（ａ）～（ｃ）は本発明の第１の実施形態に係る配線構造体の形成方法において、第２のレジストパターンが位置ずれを起こした場合の問題点を説明する断面図である。

【図６】

（ａ）～（ｃ）は本発明の第１の実施形態に係る配線構造体の形成方法において、第２のレジストパターンが位置ずれを起こした場合の問題点を説明する断面図である。

【図７】

（ａ）～（ｃ）は本発明の第１の実施形態に係る配線構造体の形成方法において、第２のレジストパターンが位置ずれを起こした場合の解決策を説明する断面図である。

【図８】

（ａ）～（ｃ）は本発明の第１の実施形態に係る配線構造体の形成方法において、第２のレジストパターンが位置ずれを起こした場合の解決策を説明する断面

図である。

【図９】

（ａ）～（ｃ）は本発明の第２の実施形態に係る配線構造体の形成方法を示す断面図である。

【図１０】

（ａ）～（ｃ）は本発明の第２の実施形態に係る配線構造体の形成方法を示す断面図である。

【図１１】

（ａ）～（ｃ）は本発明の第２の実施形態に係る配線構造体の形成方法を示す断面図である。

【図１２】

（ａ）～（ｃ）は本発明の第３の実施形態に係る配線構造体の形成方法を示す断面図である。

【図１３】

（ａ）～（ｃ）は本発明の第３の実施形態に係る配線構造体の形成方法を示す断面図である。

【図１４】

（ａ）～（ｃ）は本発明の第３の実施形態に係る配線構造体の形成方法を示す断面図である。

【図１５】

（ａ）～（ｃ）は本発明の第３の実施形態の変形例に係る配線構造体の形成方法を示す断面図である。

【図１６】

（ａ）～（ｄ）は本発明の第３の実施形態の変形例に係る配線構造体の形成方法を示す断面図である。

【図１７】

（ａ）～（ｃ）は本発明の第３の実施形態の変形例に係る配線構造体の形成方法を示す断面図である。

【図１８】

（ａ）～（ｃ）は本発明の第４の実施形態に係る配線構造体の形成方法を示す断面図である。

【図１９】

（ａ）～（ｃ）は本発明の第４の実施形態に係る配線構造体の形成方法を示す断面図である。

【図２０】

（ａ）～（ｃ）は本発明の第４の実施形態に係る配線構造体の形成方法を示す断面図である。

【符号の説明】

１００　半導体基板

１０１　第１の金属膜

１０２　シリコン窒化膜

１０２Ａ　パターン化されたシリコン窒化膜

１０３　第１の有機膜

１０３Ａ　パターン化された第１の有機膜

１０４　有機含有シリコン酸化膜

１０４Ａ　パターン化された有機含有シリコン酸化膜

１０５　第２の有機膜

１０５Ａ　パターン化された第２の有機膜

１０６　窒化チタン膜

１０７　第１のレジストパターン

１０８　マスクパターン

１０９　第２のレジストパターン

１１０　コンタクトホール

１１１　配線溝

１１２　密着層

１１３　金属膜

１１４　第２の金属配線

１１５　コンタクト

２００　半導体基板

２０１　第１の金属膜

２０２　シリコン窒化膜

２０２Ａ　パターン化されたシリコン窒化膜

２０３　第１の有機膜

２０３Ａ　パターン化された第１の有機膜

２０４　有機含有シリコン酸化膜

２０４Ａ　パターン化された有機含有シリコン酸化膜

２０５　第２の有機膜

２０５Ａ　パターン化された第２の有機膜

２０６　窒化チタン膜

２０７　第１のレジストパターン

２０８　マスクパターン

２０９　第２のレジストパターン

２１０　コンタクトホール

２１１　配線溝

２１２　密着層

２１３　金属膜

２１４　第２の金属配線

２１５　コンタクト

３００　半導体基板

３０１　第１の金属膜

３０２　シリコン窒化膜

３０２Ａ　パターン化されたシリコン窒化膜

３０３　第１の有機含有シリコン酸化膜

３０３Ａ　パターン化された第１の有機含有シリコン酸化膜

３０４　低誘電率ＳＯＧ膜

３０５　第２の有機含有シリコン酸化膜

３０５Ａ　パターン化された第２の有機含有シリコン酸化膜
３０６　窒化チタン膜
３０７　第１のレジストパターン
３０８　マスクパターン
３０９　第２のレジストパターン
３１０　コンタクトホール
３１１　配線溝
３１２　密着層
３１３　金属膜
３１４　第２の金属配線
３１５　コンタクト
３５０　半導体基板
３５１　第１の金属膜
３５２　シリコン窒化膜
３５２Ａ　パターン化されたシリコン窒化膜
３５３　第１のシリコン酸化膜
３５３Ａ　パターン化された第１のシリコン酸化膜
３５４　有機膜
３５５　第２のシリコン酸化膜
３５５Ａ　パターン化された第２のシリコン酸化膜
３５６　窒化チタン膜
３５７　第１のレジストパターン
３５８　マスクパターン
３５９　第２のレジストパターン
３６０　コンタクトホール形成用開口部
３６１　コンタクトホール
３６２　配線溝
３６３　密着層
３６４　金属膜

３６５　第２の金属配線

３６６　コンタクト

４００　半導体基板

４０１　第１の金属配線

４０２　シリコン窒化膜

４０２Ａ　パターン化されたシリコン窒化膜

４０３　第１の低誘電率ＳＯＧ膜

４０３Ａ　パターン化された第１の低誘電率ＳＯＧ膜

４０４　有機含有シリコン酸化膜

４０４Ａ　パターン化された有機含有シリコン酸化膜

４０５　第２の低誘電率ＳＯＧ膜

４０５Ａ　パターン化された第２の低誘電率ＳＯＧ膜

４０６　窒化チタン膜

４０７　第１のレジストパターン

４０８　マスクパターン

４０９　第２のレジストパターン

４１０　ダメージ層

４１１　コンタクトホール

４１２　配線溝

４１３　密着層

４１４　金属膜

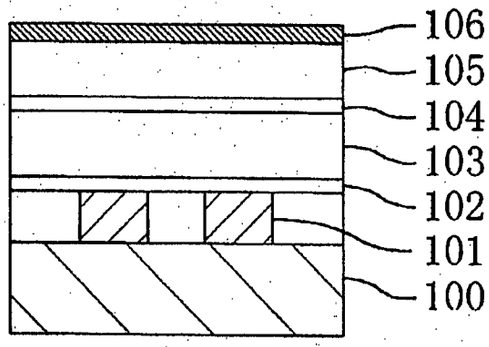
４１５　第２の金属膜

４１６　コンタクト

【書類名】　図面

【図１】

(a)


106
105
104
103
102
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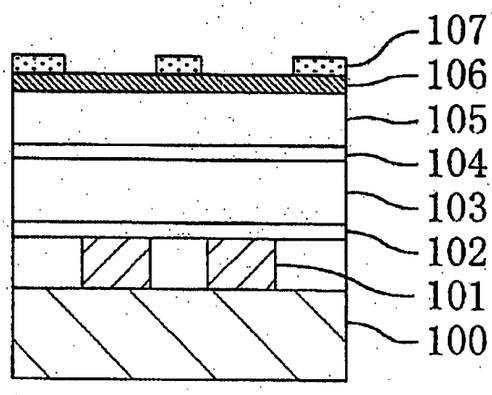
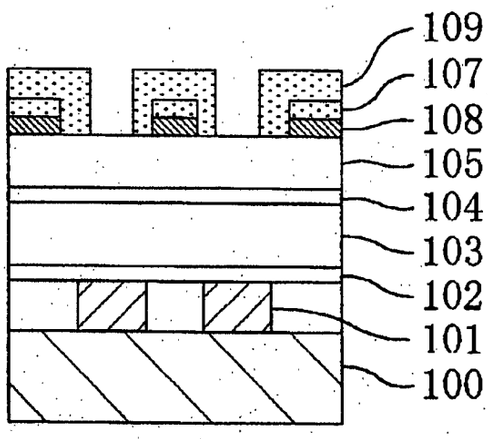
100

(b)

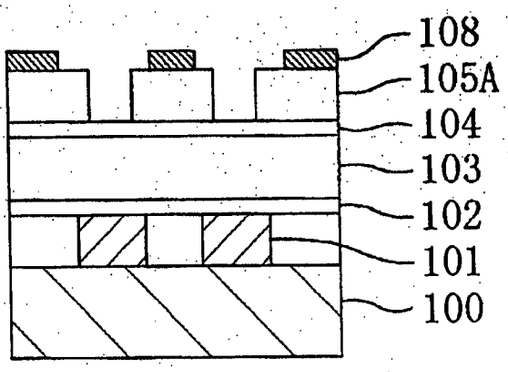

107
106
105
104
103
102
101
100

(c)

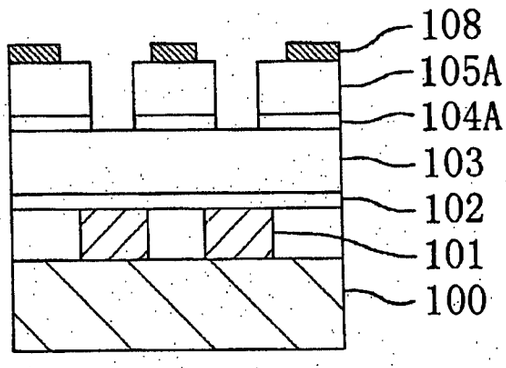

109
107
108
105
104
103
102
101
100

【図２】

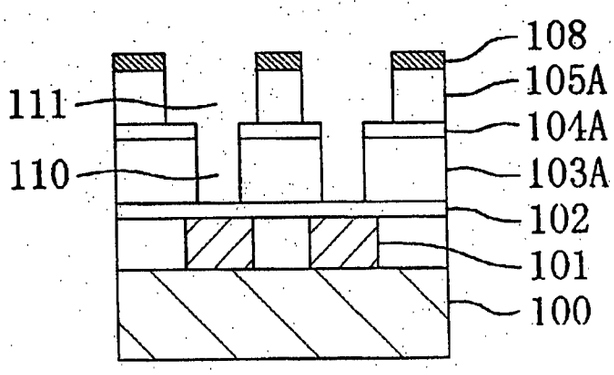
(a)


108
105A
104
103
102
101
100

(b)


108
105A
104A
103
102
101
100

(c)


111
110
108
105A
104A
103A
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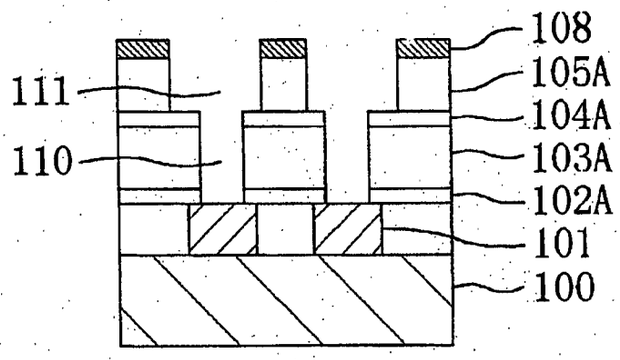
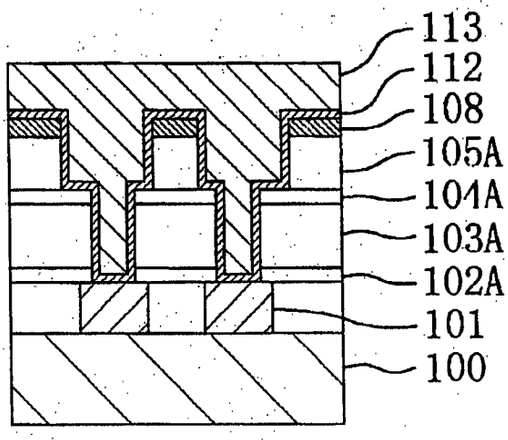
【図３】

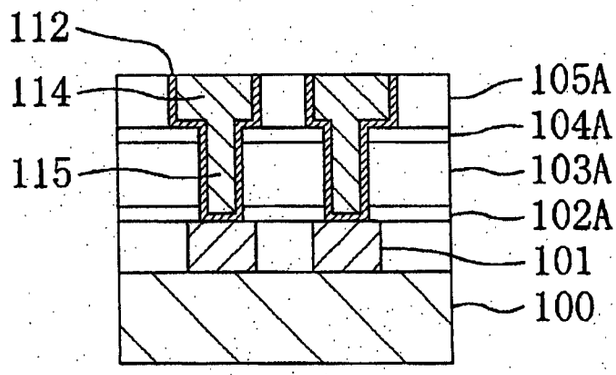
(a)


108
105A
111
104A
110
103A
102A
101
100

(b)


113
112
108
105A
104A
103A
102A
101
100

(c)


112
114
105A
104A
115
103A
102A
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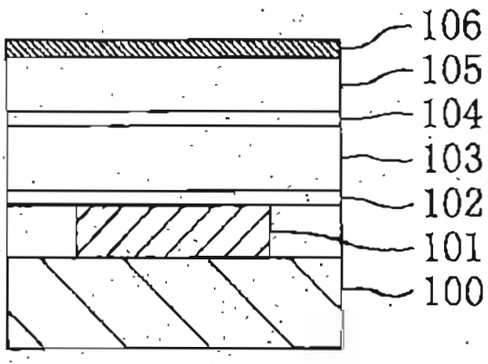
【図４】

(a)


106
105
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103
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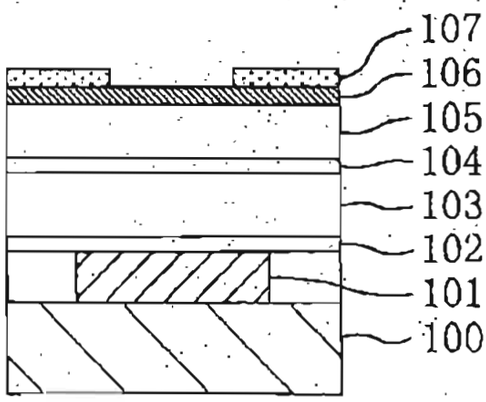
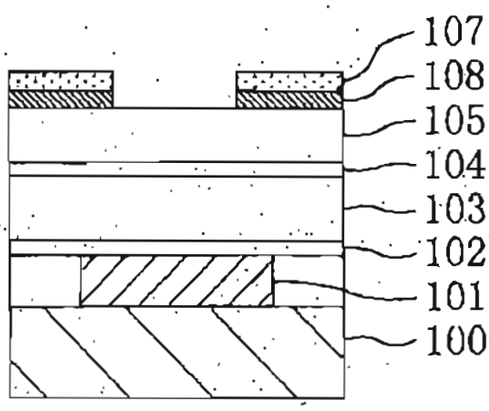
(b)


107
106
105
104
103
102
101
100

(c)


107
108
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104
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102
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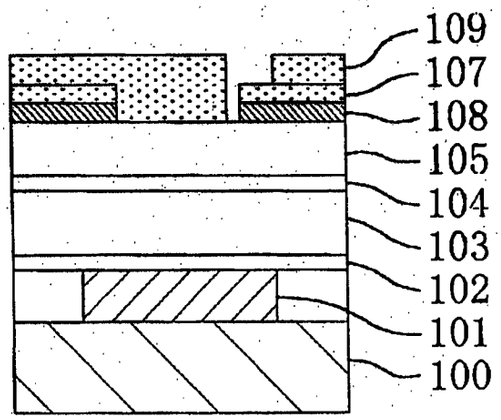
100

【図５】

(a)


109
107
108
105
104
103
102
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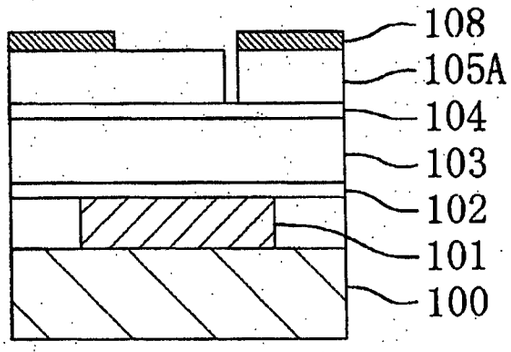
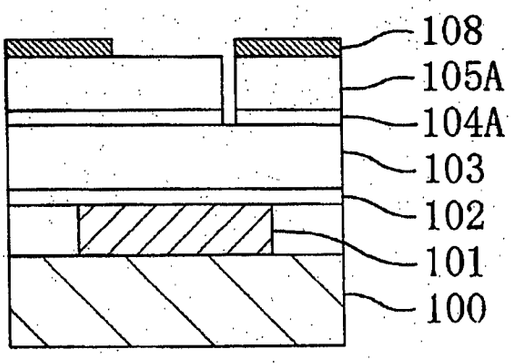
100

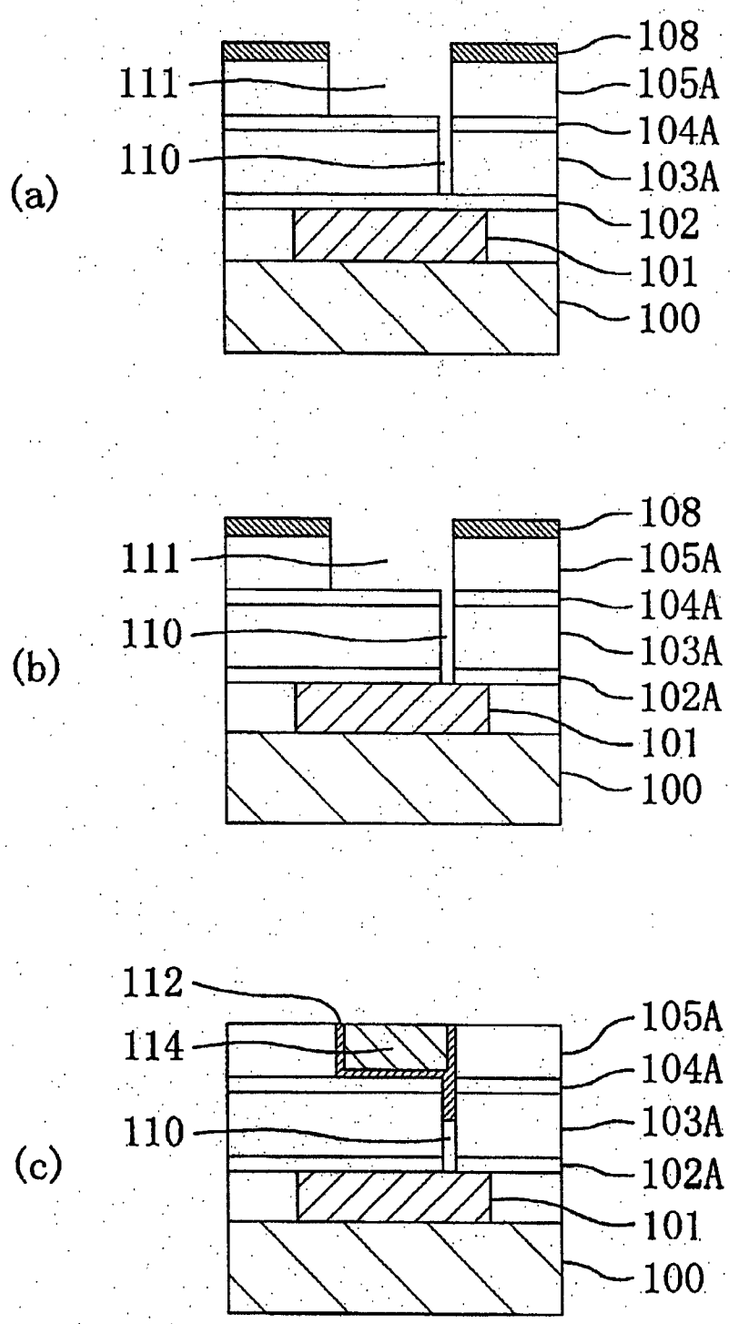
(b)


108
105A
104
103
102
101
100

(c)

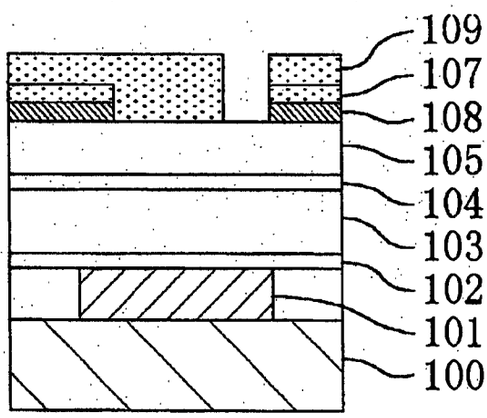

108
105A
104A
103
102
101
100

【図６】

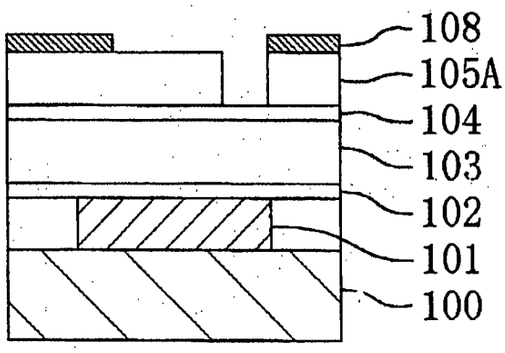

(a)
111
110
108
105A
104A
103A
102
101
100
(b)
111
110
108
105A
104A
103A
102A
101
100
(c)
112
114
110
105A
104A
103A
102A
101
100

【図７】

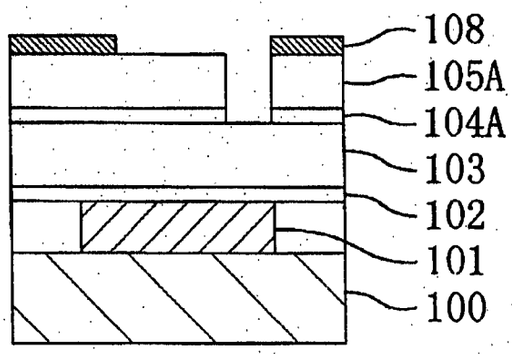
(a)


109
107
108
105
104
103
102
101
100

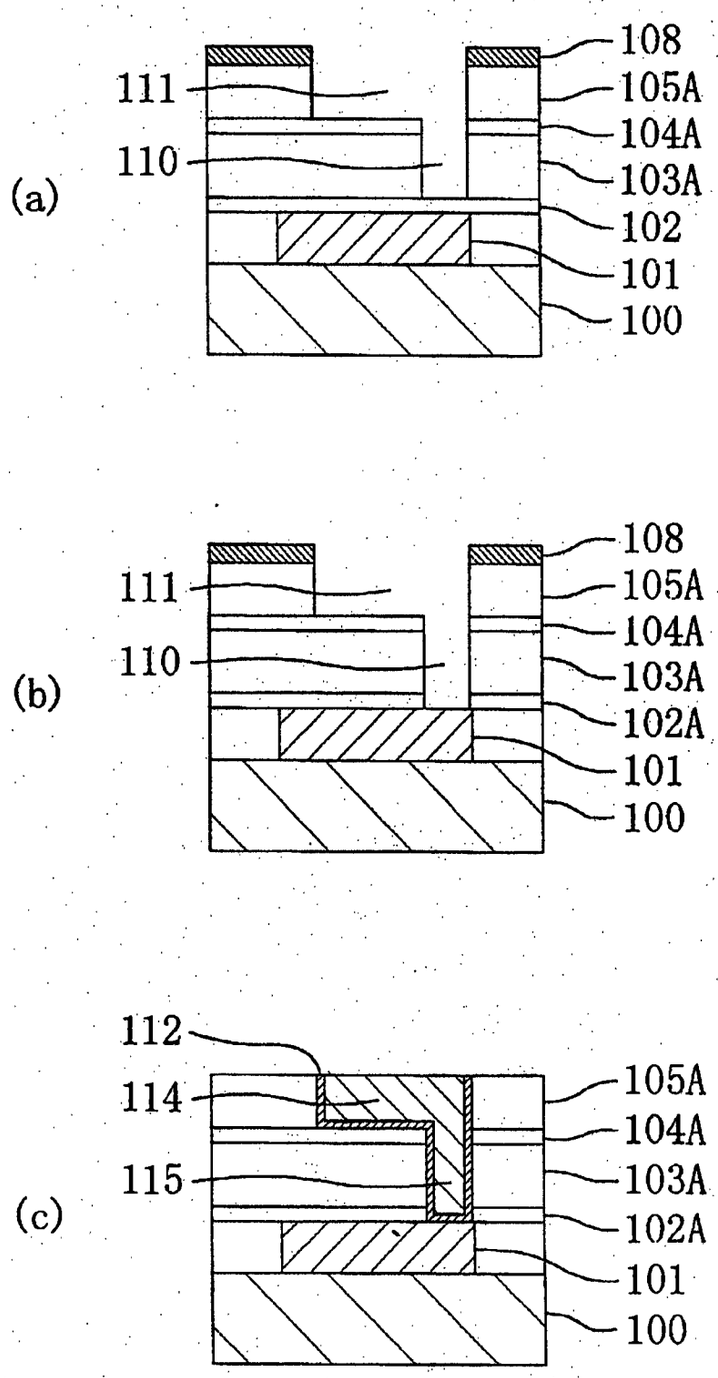
(b)


108
105A
104
103
102
101
100

(c)

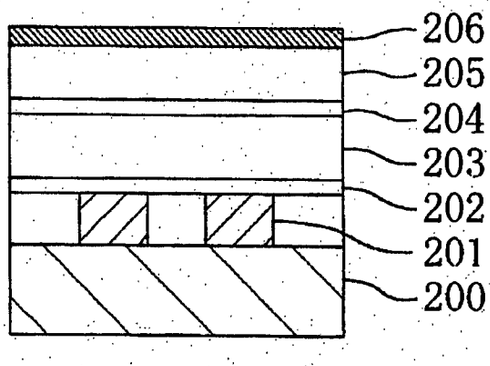

108
105A
104A
103
102
101
100

【図８】

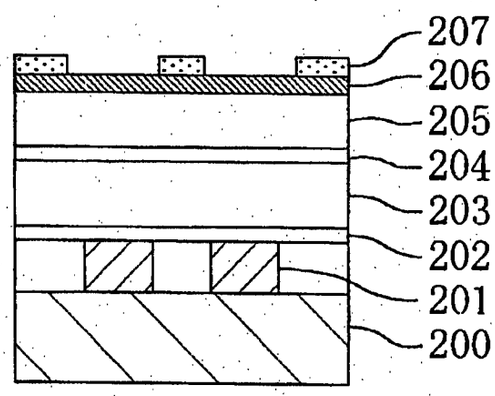

(a)
111
110
108
105A
104A
103A
102
101
100
(b)
111
110
108
105A
104A
103A
102A
101
100
(c)
112
114
115
105A
104A
103A
102A
101
100

【図９】

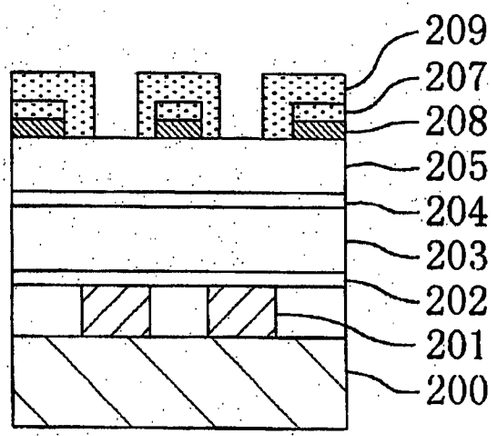
(a)


206
205
204
203
202
201
200

(b)

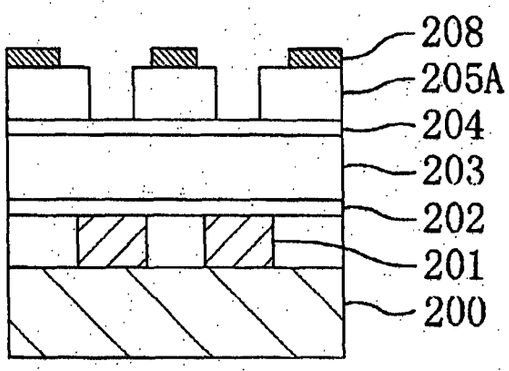

207
206
205
204
203
202
201
200

(c)

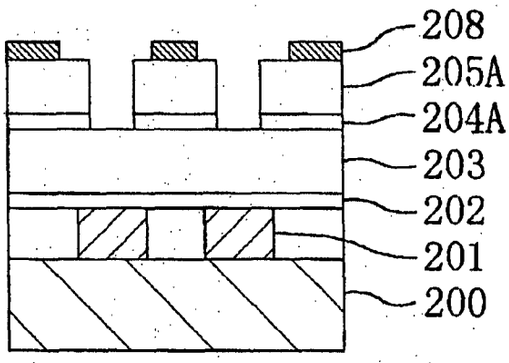

209
207
208
205
204
203
202
201
200

【図１０】

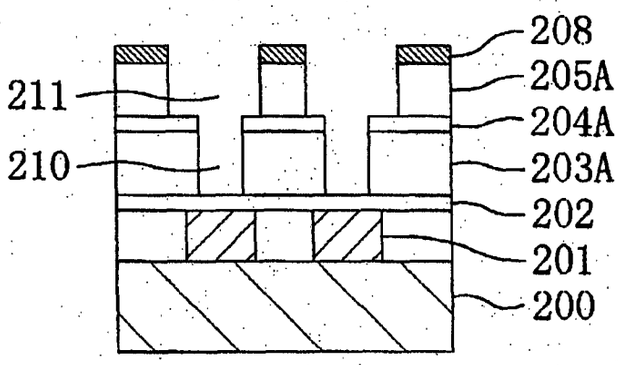
(a)


208
205A
204
203
202
201
200

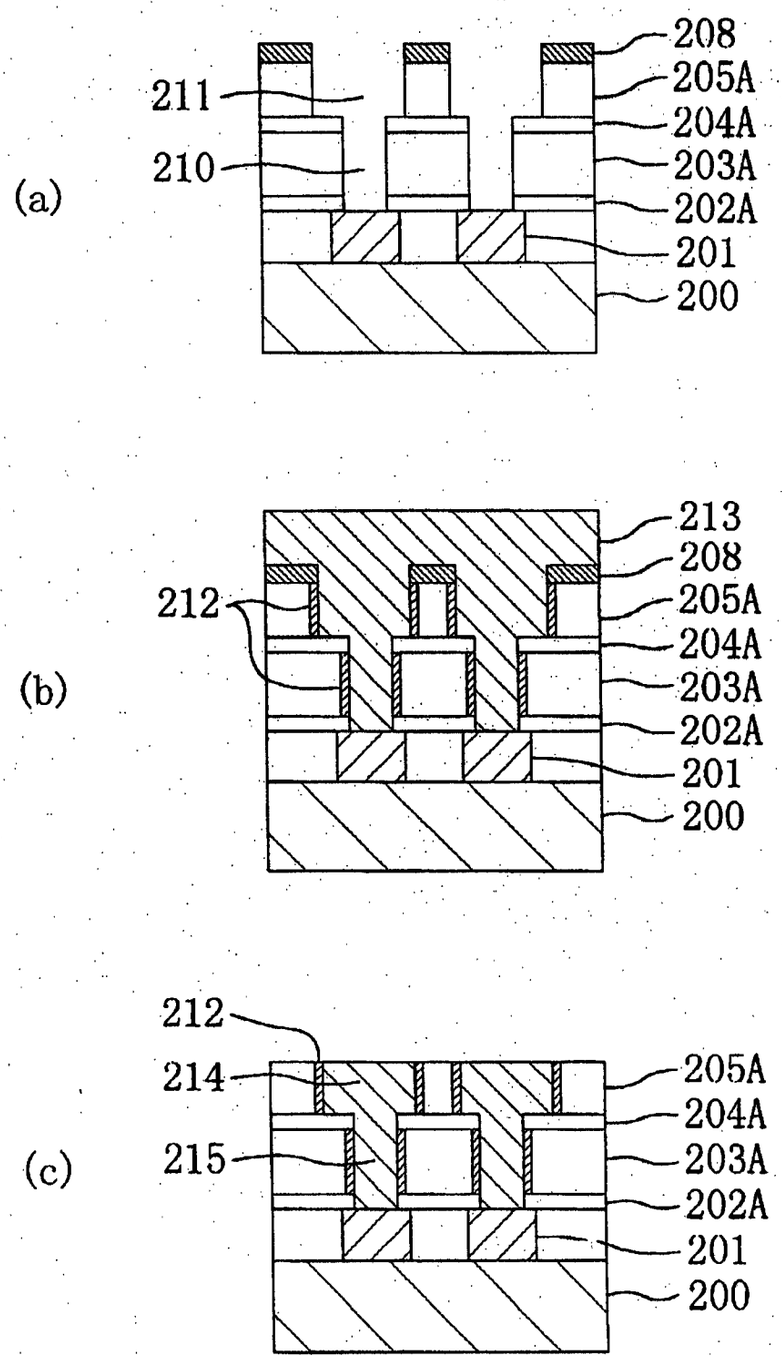
(b)


208
205A
204A
203
202
201
200

(c)

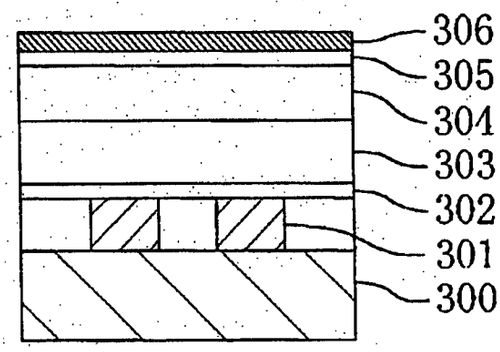

211
210
208
205A
204A
203A
202
201
200

【図１１】

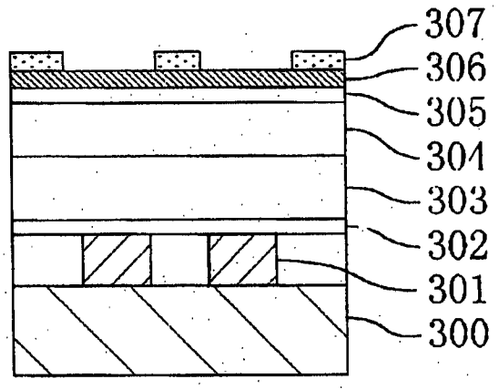

(a)
208
205A
211
204A
210
203A
202A
201
200
(b)
213
208
212
205A
204A
203A
202A
201
200
(c)
212
214
205A
204A
215
203A
202A
201
200

【図１２】

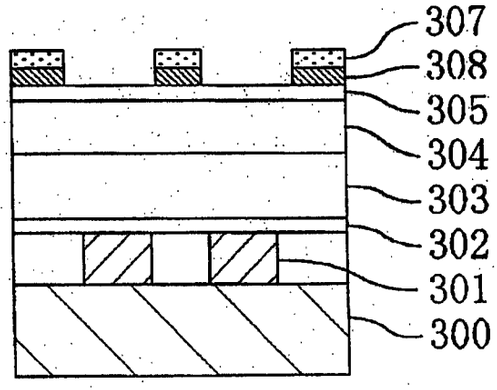
(a)


306
305
304
303
302
301
300

(b)


307
306
305
304
303
302
301
300

(c)


307
308
305
304
303
302
301
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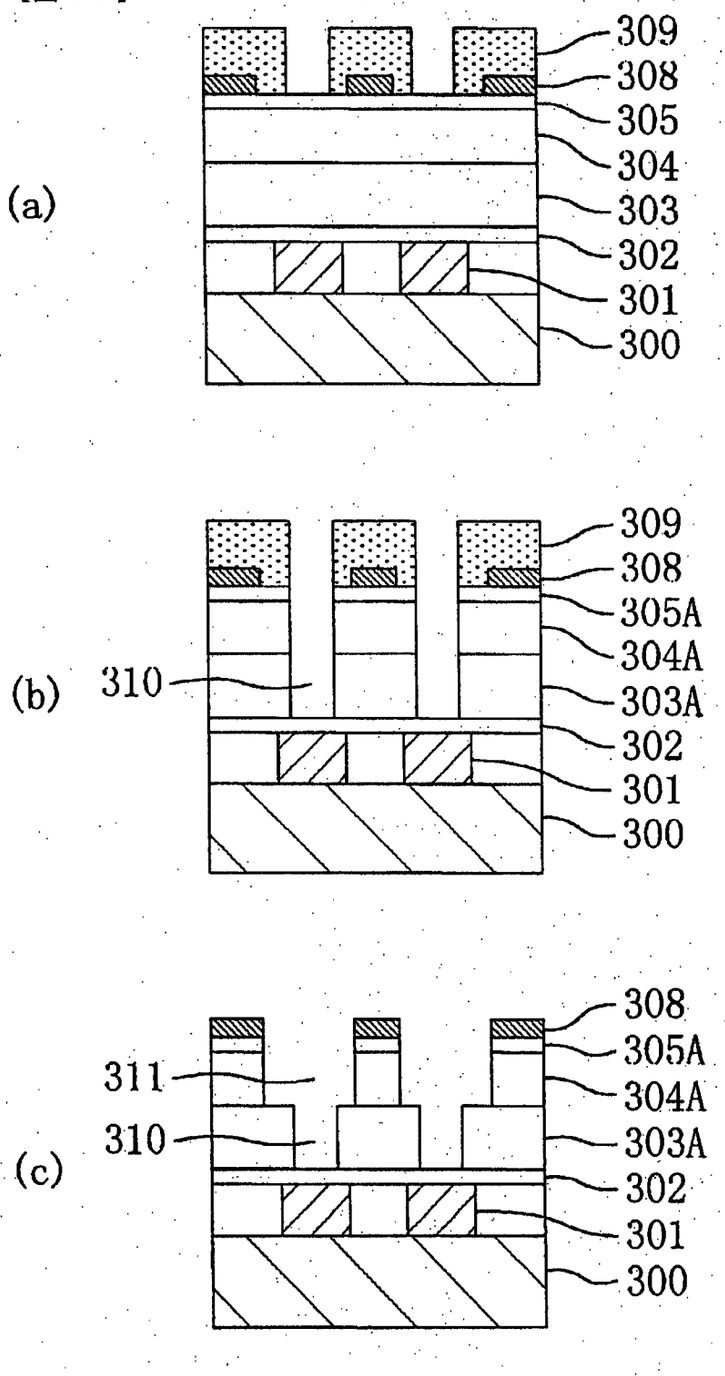
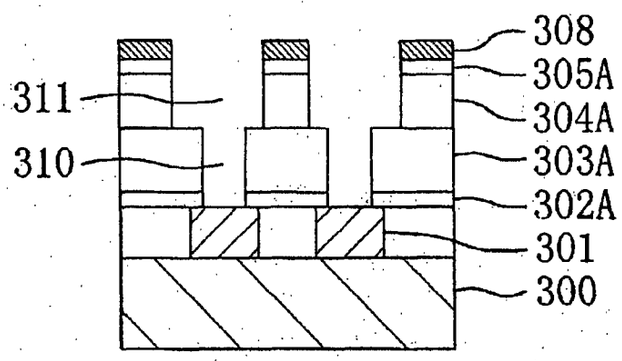
【図１３】

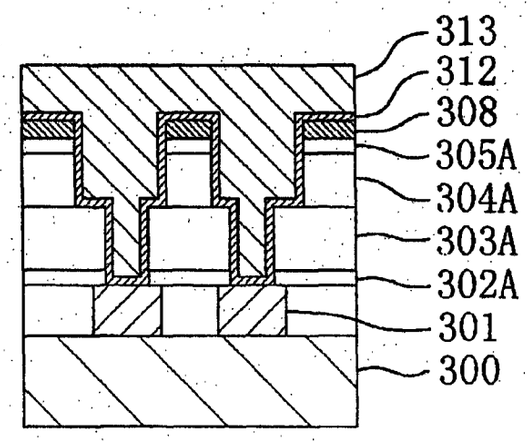

(a)
309
308
305
304
303
302
301
300
(b)
310
309
308
305A
304A
303A
302
301
300
(c)
311
310
308
305A
304A
303A
302
301
300

【図１４】

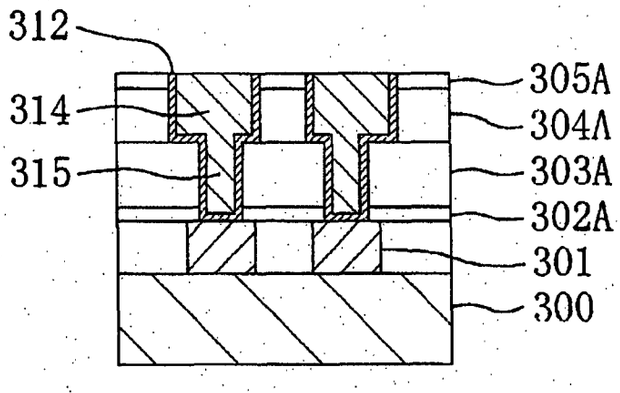
(a)


308
305A
311
304A
310
303A
302A
301
300

(b)

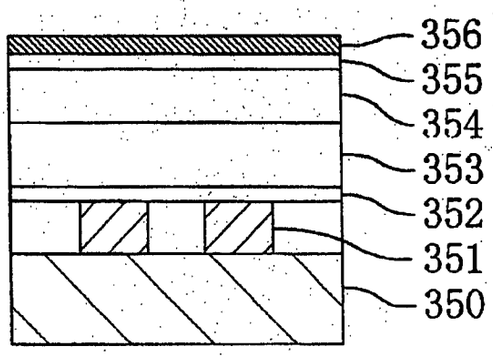

313
312
308
305A
304A
303A
302A
301
300

(c)

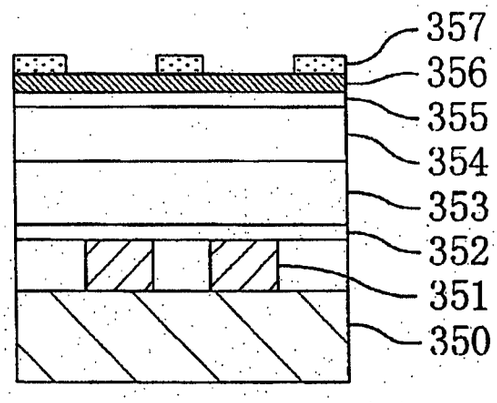

312
305A
314
304A
315
303A
302A
301
300

【図１５】

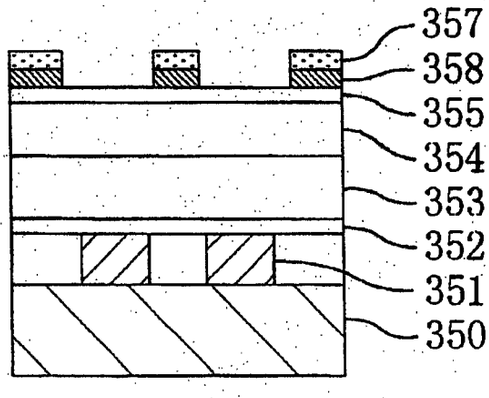
(a)


356
355
354
353
352
351
350

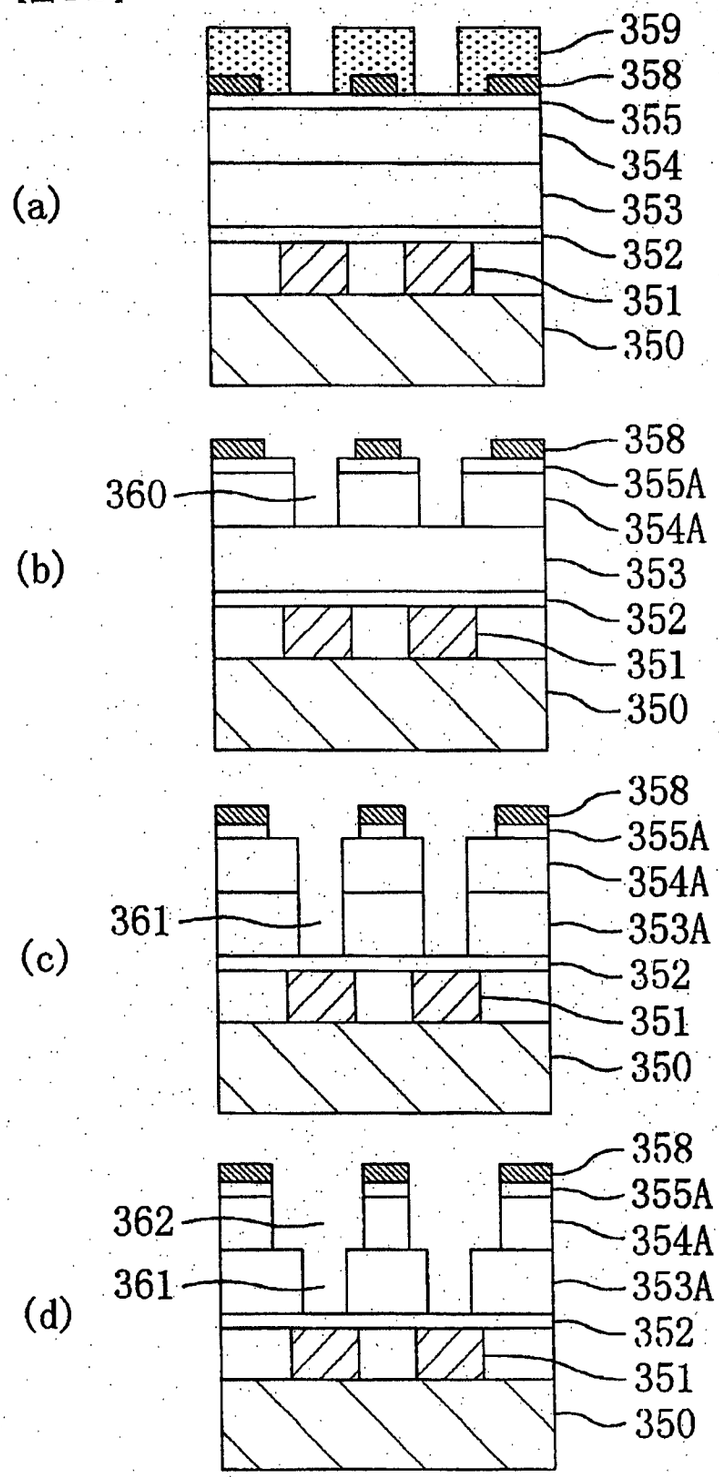
(b)


357
356
355
354
353
352
351
350

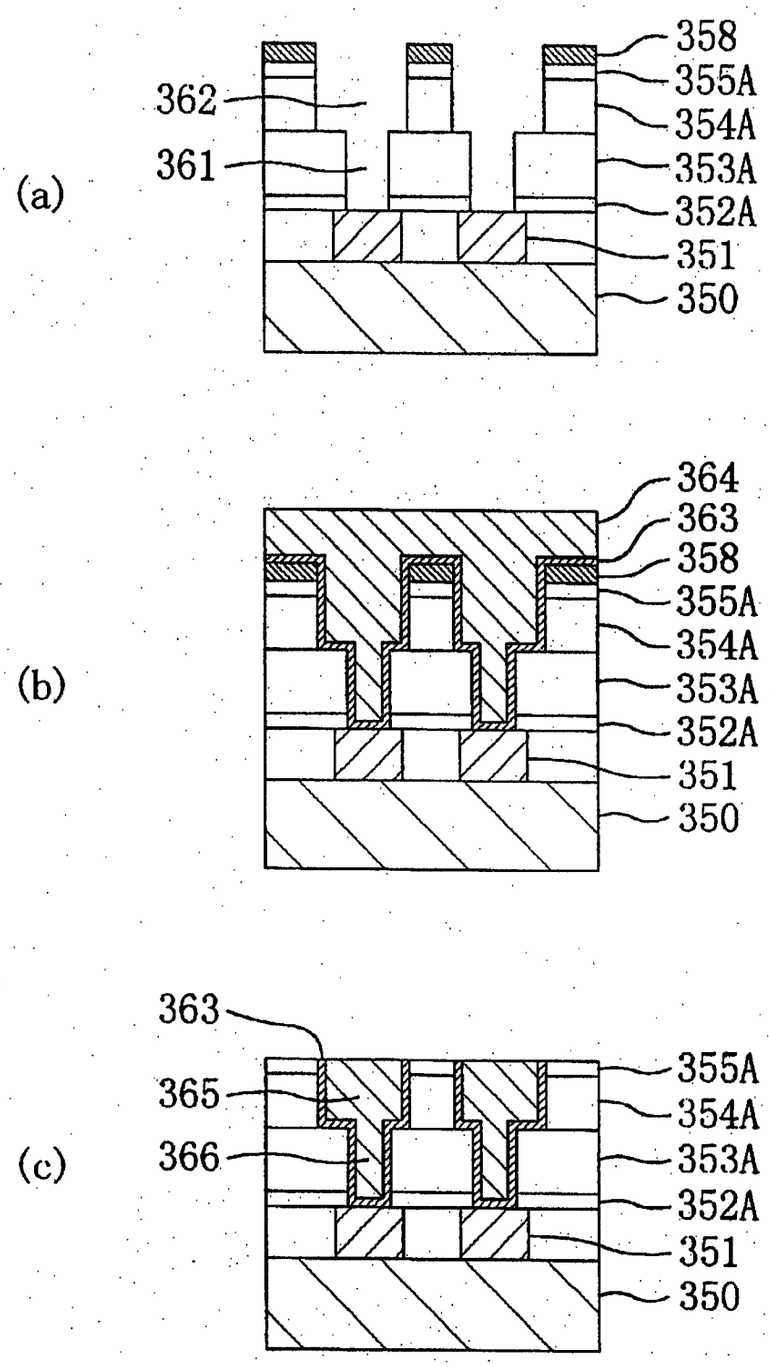
(c)


357
358
355
354
353
352
351
350

【図１６】

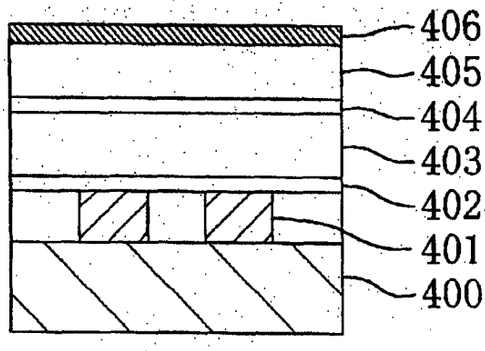

(a)
359
358
355
354
353
352
351
350
(b)
360
358
355A
354A
353
352
351
350
(c)
361
358
355A
354A
353A
352
351
350
(d)
362
361
358
355A
354A
353A
352
351
350

【図１７】


(a)
362
361
358
355A
354A
353A
352A
351
350
(b)
364
363
358
355A
354A
353A
352A
351
350
(c)
363
365
366
355A
354A
353A
352A
351
350

【図１８】

(a)


406
405
404
403
402
401
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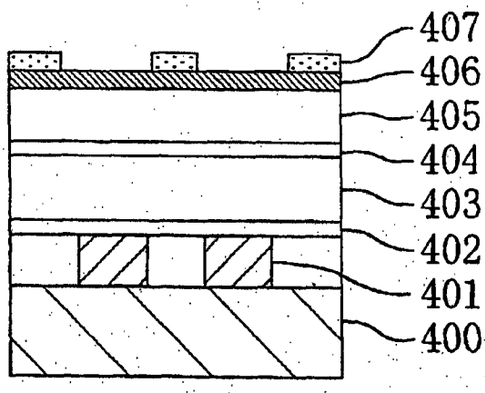
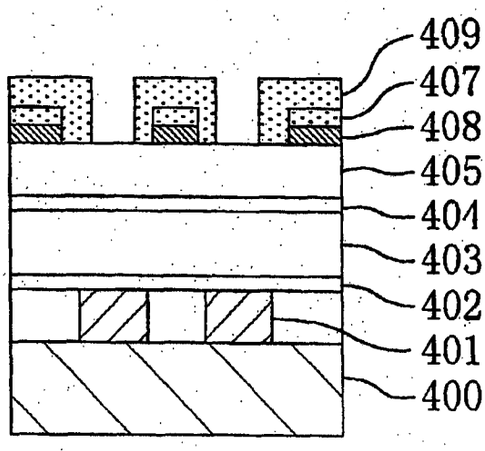
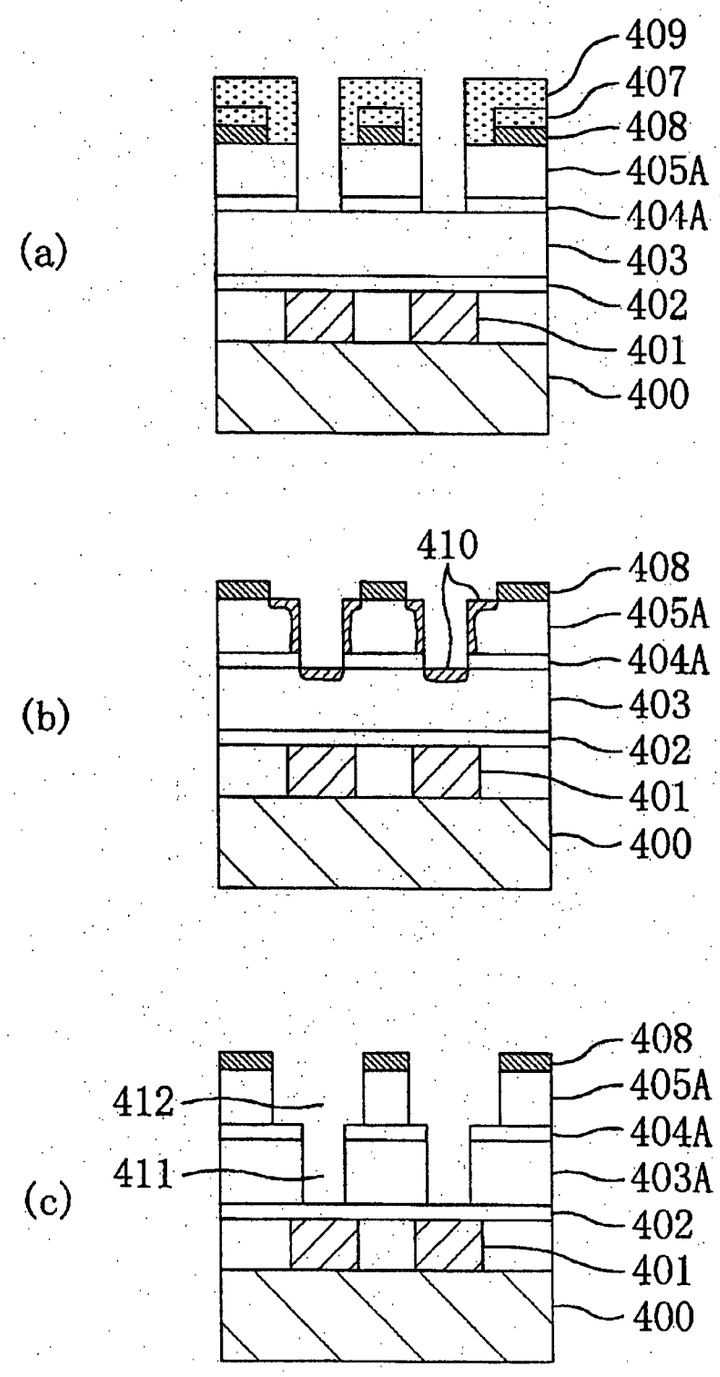
(b)


407
406
405
404
403
402
401
400

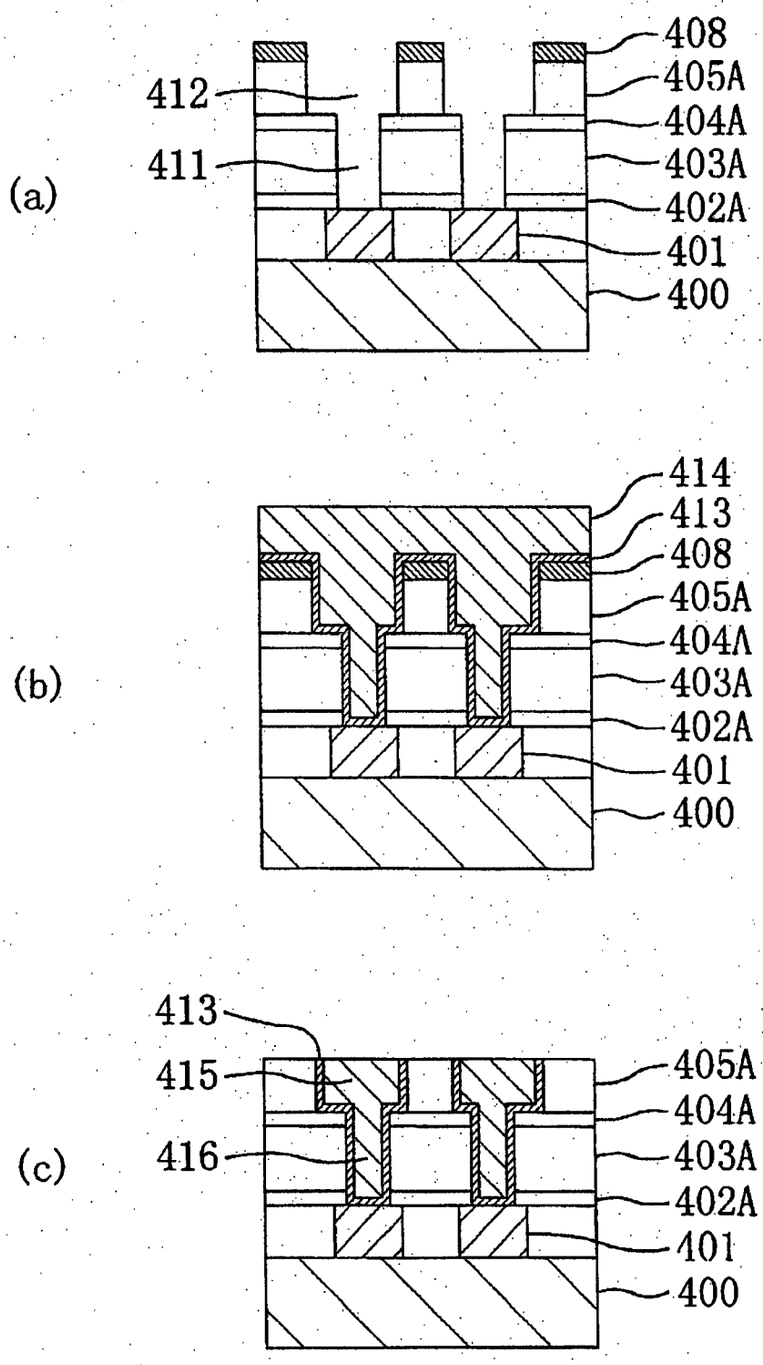
(c)


409
407
408
405
404
403
402
401
400

【図１９】


(a)
409
407
408
405A
404A
403
402
401
400
(b)
410
408
405A
404A
403
402
401
400
(c)
412
411
408
405A
404A
403A
402
401
400

【図２０】


(a)
412
411
408
405A
404A
403A
402A
401
400
(b)
414
413
408
405A
404A
403A
402A
401
400
(c)
413
415
416
405A
404A
403A
402A
401
400

【書類名】　　要約書

【要約】

【課題】　通常のレジストプロセスを採用して、比誘電率が低い層間絶縁膜を形成できるようにする。

【解決手段】　半導体基板１００上の第１の金属配線１０１の上に、シリコン窒化膜１０２、第１の有機膜１０３、有機含有シリコン酸化膜１０４、第２の有機膜１０５及び窒化チタン膜１０６を順次堆積した後、窒化チタン膜１０６の上に形成された第１のレジストパターン１０７をマスクとして窒化チタン膜１０６に対してエッチングを行なってマスクパターン１０８を形成し、その後、第２の有機膜１０５の上に第２のレジストパターン１０９を形成する。第２の有機膜１０５に対して第２のレジストマスク１０９をマスクとしてエッチングを行なって、第２の有機膜１０５をパターン化すると共に第１及び第２のレジストパターン１０７、１０９を除去する。第２の有機膜１０５に対してマスクパターン１０８をマスクとしてエッチングして配線溝を形成すると共に、第１の有機膜１０３に対してパターン化された有機含有シリコン酸化膜１０４をマスクとしてエッチングしてコンタクトホールを形成する。

【選択図】　　図１

【書類名】　職権訂正データ
【訂正書類】　特許願

＜認定情報・付加情報＞
【特許出願人】
【識別番号】　000005821
【住所又は居所】　大阪府門真市大字門真１００６番地
【氏名又は名称】　松下電器産業株式会社
【代理人】　申請人
【識別番号】　100077931
【住所又は居所】　大阪府大阪市西区靭本町１丁目４番８号　太平ビル　前田特許事務所
【氏名又は名称】　前田　弘
【選任した代理人】
【識別番号】　100094134
【住所又は居所】　大阪府大阪市西区靭本町１丁目４番８号　太平ビル　前田特許事務所
【氏名又は名称】　小山　廣毅
【選任した代理人】
【識別番号】　100107445
【住所又は居所】　大阪府大阪市西区靭本町１丁目４番８号　太平ビル　前田特許事務所
【氏名又は名称】　小根田　一郎

出　願　人　履　歴　情　報

識別番号　〔０００００５８２１〕

１．変更年月日　１９９０年　８月２８日
［変更理由］　新規登録
住　所　大阪府門真市大字門真１００６番地
氏　名　松下電器産業株式会社

Transaction History Date 1999-08-09
Date information retrieved from USPTO Patent Application Information Retrieval (PAIR) system records at www.uspto.gov

Gp 1763

OIPE 1085 AUG 09 1999 PATENT & TRADEMARK OFFICE

Docket: 0819-0226

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of)
NOBUO AOI)
Serial No. 09/274,114) Group Art Unit: 1763
Filed: March 23, 1999) Examiner: Unassigned
For: METHOD FOR FORMING)
INTERCONNECTION STRUCTURE)

RECEIVED AUG 11 1999 TC 1700 MAIL ROOM

Honorable Assistant Commissioner of Patents
Washington, D.C. 20231
Sir:

Transmitted herewith is an Information Disclosure Statement in the above-identified application.

[X] In the event applicant(s) has overlooked the need for any petition to effect the entry of the documents submitted herewith, it is respectfully requested that this be treated as such petition and that any necessary fees associated with this petition be charged to Deposit Account No. 19-2380.

[X] In the event applicant(s) has overlooked the need for any petition and fee for extension of time, and such extension is required, applicant(s) requests that this be considered a petition therefor and that such fee be charged to Deposit Account No. 19-2380.

[X] The Commissioner is hereby authorized to charge fees under 37 CFR 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c) and 1.20 (d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment, to Deposit Account No. 19-2380. A duplicate copy of this sheet is attached.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on 8-4-99

Joan M Fisher

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285
Sixbey, Friedman, Leedom & Ferguson, P.C.
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

Docket: 0819-0226

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of	)	
NOBUO AOI	)	
Serial No. 09/274,114	)	Group Art Unit: 1763
Filed: March 23, 1999	)	Examiner: Unassigned
For: METHOD FOR FORMING INTERCONNECTION STRUCTURE	)	

RECEIVED
AUG 11 1999
TC 1700 MAIL ROOM

Honorable Assistant Commissioner of Patents
Washington, D.C. 20231
Sir:

Transmitted herewith is an Information Disclosure Statement in the above-identified application.

[X] In the event applicant(s) has overlooked the need for any petition to effect the entry of the documents submitted herewith, it is respectfully requested that this be treated as such petition and that any necessary fees associated with this petition be charged to Deposit Account No. 19-2380.

[X] In the event applicant(s) has overlooked the need for any petition and fee for extension of time, and such extension is required, applicant(s) requests that this be considered a petition therefor and that such fee be charged to Deposit Account No. 19-2380.

[X] The Commissioner is hereby authorized to charge fees under 37 CFR 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c) and 1.20 (d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment, to Deposit Account No. 19-2380. A duplicate copy of this sheet is attached.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on 8-4-99

Dana M Fisher

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285
Sixbey, Friedman, Leedom & Ferguson, P.C.
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

OIPE
AUG 09 1999
PATENT & TRADEMARK OFFICE

Docket: 0819-0226

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of	)	
NOBUO AOI	)	
Serial No. 09/274,114	)	Group Art Unit: 1763
Filed: 03/23/1999	)	Examiner: Unassigned
For: METHOD FOR FORMING	)	
INTERCONNECTION STRUCTURE	)	
	)	

RECEIVED
AUG 11 1999
TC 1700 MAIL ROOM

INFORMATION DISCLOSURE STATEMENT

Honorable Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, Applicant submits herewith attached Form PTO-1449 listing references known to Applicant and requests that these references be made of record in the above identified application. Copies of the references listed are submitted herewith in accordance with 37 C.F.R. 1.98(a).

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 19-2380. A duplicate copy of this sheet is attached.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

Sixbey, Friedman, Leedom & Ferguson, P.C.
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

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 Docket: 0819-0226

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of	)	
NOBUO AOI	)	
Serial No. 09/274,114	)	Group Art Unit: 1763
Filed: 03/23/1999	)	Examiner: Unassigned
For: METHOD FOR FORMING	)	
INTERCONNECTION STRUCTURE	)	
	)	

RECEIVED
AUG 11 1999
TC 1700 MAIL ROOM

INFORMATION DISCLOSURE STATEMENT

Honorable Assistant Commissioner of Patents

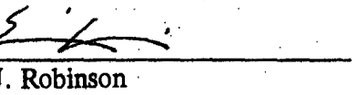
Washington, D.C. 20231

Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, Applicant submits herewith attached Form PTO-1449 listing references known to Applicant and requests that these references be made of record in the above identified application. Copies of the references listed are submitted herewith in accordance with 37 C.F.R. 1.98(a).

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 19-2380. A duplicate copy of this sheet is attached.

Respectfully submitted,



Eric J. Robinson
Reg. No. 38,285

Sixbey, Friedman, Leedom & Ferguson, P.C.
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

CERTIFICATE OF MAILING

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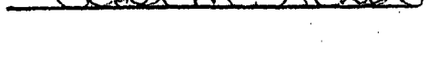

#3

Sheet 1 of 2

Form PTO-1449 (Rev. 8-83) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No.:	Serial No. 09/274114
INFORMATION DISCLOSURE STATEMENT	Applicant:	
(Use several sheets if necessary)	Filing Date:	Group:

OIPE JC85 AUG 0 9 1999 PATENT & TRADEMARK OFFICE

U.S. PATENT DOCUMENTS

Examiner Initial		Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if approp.)
L.J.U.E.		5,651,855	07/29/97	Dennison et al.	438	628	
L.J.U.E.		5,110,712	05/05/92	Kessler et al.	438	623	

OIPE JC85 AUG 0 9 1999 PATENT & TRADEMARK OFFICE

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
L.J.U.E.		0 680 085 A1	11/02/95	EPO	H01L	21/768		
L.J.U.E.		0 425 787 A2	05/08/91	EPO	H01L	21/90		

OTHER DOCUMENTS (Including Author, Title, Relevant Pages, Date, Place of Publication)

L.J.U.E.		European Search Report dated July 1, 1999

Examiner Lynette J. Uz-Ewnini Date Considered 10/6/2000

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (Rev. 8-83)	U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No.:	Serial No.
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		Applicant:	
		Filing Date:	Group:

OIPE JC
AUG 0 9 1999
PATENT & TRADEMARK OFFICE

U.S. PATENT DOCUMENTS

Examiner Initial		Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if approp.)
		5,651,855	07/29/97	Dennison et al.			
		5,110,712	05/05/92	Kessler et al.			

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RECEIVED
AUG 11 1999

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
		0 680 085 A1	11/02/95	EPO				
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Examiner	Date Considered

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File History Content Report

The following content is missing from the original file history record obtained from the United States Patent and Trademark Office. No additional information is available.

Document Date - 1999-08-09

Document Title - List of References cited by applicant and considered by examiner

Page(s) - 2 of 2

This page is not part of the official USPTO record. It has been determined that content identified on this document is missing from the original file history record.

Other Prior Art

According to the information contained in form PTO-1449 or PTO-892, there are one or more other prior art/non-patent literature documents missing from the original file history record obtained from the United States Patent and Trademark Office. Upon your request we will attempt to obtain these documents from alternative resources. Please note that additional charges will apply for this service.

This page is not part of the official USPTO record. It has been determined that content identified on this document is missing from the original file history record.

Transaction History Date 2000-02-09
Date information retrieved from USPTO Patent Application Information Retrieval (PAIR) system records at www.uspto.gov

PE JC46 FEB 0 9 2000 PATENT & TRADEMARK OFFICE

CERTIFICATE OF M[illegible]NG

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on 2-4-00.

Rose M Fichtel

Gau 176
#
2-17-0
Linda B

Docket No. 0819-226

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT Application of	)	
Nobuo AOI	)	
Serial No. 09/274,114	)	Group Art Unit: 1763
Filed: March 23, 1999	)	Examiner: Unassigned
For: METHOD FOR FORMING	)	
INTERCONNECTION STRUCTURE	)	

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, Applicant submits herewith attached Form PTO-1449 listing references known to Applicant and requests that these references be made of record in the above-identified application. Copies of the references are submitted herewith in accordance with 37 C.F.R. 1.98(a).

The Commissioner is hereby authorized to charge fees under 37 CFR 1.17 which may be required now or hereafter, or credit any overpayment, to Deposit Account No. 19-2380. A duplicate copy of this paper is attached.

Respectfully submitted,

Eric J. Robinson
Registration No. 38,285
Sixbey, Friedman, Leedom & Ferguson, P.C.
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110
(703) 883-0370 (Fax)

OIPE JC46
FEB 0 9 2000
PATENT & TRADEMARK OFFICE

Sheet 1 of 1

Form PTO-1449 (Rev. 8-83) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No.: 0819-226	Serial No.: 09/274,114
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	Applicant: Nobuo AOI	
	Filing Date: March 23, 1999	Group: 1763

U.S. PATENT DOCUMENTS

Examiner Initial*		Document Number	Date	Name	Class	Subclass	Filing Date (if appropriate)

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
L.T.N.E.		6-291193	10/18/94	Japan	H01L	21/90	Abst.	
L.T.N.E.		7-153842	06/16/95	Japan	H01L	21/768	Abst.	
L.T.N.E.		9-64034	03/07/97	Japan	H01L	21/3205	Abst.	
L.T.N.E.		9-153545	06/10/97	Japan	H01L	21/768	Abst.	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner: Lynette T. Uz-Eunini

Date Considered: 10/6/2000

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

OIPE JC46
FEB 09 2000
PATENT & TRADEMARK OFFICE

Form PTO-1449 (Rev. 8-83)	U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No.: 0819-226	Serial No.: 09/274,114
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		Applicant: Nobuo AOI	
		Filing Date: March 23, 1999	Group: 1763

U.S. PATENT DOCUMENTS

Examiner Initial*		Document Number	Date	Name	Class	Subclass	Filing Date (if appropriate)

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
		6-291193	10/18/94	Japan			Abst.	
		7-153842	06/16/95	Japan			Abst.	
		9-64034	03/07/97	Japan			Abst.	
		9-153545	06/10/97	Japan			Abst.	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner:	Date Considered:

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Transaction History Date 2000-10-10
Date information retrieved from USPTO Patent Application Information Retrieval (PAIR) system records at www.uspto.gov

Notice of Allowability	Application No. 09/274,114	Applicant(s) AOI
	Examiner Lynette T. Umez-Eronini	Group Art Unit 1765

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☐ This communication is responsive to _____.

☒ The allowed claim(s) is/are *1-15*.

☒ The drawings filed on *Mar 23, 1999* are acceptable.

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☒ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE **THREE MONTHS** FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☐ Applicant MUST submit NEW FORMAL DRAWINGS

☐ because the originally filed drawings were declared by applicant to be informal.

☐ including changes required by the Notice of Draftsperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _____.

☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal lettter addressed to the Official Draftsperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any response to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *3 & 4*

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☐ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

☒ Examiner's Statement of Reasons for Allowance

REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance: Prior art lacks the steps of forming an interconnection structure as recited in the claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is (703) 306-9074.

BENJAMIN L. UTECH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700

ltue

October 6, 2000

Notice of References Cited

Application No.	Applicant(s)		
09/274,114	AOI		
Examiner		Group Art Unit	Page 1 of 1
Lynette T. Umez-Eronini		1765	

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
	A	5,518,963	5/1996	PARK	438	624
	B	5,635,423	6/1997	HUANG ET AL.	438	638
	C	5,702,982	12/1997	LEE ET AL.	438	620
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
	N						
	O						
	P						
	Q						
	R						
	S						
	T						

NON-PATENT DOCUMENTS

		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
	U		
	V		
	W		
	X		

FORM PTO 948 (REV. 01-97) U.S. DEPARTMENT OF COMMERCE-Patent and Trademark Office Application No. 09/274,114

NOTICE OF DRAFTPERSON'S PATENT DRAWING REVIEW

The drawing filied (insert date) 03/23/99 are:

A. ✓ not objected to by the Draftperson under 37 CFR 1.84 or 1.152.

B. _____ objected to by the Draftperson under 37 CFR 1.84 or 1.152 as indicated below. The Examiner will require submission of new, corrected drawings whe necessary. Corrected drawings must be submitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings: Black ink. Color.
   - _____ Color drawing are not acceptable until petition is granted. Fig.(s) _____
   - _____ Pencil and non black ink is not permitted. Fig(s)_____
2. PHOTOGRAPHS. 37 CFR 1.84(b)
   - _____ Photographs are not acceptable until petition is granted,
   - _____ 3 full-tone sets are required. Fig(s)_____
   - _____ Photographs not properly mounted (must brystol board or photographic double-weight paper). Fig(s)_____
   - _____ Poor quailty (half-tone). Fig(s)_____
3. TYPE OF PAPER. 37 CFR 1.84(e)
   - _____ Paper not flexible, strong, white and durable. Fig.(s)_____
   - _____ Erasures, alterations, overwritings, interlineations, folds, copy machine marks not acceptable. (too thin)
   - _____ Mylar, vellum paper is not acceptable (too thin). Fig(s)_____
4. SIZE OF PAPER. 37 CFR 1.84(F): Acceptable sizes:
   - _____ 21.0 cm by 29.7 cm (DIN size A4)
   - _____ 21.6 cm by 27.9 cm (8 1/2 x 11 inches)
   - _____ All drawings sheets not the same size. Sheet(s)_____
5. MARGINS. 37 CFR 18.4(g): Acceptable margins:
   - Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm SIZE: A4 Size
   - Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm SIZE: 8 1/2 x 11
   - _____ Margins not acceptable. Fig(s)_____
   - _____ Top (T) _____ Left (L)
   - _____ Right (R) _____ Bottom (B)
6. VIEWS. CFR 1.84(h)
   REMINDER: Specification may require revision to correspond to drawing changes.
   - _____ Views connected by projection lines or lead lines. Fig.(s)_____

   Partial views. 37 CFR 1.84(h)(2)
   - _____ Brackets needed to show figure as one entity. Fig.(s)_____
   - _____ Views not labeled separately or properly. Fig.(s)_____
   - _____ Enlarged view not labeled separately or properly. Fig.(s)_____
7. SECTIONAL VIEWS. 37 CFR 1.84(h)(3)
   - _____ Hatching not indicated for sectional portions of an object. Fig.(s)_____
   - _____ Sectional designation should be noted with Arabic or Roman numbers. Fig.(s)_____
8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
   - _____ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned, so that the top becomes the right side, except for graphs. Fig.(s)_____
   - _____ Views not on the same plane on drawing sheet. Fig.(s)_____
9. SCALE. 37 CFR 1.84(k)
   - _____ Scale not large enough to show mechansim with crowding when drawing is reduced in size to two-thirds in reproduction. Fig.(s)_____
10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(l)
    - _____ Lines, numbers & letters not uniformly thick and well defined, clean, durable and black (poor line quality). Fig.(s)_____
11. SHADING. 37 CFR 1.84(m)
    - _____ Solid black areas pale. Fig.(s)_____
    - _____ Solid black shading not permitted. Fig.(s)_____
    - _____ Shade lines, pale, rough and blurred. Fig.(s)
12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.48(p)
    - _____ Numbers and reference characters not plain and legible. Fig.(s)_____
    - _____ Figure legends are poor. Fig.(s)_____
    - _____ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(3) Fig.(s)_____
    - _____ Engligh alphabet not used. 37 CFR 1.84(p)(3) Fig.(s)_____
    - _____ Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig.(s)_____
13. LEAD LINES. 37 CFR 1.84(q)
    - _____ Lead lines cross each other. Fig.(s)_____
    - _____ Lead lines missing. Fig.(s)_____
14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.48(t)
    - _____ Sheets not numbered consecutively, and in Ababic numerals beginning with number 1. Fig.(s)_____
15. NUMBERING OF VIEWS. 37 CFR 1.84(u)
    - _____ Views not numbered consecutively, and in Abrabic numerals, beginning with number 1. Fig.(s)_____
16. CORRECTIONS. 37 CFR 1.84(w)
    - _____ Corrections not made from PTO-948 dated _____
17. DESIGN DRAWINGS. 37 CFR 1.152
    - _____ Surface shading shown not appropriate. Fig.(s)_____
    - _____ Solid black shading not used for color contrast. Fig.(s)_____

COMMENTS

Draftsman: Son Lam
(703)308-0366

REVIEWER _____ DATE 10/06/00 TELEPHONE NO. _____

ATTACHMENT TO PAPER NO. _____

PTO COPY

BEST COPY

UNITED STATE[illegible]EPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

IM61/1010

GERALD J FERGUSON JR
SIXBEY FRIEDMAN LEEDOM & FERGUSON
8180 GREENSBORO DRIVE
SUITE 800
MCLEAN VA 22102

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT		DATE MAILED
09/274,114	03/23/99	015	UMEZ ERONINI, L	1765	10/10/00

First Named Applicant		
AOI,	35 USC 154(b) term ext. =	0 Days.

TITLE OF INVENTION: METHOD FOR FORMING INTERCONNECTION STRUCTURE

ATTY'S DOCKET NO.	CLASS/SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
1 0819-226	438-700.000	T53	UTILITY	NO	$1240.00	01/10/01

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or

B. If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

A. Pay FEE DUE shown above, or

B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B-Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY

PTOL-85 (REV. 10-98) Approved for use through 08/30/99. (0651-0033)

U.S. GPO: 1998-437-839/60023

Transaction History Date 2001-01-09
Date information retrieved from USPTO Patent Application Information Retrieval (PAIR) system records at www.uspto.gov

BEST COPY

PART B—ISSUE FEE TRANSMITTAL

Mail to: Box ISSUE FEE
Assistant Commissioner for Patents
Washington, D.C. 20231

...ed for transmitting the ISSUE FEE. Blocks 1 through ... ...l further correspondence including the Issue Fee Receipt, the ... ...on of maintenance fees will be mailed to the current correspondence address as ... ...corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

Note: The certificate of mailing below ... for domestic mailings of the Issue Fee Transmittal. ... cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

IM61/1010

GERALD J FERGUSON JR
SIXBEY FRIEDMAN LEEDOM & FERGUSON
8180 GREENSBORO DRIVE
SUITE 800
MCLEAN VA 22102

Certificate of Mailing

I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

Rose M. Fichtel (Depositor's name)
Rose M Fichtel (Signature)
January 8, 2001 (Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT		DATE MAILED
09/274,114	03/23/99	015	UMEZ ERONINI, L	1765	10/10/00
First Named Applicant AOI,			35 USC 154(b) term ext. =	0 Days.	

TITLE OF INVENTION METHOD FOR FORMING INTERCONNECTION STRUCTURE

01/16/2001 EEKUBAY2 00000201 09274114
01 FC:142 1240.00 OP

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
1 0819-226	438-700.000	T53	UTILITY	NO	$1240.00	01/10/01

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Eric J. Robinson
2 Nixon Peabody LLP
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE
Matsushita Electric Industrial Co., Ltd.
(B) RESIDENCE: (CITY & STATE OR COUNTRY)
Osaka, Japan

Please check the appropriate assignee category indicated below (will not be printed on the patent)
☐ Individual ☒ corporation or other private group entity ☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):
☒ Issue Fee
☒ Advance Order - # of Copies 10

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☒ Advance Order - # of Copies

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature) (Date)
Reg. No. 38,285

NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

01/11/2001 EEKUBAY2 00000030 09274114
~~01 FC:141~~ ~~1240.00 OP~~
02 FC:561 30.00 OP

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Adjustment date: 01/16/2001 EEKUBAY2
01/11/2001 EEKUBAY2 00000030 09274114
01 FC:141 -1240.00 OP

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PTOL-85B (REV.10-98) Approved for use through 06/30/99. OMB 0651-0033 Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

File History Content Report

The following content is missing from the original file history record obtained from the United States Patent and Trademark Office. No additional information is available.

Document Date - 2001-03-06

Document Title - USPTO Grant

This page is not part of the official USPTO record. It has been determined that content identified on this document is missing from the original file history record.

(staple to front of application) USPTO

1700 INTERNAL TRANSFER REQUEST FOR S.N. 09/274,114

DATE: 10/5/00	FROM: ANITA ALANKO (print name)
FORWARD TO:	REASON(S):
A. Art Unit: 1765	A. You had Parent ☐ (check box)
B. Class: 438	B. See Spec. page(s) _____
C Subclass: 689+	C. See Claims _____

REASONS forming interconnect for semicond.

DATE: _____	FROM: _____ (print name)
FORWARD TO:	REASON(S):
A. Art Unit: _____	A. You had Parent ☐ (check box)
B. Class: _____	B. See Spec. page(s) _____
C Subclass: _____	C. See Claims _____

REASONS

DATE: _____	FROM: _____ (print name)
FORWARD TO:	REASON(S):
1700 CLASSIFICATION UNIT	A. You had Parent ☐ (check box)
[redacted]	B. See Spec. pages(s) _____
	C. See Claims _____

REASONS

DISPOSITION BY 1700 CLASSIFICATION UNIT

DATE: _____	CLASSIFIER: _____
FORWARD TO:	REASON(S):
A. Art Unit: _____	A. You had Parent ☐ (check box)
B. Class: _____	B. See Spec. page(s) _____
C Subclass: _____	C. See Claims _____

REASONS

BEST COPY

PATENT APPLICATION FEE DETERMINATION RECORD Effective November 10, 1998	Application or Docket Number

CLAIMS AS FILED - PART I

	(Column 1) NUMBER FILED		(Column 2) NUMBER EXTRA	SMALL ENTITY RATE	SMALL ENTITY FEE		OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY FEE
FOR						OR		
BASIC FEE					380.00	OR		760.00
TOTAL CLAIMS	15	minus 20=	*	X$ 9=		OR	X$18=	
INDEPENDENT CLAIMS	4	minus 3 =	* 1	X39=		OR	X78=	78
MULTIPLE DEPENDENT CLAIM PRESENT				+130=		OR	+260=	
				TOTAL		OR	TOTAL	838

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE		OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
Total	*	Minus	**	=	X$ 9=		OR	X$18=	
Independent	*	Minus	***	=	X39=		OR	X78=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+130=		OR	+260=	
					TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE		OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
Total	*	Minus	**	=	X$ 9=		OR	X$18=	
Independent	*	Minus	***	=	X39=		OR	X78=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+130=		OR	+260=	
					TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE		OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
Total	*	Minus	**	=	X$ 9=		OR	X$18=	
Independent	*	Minus	***	=	X39=		OR	X78=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+130=		OR	+260=	
					TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875
(Rev. 11/98)

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
☆ U.S. GPO:1998-454-473/80301

Thomson Innovation Patent Export, 2015-05-12 12:57:54 -0400

Table of Contents

1. US6197696B1 Method for forming interconnection structure

Family 1/1

13 record(s) per family, collapsed by 7 record(s)

Record 1/7 JP03062491B2 The formation method of a wiring structure

Publication Number:

JP03062491B2 20000710

JP2000003913A 20000107

Title:

The formation method of a wiring structure

Title - DWPI:

Priority Number:

JP199879371A

Priority Date:

1998-03-26

Application Number:

JP199975519A

Application Date:

1999-03-19

Publication Date:

2000-07-10

IPC Class Table:

IPC	Section	Class	Subclass	Class Group	Subgroup
H01L00213205	H	H01	H01L	H01L0021	H01L00213205
H01L0021312	H	H01	H01L	H01L0021	H01L0021312
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522

IPC Class Table - DWPI:

Assignee/Applicant:

JP F Terms:

| 5F033HH07 | 5F033HH08 | 5F033HH11 | 5F033HH12 | 5F033HH13 | 5F033HH14 | 5F033HH15 | 5F033HH19 | 5F033HH33 | 5F033JJ01 | 5F033JJ07 | 5F033JJ08 | 5F033JJ11 | 5F033JJ12 | 5F033JJ13 | 5F033JJ14 | 5F033JJ15 | 5F033JJ19 | 5F033JJ33 | 5F033MM02 | 5F033MM12 | 5F033MM13 | 5F033NN06 | 5F033NN07 | 5F033PP06 | 5F033PP15 | 5F033PP26 | 5F033QQ08 | 5F033QQ09 | 5F033QQ10 | 5F033QQ11 | 5F033QQ21 | 5F033QQ27 | 5F033QQ28 | 5F033QQ29 | 5F033QQ37 | 5F033QQ48 | 5F033RR04 | 5F033RR06 | 5F033RR09 | 5F033RR21 | 5F033RR25 | 5F033SS01 | 5F033SS02 | 5F033SS03 | 5F033SS15 | 5F033TT04 | 5F033TT07 | 5F033XX12 | 5F033XX15 | 5F033XX24 | 5F058AA10 | 5F058AD02 | 5F058AD04 | 5F058AD05 | 5F058AD09 | 5F058AD11 | 5F058AF02 | 5F058AF04 | 5F058AH01 | 5F058AH02 | 5F058BA20 | 5F058BD02 | 5F058BD10 | 5F058BD19 | 5F058BF07 | 5F058BH20 | 5F058BJ01 | 5F058BJ02

JP FI Codes:

| H01L0021312-N | H01L002188-K | H01L002190-S

Assignee - Original:

Any CPC Table:

ECLA:

Abstract:

Language of Publication:

JA

INPADOC Legal Status Table:

Gazette Date	Code	INPADOC Legal Status Impact
2015-03-17	R250	+
Description: RECEIPT OF ANNUAL FEES JAPANESE INTERMEDIATE CODE: R250		
2014-01-17	R350	-
Description: WRITTEN NOTIFICATION OF REGISTRATION OF TRANSFER JAPANESE INTERMEDIATE CODE: R350		

2014-01-08	S111	-
Description: REQUEST FOR CHANGE OF OWNERSHIP OR PART OF OWNERSHIP JAPANESE INTERMEDIATE CODE: R313113		
2013-11-18	R350	-
Description: WRITTEN NOTIFICATION OF REGISTRATION OF TRANSFER JAPANESE INTERMEDIATE CODE: R350		
2013-11-08	S533	-
Description: WRITTEN REQUEST FOR REGISTRATION OF CHANGE OF NAME JAPANESE INTERMEDIATE CODE: R313533		
2013-04-02	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20140428		
2013-03-28	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20130428		
2012-05-08	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20130428		
2012-04-05	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20120428		
2011-04-05	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20120428		
2010-04-06	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20110428		
2009-03-31	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20100428		
2008-04-22	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20090428		
2008-03-27	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20080428		

Post-Issuance (US):

Reassignment (US) Table:

Maintenance Status (US):

Litigation (US):

Opposition (EP):

License (EP):

EPO Procedural Status:

Front Page Drawing:

Record 2/7 JP2000294643A METHOD FOR FORMATION OF WIRING STRUCTURE | The formation method of a wiring structure

Publication Number:
JP2000294643A 20001020
JP03078811B1 20000821

Title:
METHOD FOR FORMATION OF WIRING STRUCTURE | The formation method of a wiring structure

Title - DWPI:
Interconnection structure for a semiconductor integrated circuit

Priority Number:
JP199879371A

Priority Date:
1998-03-26

Application Number:
JP200066163A

Application Date:
1999-03-19

Publication Date:
2000-10-20

IPC Class Table:

IPC	Section	Class	Subclass	Class Group	Subgroup
H01L00213205	H	H01	H01L	H01L0021	H01L00213205
H01L0021302	H	H01	H01L	H01L0021	H01L0021302
H01L00213065	H	H01	H01L	H01L0021	H01L00213065
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522

IPC Class Table - DWPI:

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
H01L0021302	H	H01	H01L	H01L0021	H01L0021302
H01L00213065	H	H01	H01L	H01L0021	H01L00213065
H01L0021312	H	H01	H01L	H01L0021	H01L0021312
H01L00213205	H	H01	H01L	H01L0021	H01L00213205

H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522
H01L0021311	H	H01	H01L	H01L0021	H01L0021311

Assignee/Applicant:
MATSUSHITA ELECTRIC IND CO LTD
JP F Terms:
| 5F004DB00 | 5F004DB03 | 5F004DB23 | 5F004DB25 | 5F004EA03 | 5F004EA06 | 5F004EA07 | 5F004EB01 | 5F004EB03 | 5F033HH08 | 5F033HH09 | 5F033HH11 | 5F033HH12 | 5F033HH13 | 5F033HH14 | 5F033HH15 | 5F033HH19 | 5F033HH33 | 5F033JJ08 | 5F033JJ09 | 5F033JJ11 | 5F033JJ12 | 5F033JJ13 | 5F033JJ14 | 5F033JJ15 | 5F033JJ19 | 5F033JJ33 | 5F033KK08 | 5F033KK09 | 5F033KK11 | 5F033KK12 | 5F033KK13 | 5F033KK14 | 5F033KK15 | 5F033KK19 | 5F033KK33 | 5F033MM02 | 5F033NN06 | 5F033PP06 | 5F033PP15 | 5F033PP26 | 5F033QQ10 | 5F033QQ11 | 5F033QQ12 | 5F033QQ21 | 5F033QQ24 | 5F033QQ25 | 5F033QQ27 | 5F033QQ28 | 5F033QQ35 | 5F033QQ37 | 5F033QQ48 | 5F033RR06 | 5F033RR09 | 5F033RR12 | 5F033RR21 | 5F033RR25 | 5F033RR26 | 5F033SS03 | 5F033SS11 | 5F033SS15 | 5F033SS22 | 5F033TT04 | 5F033TT07 | 5F033XX24
JP FI Codes:
| H01L0021302-105A | H01L0021302-301N | H01L0021302-301S | H01L0021302-J | H01L002188-B | H01L002190-A | H01L002190-B | H01L002190-S
Assignee - Original:
MATSUSHITA ELECTRIC IND CO LTD
Any CPC Table:

ECLA:

Abstract:

PROBLEM TO BE SOLVED: To obtain a method for formation of wiring structure by which an interlayer insulating film having a low specific inductive capacity can be formed by adopting an ordinary resist process.

SOLUTION: In the method for formation of wiring structure, a first organic film 603, a silicon oxide film 604, and a second organic film 605 are sequentially deposited on a semiconductor substrate 600, and then, a mask pattern 608 is formed on the second organic film 605. Then the organic film 605 is patterned by etching the film 605 by using a second resist pattern 609 and the mask pattern 608 as a mask and, at the same time, the second resist pattern 609 is removed. In addition, the silicon oxide film 604 is patterned by etching the film 604 by using the patterned second organic film 605A as a mask. Thereafter, a wiring groove is formed in the second organic film 605A by etching the film 605A by using the mask pattern 608 as a mask and the first organic film 603 by using the silicon oxide film 604 as a mask and, at the same time, a contact hole is formed in the first organic film 603.

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SUBJECT of the Invention

A normal resist process is employ|adopted and it enables it to form an interlayer insulation film with a low dielectric constant.

PROBLEM to be solved

After depositing the 1st organic membrane 603, the silicon oxide film 604, and the 2nd organic membrane 605 one by one on the semiconductor substrate 600, the mask pattern 608 is formed on the 2nd organic membrane 605.
It etches with respect to organic insulating film 605 by setting the 2nd resist pattern 609 and the mask pattern 608 as a mask, and while patternizing the 2nd organic membrane 605, the 2nd resist pattern 609 is removed.
It etches by setting as a mask 2nd organic membrane 605A patternized with respect to the silicon oxide film 604, and the silicon oxide film 604 is patternized.
While etching by setting the mask pattern 608 as a mask with respect to the 2nd organic membrane 605A,
A contact hole is formed in the 1st organic membrane 603, while etching by setting a silicon oxide film as a mask with respect to the 1st organic membrane 603 and forming a wiring groove|channel in the 2nd organic membrane 605A.
[MAT_IMAGE 000002]

PROBLEM TO BE SOLVED: To obtain a method for formation of wiring structure by which an interlayer insulating film having a low specific inductive capacity can be formed by adopting an ordinary resist process. SOLUTION: In the method for formation of wiring structure, a first organic film 603, a silicon oxide film 604, and a second organic film 605 are sequentially deposited on a semiconductor substrate 600, and then, a mask pattern 608 is formed on the second organic film 605. Then the organic film 605 is patterned by etching the film 605 by using a second resist pattern 609 and the mask pattern 608 as a mask and, at the same time, the second resist pattern 609 is removed. In addition, the silicon oxide film 604 is patterned by etching the film 604 by using the patterned second organic film 605A as a mask. Thereafter, a wiring groove is formed in the second organic film 605A by etching the film 605A by using the mask pattern 608 as a mask and the first organic film 603 by using the silicon oxide film 604 as a mask and, at the same time, a contact hole is formed in the first organic film 603.

Language of Publication:

JA

INPADOC Legal Status Table:

Gazette Date	Code	INPADOC Legal Status Impact
2014-01-17	R350	-
Description: WRITTEN NOTIFICATION OF REGISTRATION OF TRANSFER JAPANESE INTERMEDIATE CODE: R350		
2014-01-08	S111	-
Description: REQUEST FOR CHANGE OF OWNERSHIP OR PART OF OWNERSHIP JAPANESE INTERMEDIATE CODE:		

R313113		
2013-11-18	R350	-
Description: WRITTEN NOTIFICATION OF REGISTRATION OF TRANSFER JAPANESE INTERMEDIATE CODE: R350		
2013-11-08	S533	-
Description: WRITTEN REQUEST FOR REGISTRATION OF CHANGE OF NAME JAPANESE INTERMEDIATE CODE: R313533		
2012-06-05	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20130616		
2012-05-31	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20120616		
2011-05-31	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20120616		
2010-06-01	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20110616		
2010-05-27	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20100616		
2009-06-02	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20100616		
2008-06-10	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20090616		
2008-06-05	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20080616		

Post-Issuance (US):

Reassignment (US) Table:

Maintenance Status (US):

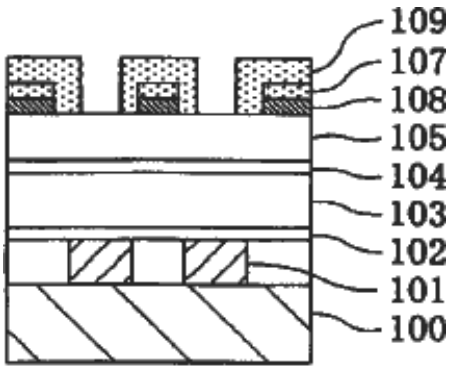
Litigation (US):

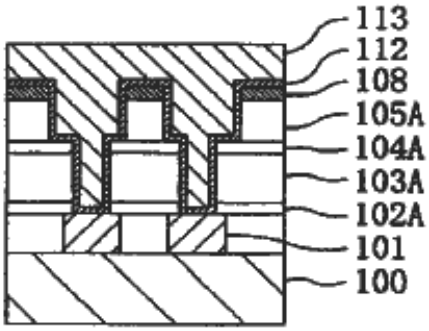
Opposition (EP):

License (EP):

EPO Procedural Status:

Front Page Drawing:





Record 3/7 JP2000294644A METHOD FOR FORMATION OF WIRING STRUCTURE | The formation method of a wiring structure

Publication Number:
JP2000294644A 20001020
JP03078812B1 20000821

Title:
METHOD FOR FORMATION OF WIRING STRUCTURE | The formation method of a wiring structure

Title - DWPI:
Interconnection structure for a semiconductor integrated circuit

Priority Number:
JP199879371A

Priority Date:
1998-03-26

Application Number:
JP200066179A

Application Date:
1999-03-19

Publication Date:
2000-10-20

IPC Class Table:

IPC	Section	Class	Subclass	Class Group	Subgroup
H01L00213205	H	H01	H01L	H01L0021	H01L00213205
H01L0021302	H	H01	H01L	H01L0021	H01L0021302
H01L00213065	H	H01	H01L	H01L0021	H01L00213065
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522

IPC Class Table - DWPI:

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
H01L0021302	H	H01	H01L	H01L0021	H01L0021302
H01L00213065	H	H01	H01L	H01L0021	H01L00213065
H01L0021312	H	H01	H01L	H01L0021	H01L0021312
H01L00213205	H	H01	H01L	H01L0021	H01L00213205

H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522
H01L0021311	H	H01	H01L	H01L0021	H01L0021311

Assignee/Applicant:
MATSUSHITA ELECTRIC IND CO LTD
JP F Terms:
| 5F004AA08 | 5F004AA16 | 5F004DA00 | 5F004DB00 | 5F004DB03 | 5F004DB07 | 5F004DB23 | 5F004DB25 | 5F004EA03 | 5F004EB01 | 5F004EB03 | 5F004EB08 | 5F033HH08 | 5F033HH09 | 5F033HH11 | 5F033HH12 | 5F033HH13 | 5F033HH14 | 5F033HH15 | 5F033HH19 | 5F033HH33 | 5F033JJ08 | 5F033JJ09 | 5F033JJ11 | 5F033JJ12 | 5F033JJ13 | 5F033JJ14 | 5F033JJ15 | 5F033JJ19 | 5F033JJ33 | 5F033KK08 | 5F033KK09 | 5F033KK11 | 5F033KK12 | 5F033KK13 | 5F033KK14 | 5F033KK15 | 5F033KK19 | 5F033KK33 | 5F033MM02 | 5F033NN06 | 5F033PP06 | 5F033PP15 | 5F033PP26 | 5F033QQ10 | 5F033QQ11 | 5F033QQ12 | 5F033QQ21 | 5F033QQ25 | 5F033QQ27 | 5F033QQ28 | 5F033QQ35 | 5F033QQ37 | 5F033QQ48 | 5F033RR06 | 5F033RR09 | 5F033RR12 | 5F033RR21 | 5F033RR25 | 5F033RR26 | 5F033SS03 | 5F033SS11 | 5F033SS15 | 5F033SS22 | 5F033TT04 | 5F033TT07 | 5F033XX24
JP FI Codes:
| H01L0021302-105A | H01L0021302-301N | H01L0021302-301S | H01L0021302-301Z | H01L0021302-J | H01L002188-B | H01L002190-A | H01L002190-B | H01L002190-S
Assignee - Original:
MATSUSHITA ELECTRIC IND CO LTD
Any CPC Table:

ECLA:

Abstract:

PROBLEM TO BE SOLVED: To provide a method for formation of wiring structure by which an interlayer insulating film having a low specific inductive capacity can be formed by adopting an ordinary resist process.

SOLUTION: In the method for formation of wiring structure, a first organic matter-bearing silicon oxide film 303, an SOG film 304 having a low specific inductive capacity, and a second organic matter-containing silicon oxide film 305 are sequentially deposited on a semiconductor substrate 300, and then, a mask pattern 308 is formed on the silicon oxide film 305. Then contact holes 310 are formed in the silicon oxide film 303 by etching the silicon oxide film 305, SOG film 304, and silicon oxide film 303 by using a second resist pattern 309 as a mask. After the pattern 309 is removed thereafter, wiring grooves 311 are formed in the SOG film 304 by etching the silicon oxide film 305 and SOG film 304 by using a mask pattern 308 as a mask.

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SUBJECT of the Invention

A normal resist process is employ|adopted and it enables it to form an interlayer insulation film with a low dielectric constant.

PROBLEM to be solved

On the semiconductor substrate 300, the 1st organic containing silicon oxide film 303, low dielectric constant SOG film 304, and the 2nd organic containing silicon oxide film 305 were deposited one by one,
Then, the mask pattern 308 is formed on the 2nd organic containing silicon oxide film 305.
It etches by setting the 2nd resist pattern 309 as a mask with respect to the 2nd organic containing silicon oxide film 305, low dielectric constant SOG film 304, and the 1st organic containing silicon oxide film 303, and the contact hole 310 is formed in the 1st organic containing silicon oxide film 303.
The 2nd resist pattern 309 was removed,
Then, it etches by setting the mask pattern 308 as a mask with respect to the 2nd organic containing silicon oxide film 305 and low dielectric constant SOG film 304, and the wiring groove|channel 311 is formed in low dielectric constant SOG film 304.
[MAT_IMAGE 000002]

PROBLEM TO BE SOLVED: To provide a method for formation of wiring structure by which an interlayer insulating film having a low specific inductive capacity can be formed by adopting an ordinary resist process. SOLUTION: In the method for formation of wiring structure, a first organic matter-bearing silicon oxide film 303, an SOG film 304 having a low specific inductive capacity, and a second organic matter-containing silicon oxide film 305 are sequentially deposited on a semiconductor substrate 300, and then, a mask pattern 308 is formed on the silicon oxide film 305. Then contact holes 310 are formed in the silicon oxide film 303 by etching the silicon oxide film 305, SOG film 304, and silicon oxide film 303 by using a second resist pattern 309 as a mask. After the pattern 309 is removed thereafter, wiring grooves 311 are formed in the SOG film 304 by etching the silicon oxide film 305 and SOG film 304 by using a mask pattern 308 as a mask.

Language of Publication:

JA

INPADOC Legal Status Table:

Gazette Date	Code	INPADOC Legal Status Impact
2014-01-17	R350	-
Description: WRITTEN NOTIFICATION OF REGISTRATION OF TRANSFER JAPANESE INTERMEDIATE CODE: R350		
2014-01-08	S111	-
Description: REQUEST FOR CHANGE OF OWNERSHIP OR PART OF OWNERSHIP JAPANESE INTERMEDIATE CODE: R313113		
2013-11-18	R350	-
Description: WRITTEN NOTIFICATION OF REGISTRATION OF TRANSFER JAPANESE INTERMEDIATE CODE: R350		

2013-11-08	S533	-
Description: WRITTEN REQUEST FOR REGISTRATION OF CHANGE OF NAME JAPANESE INTERMEDIATE CODE: R313533		
2012-06-05	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20130616		
2012-05-31	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20120616		
2011-05-31	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20120616		
2010-06-01	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20110616		
2010-05-27	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20100616		
2009-06-02	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20100616		
2008-06-10	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20090616		
2008-06-05	FPAY	+
Description: RENEWAL FEE PAYMENT (PRS DATE IS RENEWAL DATE OF DATABASE) PAYMENT UNTIL: 20080616		

Post-Issuance (US):

Reassignment (US) Table:

Maintenance Status (US):

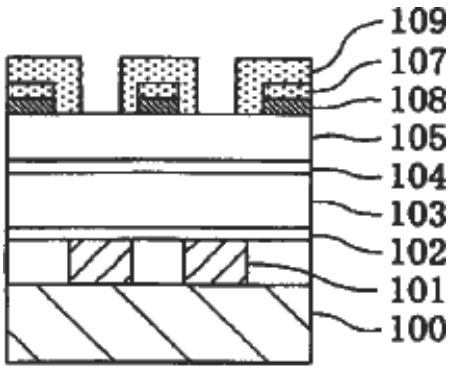
Litigation (US):

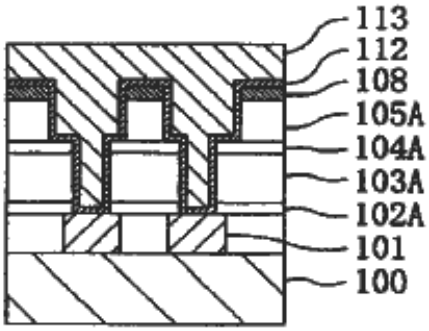
Opposition (EP):

License (EP):

EPO Procedural Status:

Front Page Drawing:





Record 4/7 US6197696B1 Method for forming interconnection structure

Publication Number:
US6197696B1 20010306

Title:
Method for forming interconnection structure
Title - DWPI:
Interconnection structure for a semiconductor integrated circuit
Priority Number:
JP199879371A
Priority Date:
1998-03-26
Application Number:
US1999274114A
Application Date:
1999-03-23
Publication Date:
2001-03-06
IPC Class Table:

IPC	Section	Class	Subclass	Class Group	Subgroup
H01L0021768	H	H01	H01L	H01L0021	H01L0021768

IPC Class Table - DWPI:

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
H01L0021302	H	H01	H01L	H01L0021	H01L0021302
H01L00213065	H	H01	H01L	H01L0021	H01L00213065
H01L0021312	H	H01	H01L	H01L0021	H01L0021312
H01L00213205	H	H01	H01L	H01L0021	H01L00213205
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522
H01L0021311	H	H01	H01L	H01L0021	H01L0021311

Assignee/Applicant:
Matsushita Electric Industrial Co. Ltd.,Osaka,JP
JP F Terms:

JP FI Codes:

Assignee - Original:

Matsushita Electric Industrial Co. Ltd.

Any CPC Table:

Type	Invention	Additional	Version	Office
Current	**H01L 21/76835**	-	20130101	EP
Current	H01L 21/76811		20130101	EP
Current	H01L 21/76813		20130101	EP
Current	H01L 21/76814		20130101	EP
Current	H01L 21/76826		20130101	EP
Current	H01L 21/76829		20130101	EP
Current	H01L 21/76831		20130101	EP
Current	H01L 21/76895		20130101	EP

ECLA:

H01L0021768B12 | H01L0021768B2D6 | H01L0021768B2D8 | H01L0021768B2F | H01L0021768B8P | H01L0021768B10 | H01L0021768B10B | H01L0021768C10

Abstract:

In a method for forming an interconnection structure, first, second and third insulating films and a thin film are sequentially formed over lower-level metal interconnects. Then, the thin film is masked with a first resist pattern and etched to form a mask pattern with openings for interconnects. Next, the third insulating film is masked with a second resist pattern and dry-etched such that the third insulating film and the first and second resist patterns are etched at a high rate and that the second insulating film is etched at a low rate to form openings for contact holes in the third insulating film and remove the first and second resist patterns. Then, the second insulating film is masked with the third insulating film and dry-etched such that the second insulating film is etched at a high rate and that the first and third insulating films are etched at a low rate to form the openings for contact holes in the second insulating film. Then, the third and first insulating films are masked with the mask pattern and the second insulating film, respectively, and dry-etched such that the first and third insulating films are etched at a high rate and that the mask pattern and the second insulating film are etched at a low rate to form wiring grooves and contact holes in the third and first insulating films, respectively. Finally, upper-level metal interconnects and contacts are formed.

Language of Publication:

EN

INPADOC Legal Status Table:

Gazette Date	Code	INPADOC Legal Status Impact
2014-02-03	AS	-
Description: ASSIGNMENT GODO KAISHA IP BRIDGE 1, JAPAN ASSIGNMENT OF ASSIGNORS INTEREST;		

ASSIGNOR:PANASONIC CORPORATION (FORMERLY MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.); REEL/FRAME:032152/0514 2014-01-17		
2012-08-20	FPAY	+
Description: FEE PAYMENT		
2008-08-27	FPAY	+
Description: FEE PAYMENT		
2004-08-04	FPAY	+
Description: FEE PAYMENT		
1999-03-23	AS	-
Description: ASSIGNMENT MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD., JAPAN ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNOR:AOI, NOBUO; REEL/FRAME:009862/0097 1999-03-19		

Post-Issuance (US):

Reassignment (US) Table:

Assignee	Assignor	Date Signed	Reel/Frame	Date
GODO KAISHA IP BRIDGE 1,TOKYO,JP	PANASONIC CORPORATION (FORMERLY MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.)	2014-01-17	032152/0514	2014-02-03
Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
Corresponent: SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVE. NW SUITE 800 WASHINGTON, DC 20037-3213				
MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD.,OSAKA 571-8501,JP	AOI, NOBUO	1999-03-19	009862/0097	1999-03-23
Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
Corresponent: SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, ERIC J. ROBINSON 8180 GREENSBORO DRIVE SUITE 800 MCLEAN, VA 22102				

Maintenance Status (US):

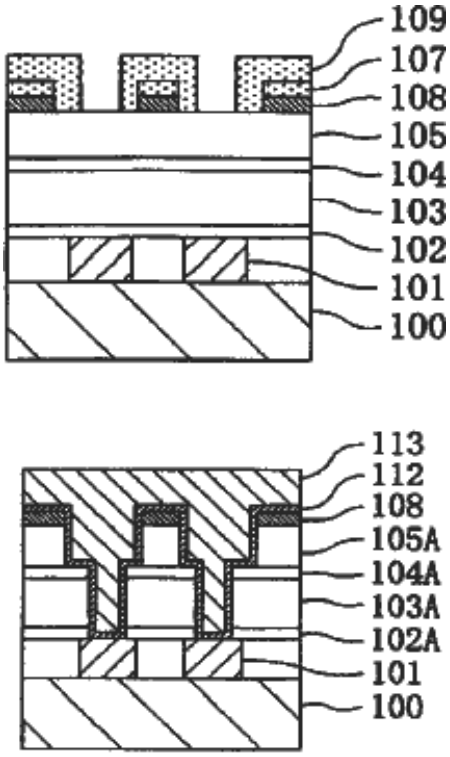
Litigation (US):

Opposition (EP):

License (EP):

EPO Procedural Status:

Front Page Drawing:



Record 5/7 US6287973B2 Method for forming interconnection structure

Publication Number:
US6287973B2 20010911
US20010001739A1 20010524

Title:
Method for forming interconnection structure
Title - DWPI:
Interconnection structure for a semiconductor integrated circuit
Priority Number:
JP199879371A | US1999274114A
Priority Date:
1998-03-26 | 1999-03-23
Application Number:
US2001756242A
Application Date:
2001-01-09
Publication Date:
2001-09-11
IPC Class Table:

IPC	Section	Class	Subclass	Class Group	Subgroup
H01L0021768	H	H01	H01L	H01L0021	H01L0021768

IPC Class Table - DWPI:

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
H01L0021302	H	H01	H01L	H01L0021	H01L0021302
H01L00213065	H	H01	H01L	H01L0021	H01L00213065
H01L0021312	H	H01	H01L	H01L0021	H01L0021312
H01L00213205	H	H01	H01L	H01L0021	H01L00213205
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522
H01L0021311	H	H01	H01L	H01L0021	H01L0021311

Assignee/Applicant:
Matsushita Electric Industrial Co. Ltd.,Osaka,JP
JP F Terms:

JP FI Codes:

Assignee - Original:
Matsushita Electric Industrial Co. Ltd.
Any CPC Table:

Type	Invention	Additional	Version	Office
Current	**H01L 21/76835**	-	20130101	EP
Current	H01L 21/76811		20130101	EP
Current	H01L 21/76813		20130101	EP
Current	H01L 21/76814		20130101	EP
Current	H01L 21/76826		20130101	EP
Current	H01L 21/76829		20130101	EP
Current	H01L 21/76831		20130101	EP
Current	H01L 21/76895		20130101	EP

ECLA:
H01L0021768B12 | H01L0021768B2D6 | H01L0021768B2D8 | H01L0021768B2F | H01L0021768B8P | H01L0021768B10 | H01L0021768B10B | H01L0021768C10
Abstract:

In a method for forming an interconnection structure, first, second and third insulating films and a thin film are sequentially formed over lower-level metal interconnects. Then, the thin film is masked with a first resist pattern and etched to form a mask pattern with openings for interconnects. Next, the third insulating film is masked with a second resist pattern and dry-etched such that the third insulating film and the first and second resist patterns are etched at a high rate and that the second insulating film is etched at a low rate to form openings for contact holes in the third insulating film and remove the first and second resist patterns. Then, the second insulating film is masked with the third insulating film and dry-etched such that the second insulating film is etched at a high rate and that the first and third insulating films are etched at a low rate to form the openings for contact holes in the second insulating film. Then, the third and first insulating films are masked with the mask pattern and the second insulating film, respectively, and dry-etched such that the first and third insulating films are etched at a high rate and that the mask pattern and the second insulating film are etched at a low rate to form wiring grooves and contact holes in the third and first insulating films, respectively. Finally, upper-level metal interconnects and contacts are formed.
Language of Publication:
EN
INPADOC Legal Status Table:

Gazette Date	Code	INPADOC Legal Status Impact
2014-02-03	AS	-

Description: ASSIGNMENT GODO KAISHA IP BRIDGE 1, JAPAN ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNOR:PANASONIC CORPORATION (FORMERLY MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.); REEL/FRAME:032152/0514 2014-01-17		
2013-02-19	FPAY	+
Description: FEE PAYMENT		
2009-02-11	FPAY	+
Description: FEE PAYMENT		
2005-02-17	FPAY	+
Description: FEE PAYMENT		

Post-Issuance (US):

Reassignment (US) Table:

Assignee	Assignor	Date Signed	Reel/Frame	Date
GODO KAISHA IP BRIDGE 1,TOKYO,JP	PANASONIC CORPORATION (FORMERLY MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.)	2014-01-17	032152/0514	2014-02-03
Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
Corresponent: SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVE. NW SUITE 800 WASHINGTON, DC 20037-3213				

Maintenance Status (US):

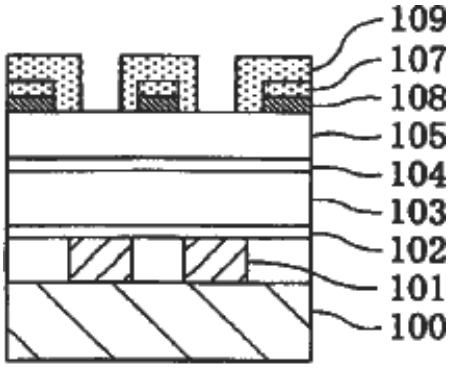
Litigation (US):

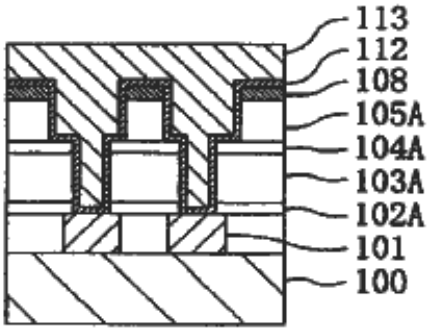
Opposition (EP):

License (EP):

EPO Procedural Status:

Front Page Drawing:


109
107
108
105
104
103
102
101
100


113
112
108
105A
104A
103A
102A
101
100

Record 6/7 EP945900B1 Method for forming interconnection structure | Verfahren zur Herstellung einer Verbindungsstruktur | Méthode de formation d'une structure d'interconnexion

Publication Number:
EP945900B1 20060809
EP945900A1 19990929

Title:
Method for forming interconnection structure | Verfahren zur Herstellung einer Verbindungsstruktur | Méthode de formation d'une structure d'interconnexion
Title - DWPI:
Interconnection structure for a semiconductor integrated circuit
Priority Number:
JP199879371A
Priority Date:
1998-03-26
Application Number:
EP1999105946A
Application Date:
1999-03-24
Publication Date:
2006-08-09
IPC Class Table:

IPC	Section	Class	Subclass	Class Group	Subgroup
H01L0021768	H	H01	H01L	H01L0021	H01L0021768

IPC Class Table - DWPI:

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
H01L0021302	H	H01	H01L	H01L0021	H01L0021302
H01L00213065	H	H01	H01L	H01L0021	H01L00213065
H01L0021312	H	H01	H01L	H01L0021	H01L0021312
H01L00213205	H	H01	H01L	H01L0021	H01L00213205
H01L0021768	H	H01	H01L	H01L0021	H01L0021768
H01L0023522	H	H01	H01L	H01L0023	H01L0023522
H01L0021311	H	H01	H01L	H01L0021	H01L0021311

Assignee/Applicant:

MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD,Kadoma shi, Osaka 571 8501,JP,01855508

JP F Terms:

JP FI Codes:

Assignee - Original:

MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD

Any CPC Table:

Type	Invention	Additional	Version	Office
Current	**H01L 21/76835**	-	20130101	EP
Current	H01L 21/76811		20130101	EP
Current	H01L 21/76813		20130101	EP
Current	H01L 21/76814		20130101	EP
Current	H01L 21/76826		20130101	EP
Current	H01L 21/76829		20130101	EP
Current	H01L 21/76831		20130101	EP
Current	H01L 21/76895		20130101	EP

ECLA:

H01L0021768B12 | H01L0021768B2D6 | H01L0021768B2D8 | H01L0021768B2F | H01L0021768B8P | H01L0021768B10 | H01L0021768B10B | H01L0021768C10

Abstract:

In a method for forming an interconnection structure, first, second and third insulating films and a thin film are sequentially formed over lower-level metal interconnects. Then, the thin film is masked with a first resist pattern and etched to form a mask pattern with openings for interconnects. Next, the third insulating film is masked with a second resist pattern and dry-etched such that the third insulating film and the first and second resist patterns are etched at a high rate and that the second insulating film is etched at a low rate to form openings for contact holes in the third insulating film and remove the first and second resist patterns. Then, the second insulating film masked with the third insulating film is dry-etched such that the second insulating film is etched at a high rate and that the first and third insulating films are etched at a low rate to form the openings for contact holes in the second insulating film. Then, the third and first insulating films masked with the mask pattern and the second insulating film, respectively, are dry-etched such that the first and third insulating films are etched at a high rate and that the mask pattern and the second insulating film are etched at a low rate to form wiring grooves and contact holes in the third and first insulating films, respectively. Finally, upper-level metal interconnects and contacts are formed.

Language of Publication:

EN

INPADOC Legal Status Table:

Gazette Date	Code	INPADOC Legal Status Impact

2015-03-31	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE NL		
2014-08-29	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE DE		
2014-06-30	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE GB		
2014-05-30	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE FR		
2014-04-30	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE NL		
2013-08-30	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE NL		
2013-04-30	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE GB		
2013-04-30	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE FR		
2013-04-30	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE DE		
2012-07-31	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE NL		
2012-07-31	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE DE		
2012-06-29	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE GB		

2012-04-30	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE FR		
2011-07-29	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE GB		
2011-07-29	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE DE		
2011-05-31	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE NL		
2011-05-31	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE FR		
2010-08-31	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE DE		
2010-08-31	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE NL		
2010-06-30	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE GB		
2010-05-31	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE FR		
2009-10-30	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE FR		
2009-08-31	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE DE		
2009-06-30	PGFP	+
Description: POSTGRANT: ANNUAL FEES PAID TO NATIONAL OFFICE GB		

USPTO Maintenance Report

Patent Bibliographic Data				05/12/2015 12:56 PM	
Patent Number:	6197696		Application Number:	09274114	
Issue Date:	03/06/2001		Filing Date:	03/23/1999	
Title:	METHOD FOR FORMING INTERCONNECTION STRUCTURE				
Status:	4th, 8th and 12th year fees paid			Entity:	LARGE
Window Opens:	N/A	Surcharge Date:	N/A	Expiration:	N/A
Fee Amt Due:	Window not open	Surchg Amt Due:	Window not open	Total Amt Due:	Window not open
Fee Code:					
Surcharge Fee Code:					
Most recent events (up to 7):	08/20/2012 07/05/2012 07/05/2012 08/27/2008 08/04/2004 09/12/2001	Payment of Maintenance Fee, 12th Year, Large Entity. Payor Number Assigned. Payer Number De-assigned. Payment of Maintenance Fee, 8th Year, Large Entity. Payment of Maintenance Fee, 4th Year, Large Entity. Payor Number Assigned. --- End of Maintenance History ---			
Address for fee purposes:	PANASONIC PATENT CENTER 20000 Mariner Avenue, Suite 200 Torrance CA 90503				