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United States Patent [19]

Jain et al.

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[54] **METHOD FOR FORMING A DIELECTRIC TANTALUM NITRIDE LAYER AS AN ANTI-REFLECTIVE COATING (ARC)**

[75] Inventors: **Ajay Jain; Kevin Lucas**, both of Austin, Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **632,209**

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[51] Int. Cl.⁶ **G03F 7/00; H01L 21/314**

[52] U.S. Cl. **430/314; 430/311; 430/312; 430/316; 430/317; 438/626; 438/633; 438/634; 438/636; 438/692; 438/694; 438/703; 438/785; 216/18**

[58] **Field of Search** **430/311, 312, 430/314, 316, 317; 156/652.1, 661.11; 437/229, 195; 216/18; 438/598, 626, 634, 636, 637, 638, 618, 703, 692, 694, 126, 133, 355, 389, 785, 633**

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Attorney, Agent, or Firm—Keith E. Witek

[57] **ABSTRACT**

The present invention provides an anti-reflective Ta₃N₅ coating which can be used in a dual damascene structure and for I line or G line lithographies. In addition, the Ta₃N₅ coating may also be used as an etch stop and a barrier layer. A dual damascene structure is formed by depositing a first dielectric layer (16). A dielectric tantalum nitride layer (18) is deposited on top of the first dielectric layer. A second dielectric layer (20) is deposited on the tantalum nitride layer. A dual damascene opening (34) is etched into the dielectric layers by patterning a first opening portion (26) and a second opening portion (32) using photolithography operations. Dielectric tantalum nitride layer (18) serves as an ARC layer during these operations to reduce the amount of reflectance from conductive region (14) to reduce distortion of the photoresist pattern. The use of a dielectric tantalum nitride layer as an ARC is particularly suitable for I line and G line lithography.

27 Claims, 6 Drawing Sheets

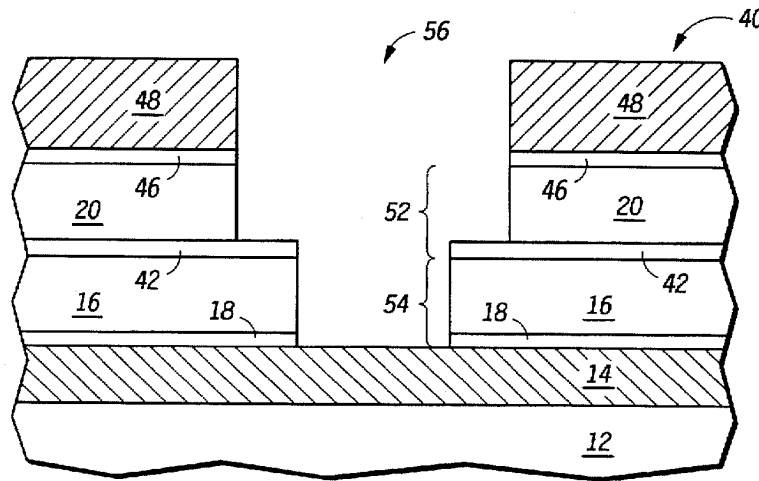


FIG. 1

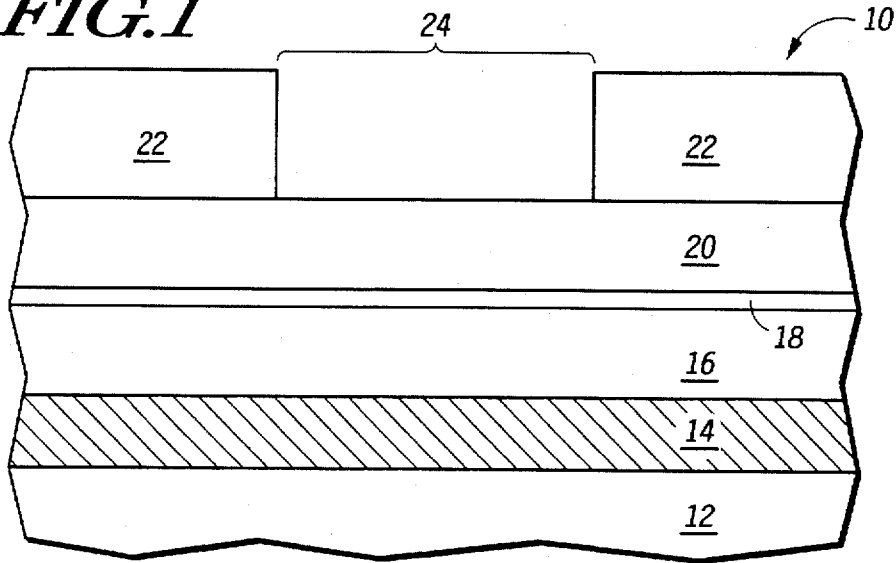


FIG. 2

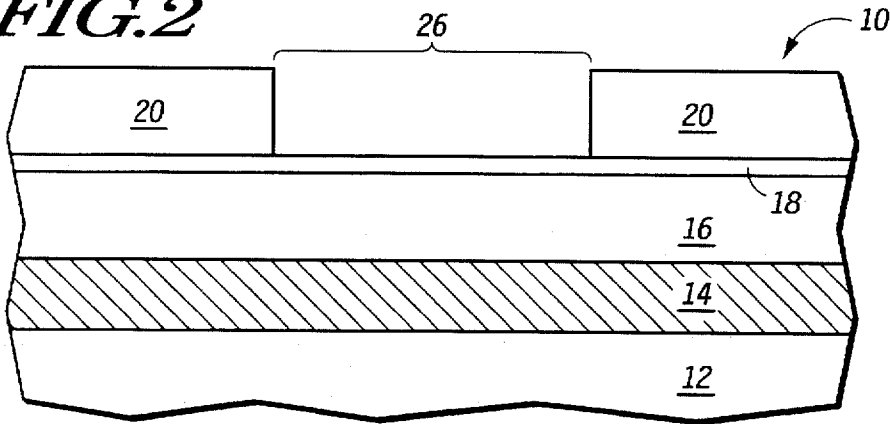
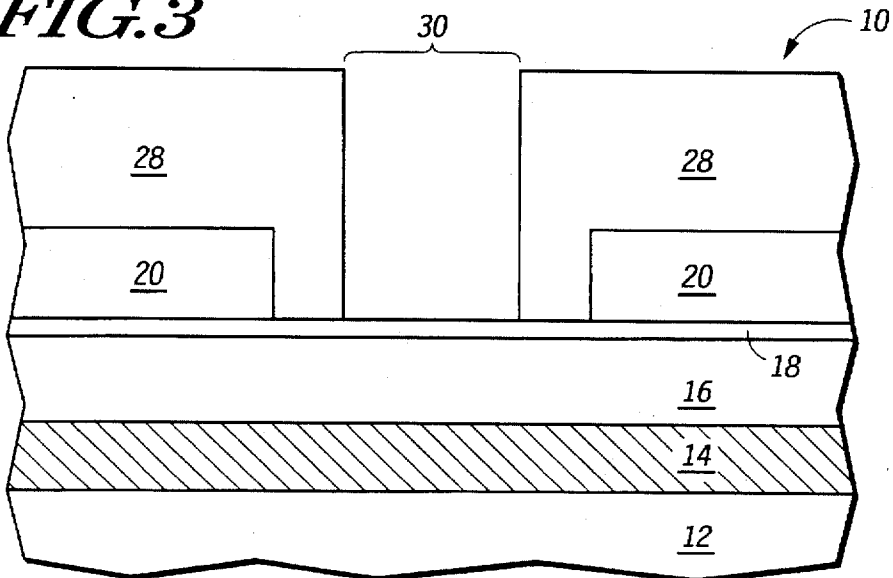
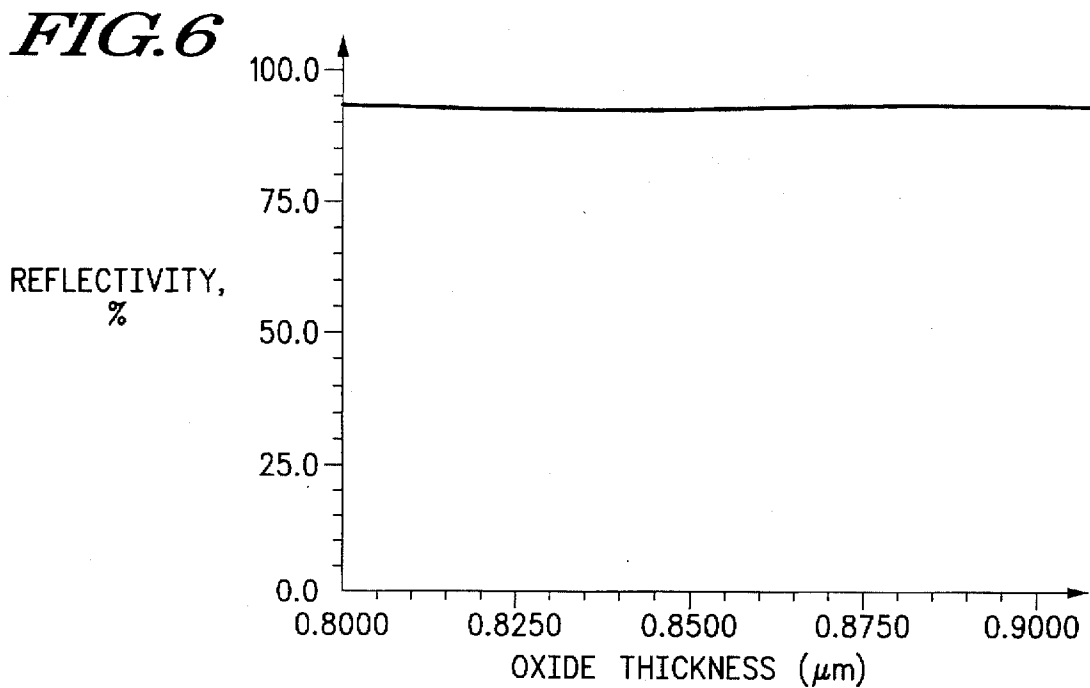
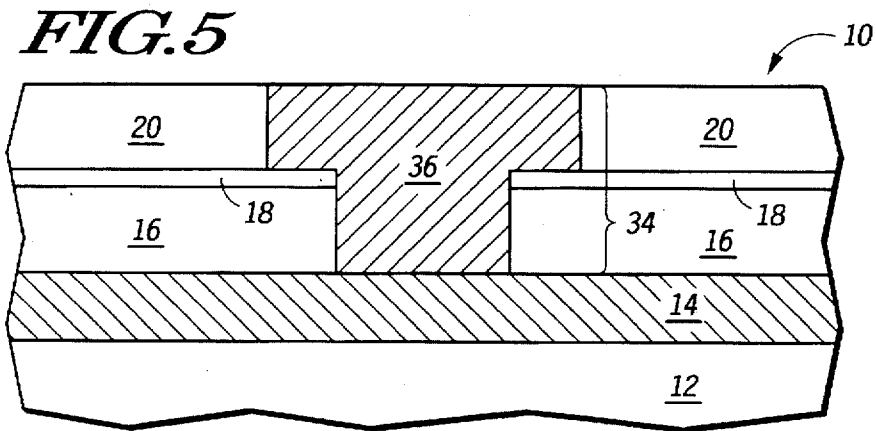
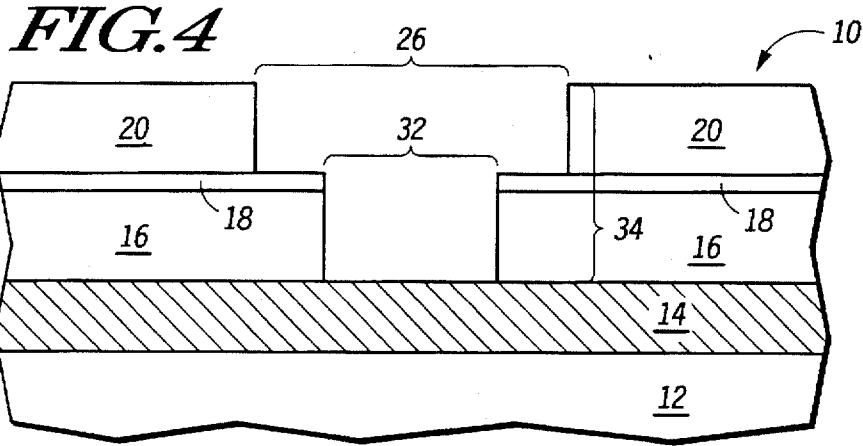


FIG. 3





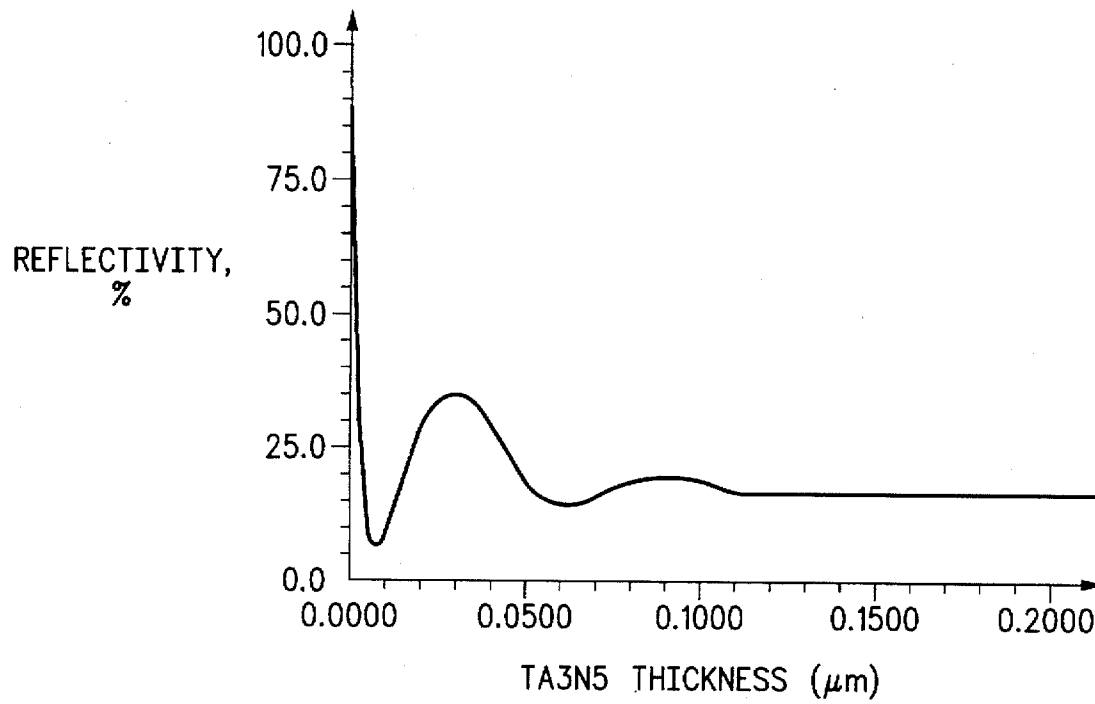


FIG. 7

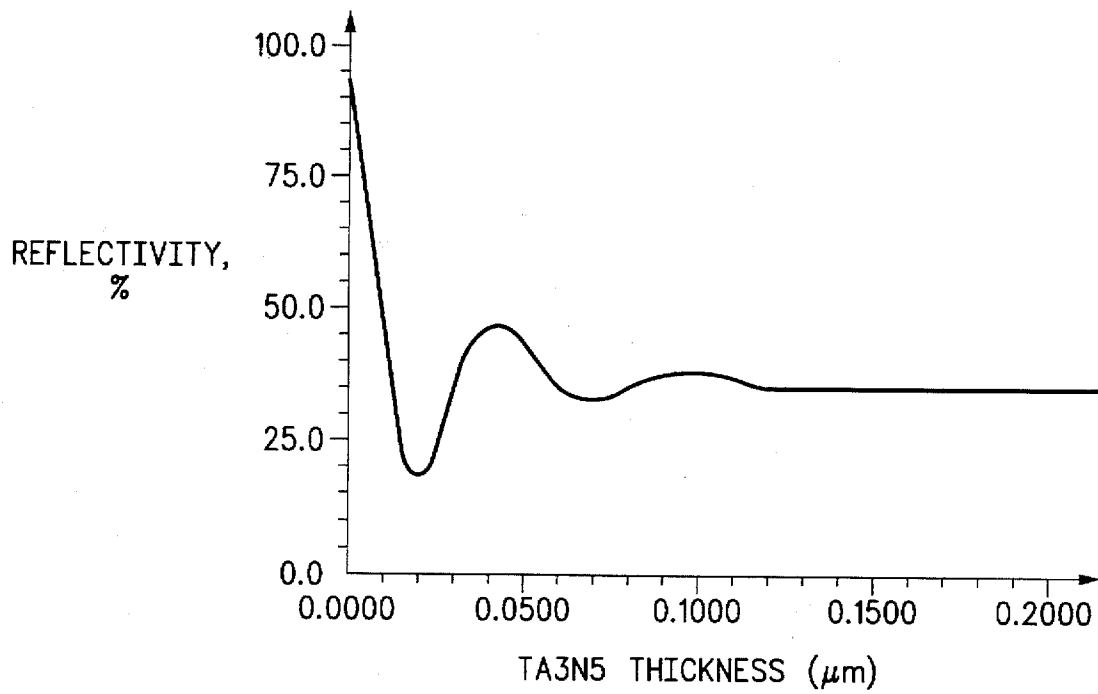


FIG. 8

FIG. 9

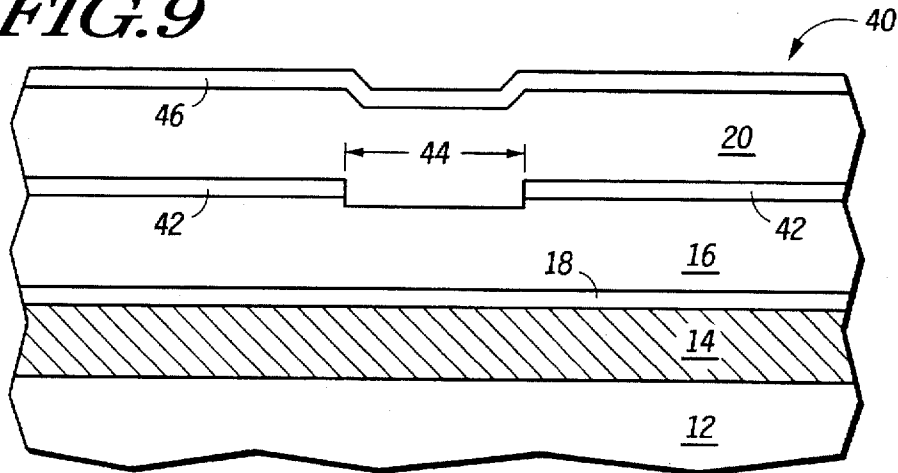


FIG. 10

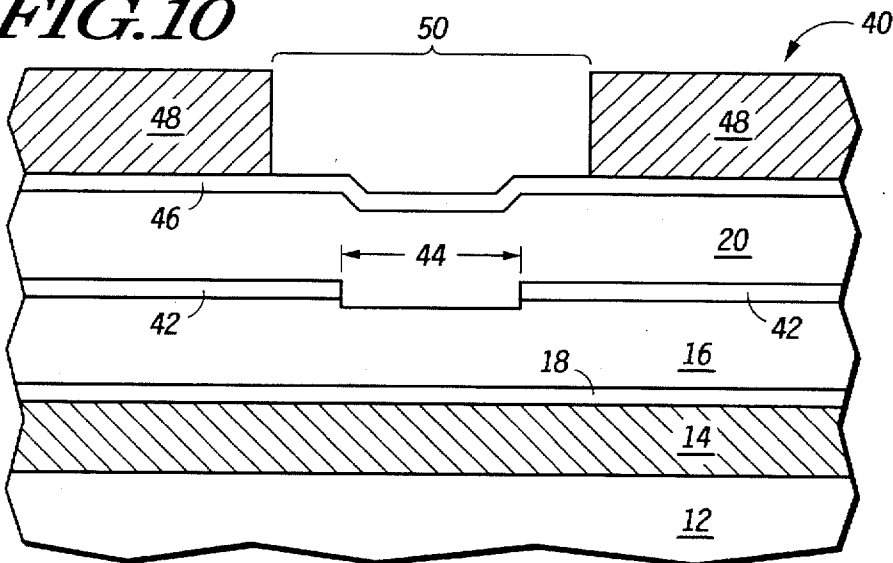
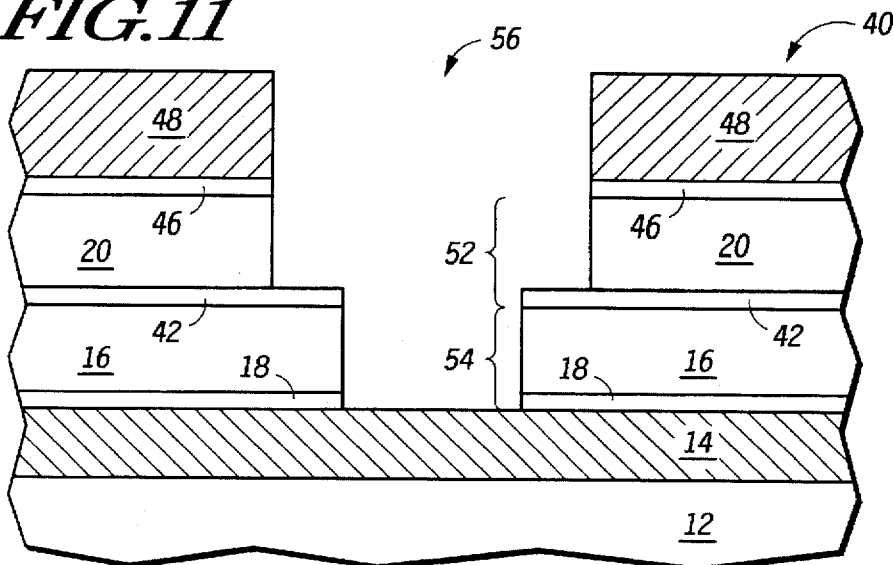


FIG. 11



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