



US005635423A

United States Patent [19]

[11] Patent Number: **5,635,423**

Huang et al.

[45] Date of Patent: **Jun. 3, 1997**

[54] **SIMPLIFIED DUAL DAMASCENE PROCESS FOR MULTI-LEVEL METALLIZATION AND INTERCONNECTION STRUCTURE**

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0 463 972 1/1992 European Pat. Off. .

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[75] Inventors: **Richard J. Huang; Angela Hui**, both of Milpitas; **Robin Cheung**, Cupertino; **Mark Chang**, Los Altos; **Ming-Ren Lin**, Cupertino, all of Calif.

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[73] Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, Calif.

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[21] Appl. No.: **320,516**

Proceedings of the 8th International IEEE VLSI Multilevel Interconnection Conference, Santa Clara, CA, USA, Jun. 11-12, 1991, pp. 144-152, Kaanta et al., "Dual damascene: a ULSI wiring technology".

[22] Filed: **Oct. 11, 1994**

[51] Int. Cl.⁶ **H01L 21/44**

Joshi, "A New Damascene Structure for Submicrometer Interconnect Wiring," IEEE Electron Letters, vol. 14, No. 3, Mar. 1993, pp. 129-132.

[52] U.S. Cl. **437/195; 437/190; 437/203; 156/652.1; 156/653.1**

Kaanta et al., "Dual Damascene: A ULSI Wiring Technology," Jun. 11-12, 1991, VMIC Conference, IEEE, pp. 144-152.

[58] Field of Search **437/195, 190, 437/182, 203; 156/DIG. 652.1, DIG. 653.1**

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Primary Examiner—Charles L. Bowers, Jr.

Assistant Examiner—Lynne A. Gurley

[57] ABSTRACT

A semiconductor device containing an interconnection structure having a reduced interwiring spacing is produced by a modified dual damascene process. In one embodiment, an opening for a via is initially formed in a second insulative layer above a first insulative layer with an etch stop layer therebetween. A larger opening for a trench is then formed in the second insulative layer while simultaneously extending the via opening through the etch stop layer and first insulative layer. The trench and via are then simultaneously filled with conductive material.

13 Claims, 8 Drawing Sheets

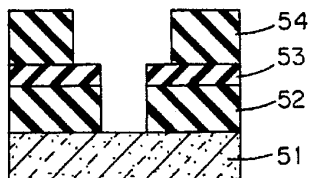
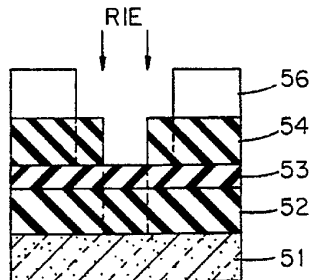


FIG. 1(a) PRIOR ART

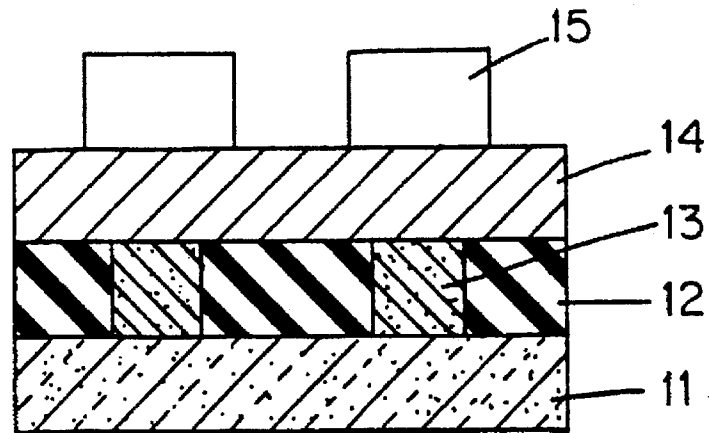


FIG. 1(b) PRIOR ART

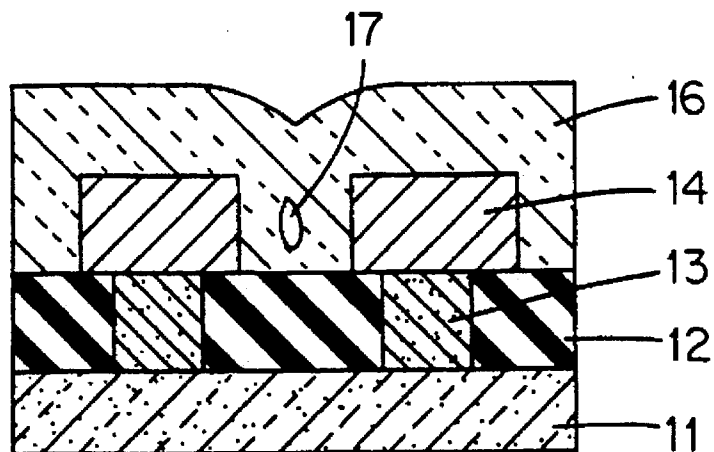


FIG. 2(a)
PRIOR ART

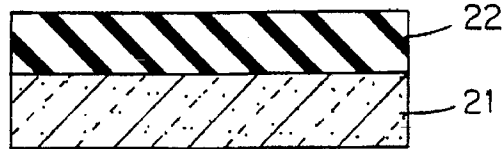


FIG. 2(b)
PRIOR ART

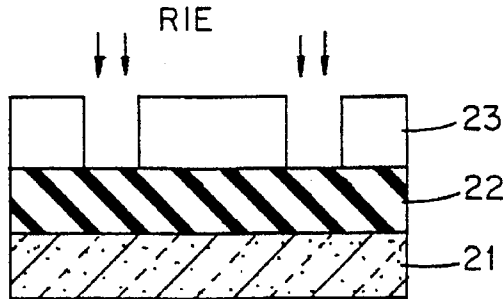


FIG. 2(c)
PRIOR ART

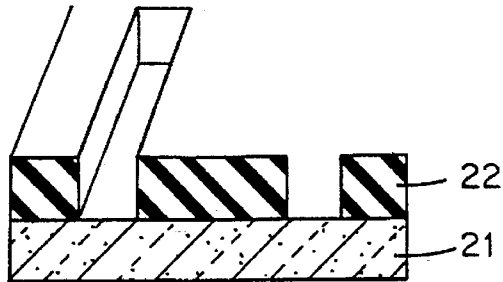


FIG. 2(d)
PRIOR ART

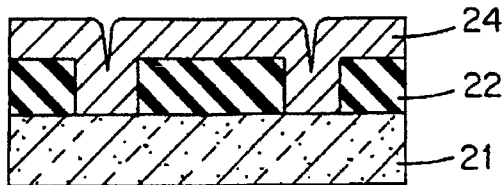


FIG. 2(e)
PRIOR ART

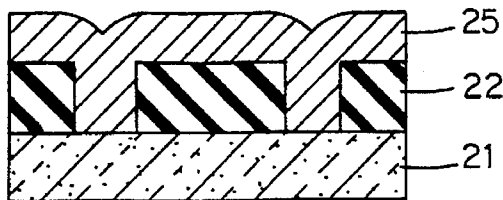


FIG. 3
PRIOR ART

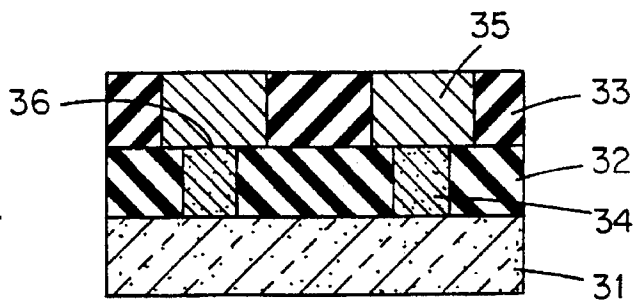


FIG. 4(a)
PRIOR ART

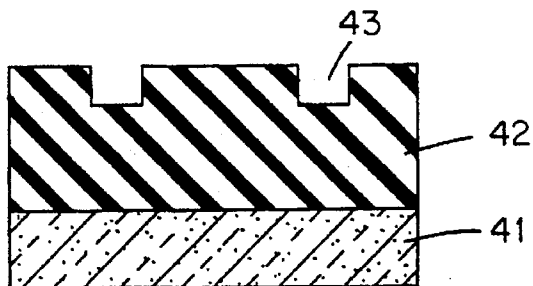


FIG. 4(b)
PRIOR ART

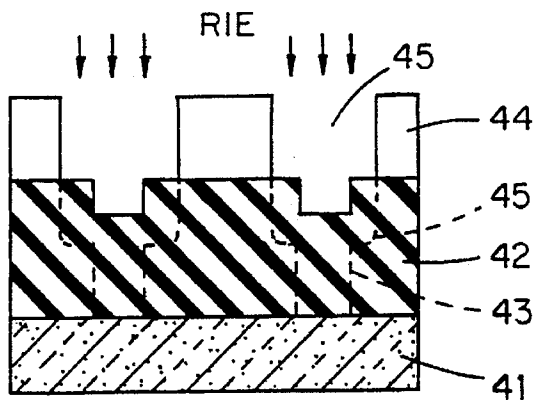


FIG. 4(c)
PRIOR ART

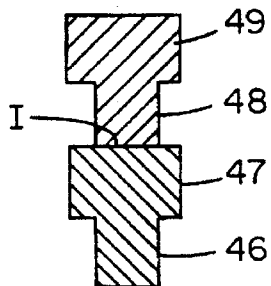


FIG. 5(a)

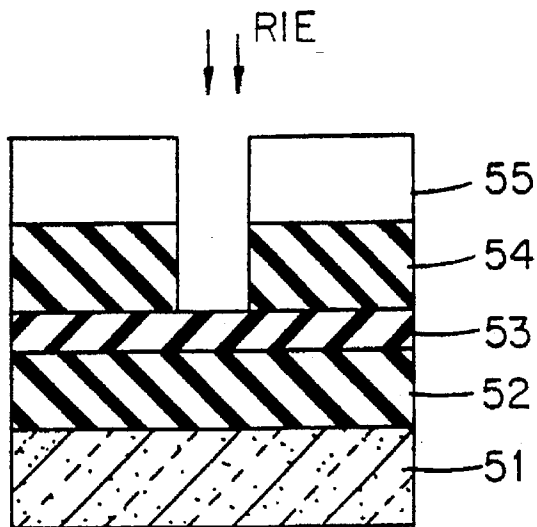


FIG. 5(b)

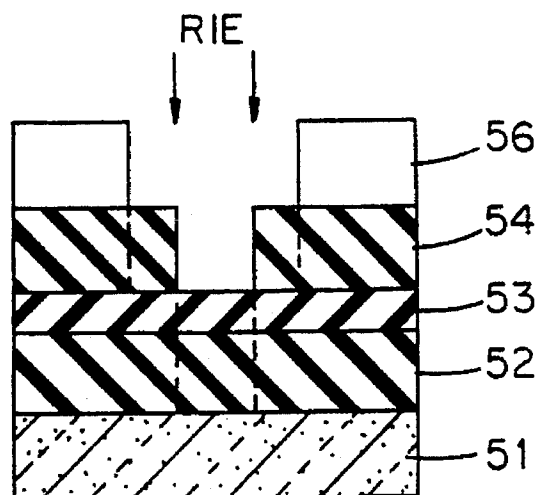
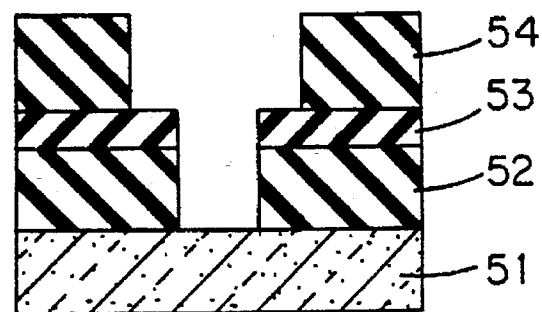


FIG. 5(c)



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